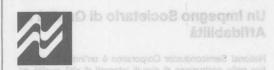


# FACT Advanced CMOS Logic Databook



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National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

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President, Chief Executive Officer National Semiconductor Corporation

Wir fühlen uns zu Qualität und

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FACTTM (Fairchild Advanced CMOS Technology) is a very high-speed, low power CMOS Logic family utilizing a 1.3  $\mu$ M Isoplanar silicon gate CMOS process. FACT logic functions can attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic: Ultra low static power and high noise immunity. FACT offers the system designer the added benefit of superior line driving characteristics and excellent ESD and Latch-up immunity.

FACT Quiet Series, an extension of the FACT family, is a high speed, low power CMOS family IDEAL for ACMOS applications requiring increased noise margins. Utilizing NSC Quiet Series Technology, FACT QS features GTO™ outputs control, undershoot corrector and a split ground bus for superior ACMOS performance. In addition, FACT QS features improved AC specifications, specifies maximum pin-to-pin output skew and provides enhanced ESD immunity and latch-up protection.

FACT FCT, an extension of the FACT family, features 7 ns propagation delays and 64/48 mA output drive. The series incorporates National's Quiet Series Technology to provide the lowest noise performance of any FCT logic family. FACT FCTA is the high speed, high drive extension of the FACT family featuring 5 ns maximum propagation delays and 64/48 mA output drive. In addition, FACT FCTA features quiet circuitry to provide increased noise margins.

The FACT/FACT QS families consist of devices in two categories:

- AC/ACQ—standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;
- ACT/ACTQ—standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

#### **Product Index and Selection Guide**

Lists FACT, FACT QS, FACT FCT, and FACT FCTA circuits currently available, in design or planned. The selection guide groups the circuits by function.

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Basic information on FACT performance including technologies.

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Contains common ratings and specifications for FACT devices, as well as AC test loads and waveforms.

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| The FACT/FACT QS families consist of devices in two categories:   |
| <ol> <li>AC/ACC—standard logic functions with CMOS compati-<br/>ble inputs and TTL and MOS compatible outputs;</li> </ol>   |
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#### Product Status Definitions

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| Data Sheet Identification     | Product Status            | Definition   |
|-------------------------------|---------------------------|--|
| Advance Information           | Formative or<br>In Design | This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.  |
| Preliminary                   | First<br>Production       | This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| No<br>Identification<br>Noted | Full<br>Production        | This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.   |

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| 54FCT/74FCT564 Octal D Flip-Flop with TRI-STATE Outputs                | 6  |
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| 54FCT/74FCT821A 10-Bit D Flip-Flop with TRI-STATE Outputs              |    |
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| 54FCT/74FCT823A 9-Bit D Flip-Flop with TRI-STATE Outputs               | 4  |
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| 54FCT/74FCT825A 9-Bit D Flip-Flop with TRI-STATE Outputs               |    |
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| 54FCT/74FCT827A 10-Bit Buffer/Line Driver with TRI-STATE Outputs       |    |
| 54FCT/74FCT827B 10-Bit Buffer/Line Driver with TRI-STATE Outputs       |    |
| 54FCT/74FCT841A 10-Bit Transparent Latch with TRI-STATE Outputs        |    |
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## FACT™ Selection Guide

#### Gates

| GIGITO GOV |                    |            |   |               |         |
|------------|--------------------|------------|---|---------------|---------|
| aeY        | Function           | OM         | ACT/74ACTG273                           | Device        | Octal D |
| Yes        | NAND               | CIA        | IFCT/74FCT273A                          | -3            | Octaf D |
|            | Quad 2-Input       |            | IAC/74AC374                             | 54AC/74AC00   |         |
|            | Quad 2-Input       |            | IACT/74ACT374                           | 54ACT/74ACT00 |         |
|            | Triple 3-Input     |            | IACQ/74ACQ374                           | 54AC/74AC10   |         |
|            | Triple 3-Input     |            | IACTQ/74ACTQ374                         | 54ACT/74ACT10 |         |
|            | Dual 4-Input       |            | IFCT/74FCT374                           | 54AC/74AC20   |         |
|            | AND                |            | IFCT/74FCT374A                          |               |         |
|            | Quad 2-Input       |            | AC/74AC377                              | 54AC/74AC08   |         |
|            | Quad 2-Input       | No<br>No   | EACT/74ACT377                           | 54ACT/74ACT08 |         |
|            | Triple 3-Input     |            | 110000000000000000000000000000000000000 | 54AC/74AC11   |         |
|            | OR/NOR/Exclusiv    |            | HETT/MECTS77                            |               |         |
|            | Quad 2-Input OR    | pM         | SECT/74ECT377A                          | 54AC/74AC32   |         |
|            | Quad 2-Input OR    |            | IACT/74ACT534                           | 54ACT/74ACT32 |         |
|            | Quad 2-Input NOR   |            | IACQ/74ACQ534                           | 54AC/74AC02   |         |
|            | Quad 2-Input NOR   |            | IACTO/74ACTOB3                          | 54ACT/74ACT02 |         |
|            | Quad 2-Input Exclu | sive-OR    | SPCT/74FCT534                           | 54AC/74AC86   |         |
|            | Inverter           | 3140-011   | (FOT/74FCT534A                          | 04/10/14/1000 |         |
|            | Hex Inverter       |            | (ACT/74ACT564                           | 54AC/74AC04   |         |
|            | Hex Inverter       |            | ACQ/74ACQ35ba                           | 54ACT/74ACT04 |         |
|            |                    | r Invertor | ASSETTION TO TOTAL                      | 54AC/74AC14   |         |
| No         | Hex Schmitt Trigge | rinverter  | 9001748771046                           | 54AC//4AC14   | Octal D |
| OVI        |                    |            |   |               |         |

#### Registers

| RAPOTURADO (A) | Inputs         |
|----------------|----------------|
| 54AC/74AC378   | No             |
| 54ACT/74ACT399 | 1(             |
| 54ACT/74ACT818 | 2 118-8        |
|                | 54ACT/74ACT399 |

#### **Parity Generator/Checkers**

| Function   | AFCRIONATUTORNA Device 0.18-0 |
|--|-------------------------------|
| Parity Generator/Checker                                       | 54AC/74AC280                  |
| Octal Bidirectional Bus Transceiver w/Parity Generator/Checker | 54ACTQ/74ACTQ657              |
| Octal Bidirectional Bus Transceiver w/Parity Generator/Checker | 54FCT/74FCT657                |
| 9-Bit Registered Transceiver w/Parity Generator/Checker        | 54AC/74AC899                  |
| 9-Bit Registered Transceiver<br>w/Parity Generator/Checker     | 54ACT/74ACT899                |
| 9-Bit Registered Transceiver<br>w/Parity Generator/Checker     | 54FCT/74FCT899                |

| Function      | Device   | TRI-STATE® Outputs | Master<br>Reset  |
|---------------|--|--------------------|--|
| Dual D        | 54AC/74AC74  | No                 | Yes  |
| Dual D        | 54ACT/74ACT74  | No                 | Yes  |
| Dual JK       | 54AC/74AC109   | No                 | Yes  |
| Dual JK       | 54ACT/74ACT109   | No                 | Yes  |
|               |  |                    | Yes  |
| Hex D         | 54AC/74AC174   | No                 |  |
| Hex D         | 54ACT/74ACT174   | No                 | Yes  |
| Quad D        | 54AC/74AC175   | No                 | Yes  |
| Quad D        | 54ACT/74ACT175   | No                 | Yes  |
| Octal D       | 54AC/74AC273   | No                 | Yes  |
| O-t-I D       | E440T/7440T0070  | Function of        | Yes  |
| Octal D       | 54AC1//4AC1Q2/3<br>54FCT/74FCT273  | No                 | Yes  |
|               | The state of the s | No                 | Yes  |
| Octal D       | 54FCT/74FCT273A  |                    | 100  |
| Octal D       | 54AC/74AC374   |                    |  |
| Octal D 00TOA | 54ACT/74ACT374   | Yes high           |  |
| Octal D       | 54ACQ/74ACQ374   |                    | I-E sight No   |
| Octal D       | 54ACTQ/74ACTQ374   | Yes tugn           | NI-  |
| Octol D       | 54FCT/74FCT374   | Voc                | No   |
| Octal D       | 54FCT/74FCT374A  | Yes                | No   |
|               |  |                    | No No  |
| Octal D       | 54AC/74AC377   | No<br>No           | The Control of the Co |
| Octal D       | 54ACT/74ACT377   | INO                | INO  |
| Octal D       | 54ACQ/74ACQ377   | 110                | No No  |
| Octal D       | 54ACTQ/74ACTQ377   | No fugn            | 1-8 signT No   |
| Octal D       | 54FCT/74FCT377   | No viestox3\       | ROMARO No  |
| Octal D       | 54FCT/74FCT377A  | No RO such         | No Ouad 2-i  |
|               | 54ACT/74ACT534   |                    | I-S bau No   |
| 0.110         | 54ACQ/74ACQ534   |                    |  |
|               | THE LOPPING  | V (ICIP) BIOD      | IF S. UZBABU   |
| Octal D SOTOA | 54ACTQ/74ACTQ534   | Yes ROM man        | No No  |
| Octal D       | 54FCT/74FCT534   | Yes                | NO NO  |
| Octal D       | 54FCT/74FCT534A  | Yes                | No   |
| Octal D       | 54ACT/74ACT564   | Yes                | No   |
| Octal D       | 54ACQ/74ACQ564   | Yes                | No No  |
| Octal D       | 54ACTQ/74ACTQ564   | Yes                |  |
| Octal D       | 54FCT/74FCT564   | netrYes report tim |  |
|               |  |                    | The second secon |
| Octal D       | 54FCT/74FCT564A  | Yes                | No   |
| Octal D       | 54AC/74AC574   | Yes                | No   |
| Octal D       | 54ACT/74ACT574   | Yes                | No   |
| Octal D       | 54ACQ/74ACQ574   | Yes                | No   |
| Octal D       | 54ACTQ/74ACTQ574   | Yes                | No   |
| Octal D       | 54FCT/74FCT574   | Yes                | No   |
| Octal D       | 54FCT/74FCT574A  | Yes eldenEl\w      |  |
|               |  | Yes                | Yes  |
| Octal D       | 54ACT/74ACT825   |                    |  |
| 8-Bit D       | 54FCT/74FCT825A/B  | Yes apart and a    |  |
| 9-Bit D       | 54ACT/74ACT823   | Yes                | Yes  |
| 9-Bit D       | 54FCT/74FCT823A/B  | Yes                | Yes  |
| 10-Bit D      | 54ACT/74ACT821   | Yes                | Yes  |
| 10-Bit D      | 54ACQ/74ACQ821   | Yes                | Yes  |
| 10-Bit D      | 54FCT/74FCT821A/B  | Yes                | Yes  |
| no bit b      | AARTAARS   |                    |  |
| 002           |  |                    |  |
|               |  |                    |  |
|               |  |                    |  |
|               |  |                    |  |
|               | SAFOT/74F  |                    |  |
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| _ | CIL | _ | - | - |

| Function           | Inverting/ | Device          | TRI-STATE<br>Outputs | Broadside<br>Pinout |
|--------------------|------------|-----------------|----------------------|---------------------|
| Octal              | 54A        | C/74AC373       | Yes                  | No                  |
| Octal              | 54A        | CT/74ACT373     | Yes                  | No                  |
| Octal Transparent  | 54A        | CQ/74ACQ373     | Yes                  | NobeuO              |
| Octal Transparent  | 54A        | CTQ/74ACTQ373   | 7 Yes ATATOANO       | Nobelia             |
| Octal Transparent  | 54F        | CT/74FCT373     | Yes ANTIOANA         | Notato              |
| Octal Transparent  | 54F        | CT/74FCT373A    | SAACT/74.89Y240      | NotatoO             |
| Octal D            | 54A        | CQ/74ACQ533     | SAACO/7ASPY2240      | No spo              |
| Octal D            | 54A        | CTQ/74ACTQ533   | OBCOT YES TOTOBAR    | Noisino             |
| Octal D            | 54F        | CT/74FCT533     | Yes                  | No                  |
| Octal D            | 54F        | CT/74FCT533A    | Yes                  |                     |
| Octal D            | 54A        | CT/74ACT563     | Yes                  | Yes                 |
| Octal D            |            | CQ/74ACQ563     | Yes                  | Yes                 |
| Octal D            |            | CTQ/74ACTQ563   | Yes                  | Yes                 |
| Octal D            | 54F        | CT/74FCT563     | SAACQ/7489Y241       | Yes                 |
| Octal D            | 1/1 54F    | CT/74FCT563A    | 54ACTQ/789YTO244     | Yes                 |
| Octal D            | M 54A      | C/74AC573       | BAPCT/7AIRSYDAT      | Yes                 |
| Octal D            | 54A        | CT/74ACT573     | AFACY SATITORAS      | Yes                 |
| Octal D            | 54A        | CQ/74ACQ573     | Yes                  | Yes                 |
| Octal D            | 54A        | CTQ/74ACTQ573   | Yes                  | Yes                 |
| Octal D            | 54F        | CT/74FCT573     | Yes                  | Yes                 |
| Octal D            | 54F        | CT/74FCT573A    | Yes                  | Yes                 |
| Octal Transparent  |            | CT/74ACT845     | Yes WOTOARE          | Yes                 |
| 8-Bit Transparent  |            | CT/74FCT845A/B  | Yes                  | Yes                 |
| 9-Bit Transparent  | 54A        | C/74AC843       | AAASYes ATATOTAG     | Yes                 |
| 9-Bit Transparent  |            | CT/74ACT843     | Yes AV YOAAE         | Yes xe              |
| 9-Bit Transparent  | 54A        | CTQ/74ACTQ843   | gar Yes ATTOANA      | Yes                 |
| 9-Bit Transparent  |            | CT/74FCTQ843A/B | Yes                  | Yes                 |
| 10-Bit Transparent |            | CT/74ACT841     | Yes                  | Yes                 |
| 10-Bit Transparent | 1.0        | CT/74FCT841A/B  | Yes                  | Yes                 |
| 10-Bit Transparent | 54A        | CTQ/74ACTQ841   | Yes                  | Yes                 |

#### Counters

| Counters        |                |                   |                            |     |                   |
|-----------------|----------------|-------------------|----------------------------|-----|-------------------|
| Function        | Device         | Parallel<br>Entry | Reset                      | U/D | TRI-STATE Outputs |
| 4-Bit Binary    | 54AC/74AC161   | S                 | A                          | No  | No                |
| 4-Bit Binary    | 54ACT/74ACT161 | S                 | A                          | No  | No                |
| 4-Bit Binary    | 54AC/74AC163   | S                 | S                          | No  | No                |
| 4-Bit Binary    | 54ACT/74ACT163 | durant S          | os S                       | No  | no somu No        |
| 4-Bit Binary    | 54AC/74AC169   | S                 |                            | Yes | No                |
| 4-Bit Binary    | 54ACT/74ACT169 | S Pare            | 54AC/ <del>74</del> AC2708 | Yes | IOMEM CHINO AS    |
| 4-Bit Binary    | 54AC/74AC191   | A Parelle         | SAACT#FAACT2708            | Yes | No No No          |
| S - Synohronous | Indianati d    | allowers          | TOTATO A CENTRAL CO        |     | A REPORT OF THE   |

S = Synchronous A = Asynchronous

<sup>|</sup> Decoders Derivation | Device | Low | Active |

| Function | Device           | Enable<br>Inputs<br>(Level) | Inverting/<br>Non-Inverting |
|----------|------------------|-----------------------------|-----------------------------|
| Quad     | 54AC/74AC125     | 1(L)                        | N SAACO                     |
| Quad     | 54ACT/74ACT125   | et(L) TOARTAG               | TOALS N                     |
| Octal M  | 54AC/74AC240     | 2(L)                        | I SAFOT                     |
| Octal    | 54ACT/74ACT240   | 2(L)                        | I SAFOT                     |
| Octal    | 54ACQ/74ACQ240   | 2(L)                        | I SAAGO                     |
| Octal    | 54ACTQ/74ACTQ240 | 2(L)                        | I SAACT                     |

54FCT/74FCT240

54FCT/74FCT240A

54AC/74AC241

54ACT/74ACT241

54ACQ/74ACQ241

54ACTQ/74ACTQ241

54FCT/74FCT827A/B

| Octai   | 04/10/10/10/10/10/10 | 1(11) 0 1(-)     | Children Control |   |   |
|---------|----------------------|------------------|------------------|---|---|
| Octal   | 54FCT/74FCT241       | 1(H) & 1(L)      | SAAC/            | N | No                                      |
| Octal   | 54FCT/74FCT241A      | 1(H) & 1(L)      | SAACT            | N | No                                      |
| Octal   | 54AC/74AC244         | 2(L)             | SAAGO            | N | No                                      |
| Octal   | 54ACT/74ACT244       | 2(L)             | TURNE            | N | No                                      |
| Octal   | 54ACQ/74ACQ244       | 2(L)             | TORKE            | N | No                                      |
| Octal   | 54ACTQ/74ACTQ244     | 2(L)             | TOALS            | N | No No                                   |
| Octal   | 54FCT/74FCT244       | 2(L)             | SAFCT            | N | No. 9                                   |
| Octal   | 54FCT/74FCT244A      | 2(L)             | SEACA            | N | In magener T No 8                       |
| Hex     | 54ACT/74ACT367       | 1(L) - 1 - 1 - 1 | SAACT            | N | IngraganaT No 9                         |
| Hex *** | 54ACT/74ACT368       | 1(L) TOASTIC     | SAACTI           | 1 | 9 on Transparent                        |
| Octal   | 54AC/74AC540         | 2(L)             | SAFOT            | 1 | Yes Yes                                 |
| Octal   | 54FCT540             | 2(L)             | TUAPE            | 1 | Yes                                     |
| Octal   | 54AC/74AC541         | 1(H) & 1(L)      | TOANS            | N | Yes                                     |
| Octal   | 54FCT541             | 1(H) & 1(L)      | 11.000           | N | Yes                                     |
| 10-Bit  | 54ACTQ/74ACTQ827     | 2(L)             |                  | N | Yes                                     |
|         |                      |                  |                  |   | 100 100 100 100 100 100 100 100 100 100 |

2(L)

2(L)

1(H) & 1(L)

1(H) & 1(L)

1(H) & 1(L)

1(H) & 1(L)

Broadside Pinout

No No No No No. O No O No

1

N

N

N

SAFOT

No

No

No

No

O No

Yes

Function

No

L = LOW H = HIGH

10-Bit

Octal

Octal

Octal

Octal

Octal

Octal

#### **FIFOs**

| Function  | Device                             | Input 88             | Output               | TRI-STATE<br>Outputs |
|---|------------------------------------|----------------------|----------------------|----------------------|
| 64 x 9 FIFO Memory<br>64 x 9 FIFO Memory                    | 54AC/74AC2708<br>54ACT/74ACT2708   | Parallel Parallel    | Parallel Parallel    | Yes                  |
| 512 x 9 FIFO Memory<br>512 x 9 Bidirectional<br>FIFO Memory | 54ACT/74ACT2725<br>54ACT/74ACT2726 | Parallel<br>Parallel | Parallel<br>Parallel | Yes<br>Yes           |

2(L)

#### **Decoders/Demultiplexers**

| Function    | Device          | LOW<br>Enable | Active-<br>HIGH<br>Enable | Active-<br>LOW<br>Outputs | Active-<br>Address<br>Inputs |
|-------------|-----------------|---------------|---------------------------|---------------------------|------------------------------|
| 1-of-8      | 54AC/74AC138    | 2             | 1                         | 8                         | 3                            |
| 1-of-8      | 54ACT/74ACT138  | 2             | 1                         | 8                         | 3                            |
| 1-of-8      | 54FCT/74FCT138  | 2             | 1                         | 8                         | 3                            |
| 1-of-8      | 54FCT/74FCT138A | 2             | 1                         | 8                         | 3                            |
| Dual 1-of-4 | 54AC/74AC139    | 1 & 1         | No                        | 4 & 4                     | 2 & 2                        |
| Dual 1-of-4 | 54ACT/74ACT139  | 1 & 1         | No                        | 4 & 4                     | 2 & 2                        |

#### **Arithmetic Functions**

| FUTATE INT. FUT | Function iden3                                   |     | evice                 | Features   |  |  |
|-----------------|--|-----|-----------------------|--|--|--|
|                 | 16 x 16 Multiplier Arithmetic Logic Unit for DSP |     | 74ACT1016<br>74ACT705 | 2s Complement & Unsigned Arithmetic<br>16-Bit ALU and 8 x 8 Parallel |  |  |
|                 | (J)1   | 014 | 74AC246               | DAM Multiplier/Accumulator Isnotosible lato                          |  |  |

#### Video Support

| aeY Function (J)     | SAFCT/74FCT245 90iv9D No | rev Features anotice this late?                  |
|----------------------|--------------------------|--|
| Video Sync Generator | 54ACT/74ACT715           | High Speed, Programmable Video Signal Generation |

### Shift Registers

| 86 Function       | (H) F & | (d) t | Device ay    | No. of<br>Bits | Reset | Serial<br>Inputs | TRI-STATE<br>Outputs |
|-------------------|---------|-------|--------------|----------------|-------|------------------|----------------------|
| Octal Shift/Stora | ge      | 54    | AC/74AC299   | 8              | A     | 2                | Yes                  |
| Octal Shift/Stora | ge      | 54.   | ACT/74ACT299 | 8              | Α Α   | 2                | Yes                  |
| Octal Shift/Stora | ge      | 54.   | AC/74AC323   | 8              | S     | 2                | Yes                  |
| Octal Shift/Stora | ge      | 54.   | ACT/74ACT323 | 8              | S     | 2                | Yes                  |

A = Asynchronous S = Synchronous

#### Multiplexers

| Function     | 1 & (J) Perice OM | Enable Inputs (Level)        | True<br>Output | Complement<br>Output |
|--------------|-------------------|------------------------------|----------------|----------------------|
| 8-Input      | 54AC/74AC151      | 1(L)                         | Yes            | 189\w bots Yes       |
| 8-Input      | 54ACT/74ACT151    | eearo <sub>1(L)</sub> OTOANE | Yes            | Yes A HE-C           |
| 8-Input      | 54AC/74AC251      | 66611(F) 11038               | Yes            | Yes Hills            |
| 8-Input      | 54ACT/74ACT251    | 1(L)                         | Yes            | Yes                  |
| Dual 4-Input | 54AC/74AC153      | 2(L)                         | Yes            | No                   |
| Dual 4-Input | 54ACT/74ACT153    | 2(L)                         | Yes            | No                   |
| Dual 4-Input | 54ACTQ/74ACTQ153  | 2(L)                         | Yes            | No                   |
| Dual 4-Input | 54AC/74AC253      | 2(L)                         | Yes            | No                   |
| Dual 4-Input | 54ACT/74ACT253    | 2(L)                         | Yes Ware       | mummil 8 No          |
| Quad 2-Input | 54AC/74AC157      | 8 1(L)                       | Yes Ware       | muminiM 8 No         |
| Quad 2-Input | 54ACT/74ACT157    | 1(L)                         | Yes            | No                   |
| Quad 2-Input | 54AC/74AC158      | 1(L)                         | No             | Yes                  |
| Quad 2-Input | 54ACT/74ACT158    | 1(L)                         | No             | Yes                  |
| Quad 2-Input | 54AC/74AC257      | 1(L)                         | Yes            | No                   |
| Quad 2-Input | 54ACT/74ACT257    | 1(L)                         | Yes            | No                   |
| Quad 2-Input | 54AC/74AC258      | 1(L)                         | No             | Yes                  |
| Quad 2-Input | 54ACT/74ACT258    | 1(L)                         | No             | Yes                  |

#### Comparators

| Function                  | Device          | Features   |
|---------------------------|-----------------|------------|
| Octal Identity Comparator | 54AC/74AC520    | Expandable |
| Octal Identity Comparator | 54ACT/74ACT520  | Expandable |
| Octal Identity Comparator | 54AC/74AC521    | Expandable |
| Octal Identity Comparator | 54ACT/74ACT521  | Expandable |
| Octal Identity Comparator | 54FCT/74FCT521  | Expandable |
| Octal Identity Comparator | 54FCT/74FCT521A | Expandable |

#### Transceivers/Registered Transceivers

| Complement & Continued State       | Device Device    | Registered | Enable Inputs (Level) | TRI-STATE Output |
|------------------------------------|------------------|------------|-----------------------|------------------|
| Octal Bidirectional Transceiver    | 54AC/74AC245     | No         | 1(L)                  | Yes              |
| Octal Bidirectional Transceiver    | 54ACT/74ACT245   | No         | 1(L)                  | Yes              |
| Octal Bidirectional Transceiver    | 54ACQ/74ACQ245   | No         | 1(L)                  | Yes              |
| Octal Bidirectional Transceiver    | 54ACTQ/74ACTQ245 | No         | 1(L)                  | Yes              |
| Octal Bidirectional Transceiver    | 54FCT/74FCT245   | No No      | 1(L) nelfar           | Yes              |
| Octal Bidirectional Transceiver    | 54FCT/74FCT245A  | No No      | 1(L)                  | Yes              |
| Octal Bus Transceiver and Register | 54AC/74AC646     | Yes        | 1(L) & 1(H)           | Yes              |
| Octal Bus Transceiver and Register | 54ACT/74ACT646   | Yes        | 1(L) & 1(H)           | Yes              |
| Octal Bus Transceiver and Register | 54ACQ/74ACQ646   | Yes        | 1(L) & 1(H)           | Yes              |
| Octal Bus Transceiver and Register | 54ACTQ/74ACTQ646 | Yes        | 1(L) & 1(H)           | Yes              |
| Octal Bus Transceiver and Register | 54FCT/74FCT646   | Yes        | 1(L) & 1(H)           | Yes              |
| Octal Bus Transceiver and Register | 54FCT/74FCT646A  | Yes        | 1(L) & 1(H)           | Yes              |
| Octal Bus Transceiver and Register | 54AC/74AC648     | Yes        | 1(L) & 1(H)           | Yes              |
| Octal Registered Transceiver       | 54ACQ/74ACQ543   | Yes        | 2(L)                  | Yes              |
| Octal Registered Transceiver       | 54ACT/74ACTQ543  | Yes        | 2(L)                  | Yes              |
| Octal Registered Transceiver       | 54FCT/74FCT543   | Yes        | 2(L)                  | Yes              |
| Octal Registered Transceiver       | 54FCT/74FCT543A  | Yes        | 2(L)                  | Yes              |
| Octal Registered Transceiver       | 54ACQ/74ACQ544   | Yes        | 2(L)                  | Yes              |
| Octal Registered Transceiver       | 54ACT/74ACTQ544  | Yes        | 2(L)                  | Yes              |
| Octal Registered Transceiver       | 54FCT/74FCT544   | Yes        | 2(L)                  | Yes              |
| Octal Registered Transceiver       | 54FCT/74FCT544A  | Yes        | 2(L)                  | Yes              |
| Octal Bus Transceiver              | 54ACTQ/74ACTQ657 | 34         | 1(L) & 1(H)           |                  |
| Octal Bus Bidirectional            | 54FCT/74FCT657   | No         | 1(L) & 1(H)           | nella Yes        |
| Transceiver w/Parity               |                  |            |                       |                  |
| 9-Bit Registered w/Parity          | 54ACQ/74AC899    | Yes        | 1 (L) & 1 (H)         | Yes              |
| 9-Bit Registered w/Parity          | 54ACTQ/74ACT899  | Yes        | 1 (L) & 1 (H)         | Yes              |
| 9-Bit Registered w/Parity          | 54FCT/74FCT899   | Yes        | 1 (L) & 1 (H)         | Yes              |

#### Clock Drivers

| Function  1 to 8 Minimum Skew Clock Driver 1 to 8 Minimum Skew Clock Driver |     | Function 89Y U)S Device TOAHTOTOAHS |                                | Multiplexed<br>Clock |  |
|---|-----|-------------------------------------|--------------------------------|----------------------|--|
|   |     | 2(L)<br>1(L)                        | 54AC/74AC2525<br>54AC/74AC2526 | No Yes               |  |
| 0/1   | Yes | (J) 1                               | SAACT/ZAACT157                 | Oued 2-Input         |  |
|   |     |                                     |                                |                      |  |
|   | No  |                                     |                                |                      |  |
|   |     |                                     |                                |                      |  |
|   |     |                                     |                                |                      |  |
|   |     |                                     |                                |                      |  |
|   |     |                                     |                                |                      |  |

| Features |                                |  |
|----------|--------------------------------|--|
|          | SAAC/74AC520<br>SAACT/74ACT520 |  |
|          |                                |  |
|          |                                |  |
|          |                                |  |
|          |                                |  |



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#### **Section 1 Contents**

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#### FACT™ Descriptions and Family Characteristics

#### National Semiconductor Advanced CMOS Technology—FACT—Logic

Fairchild Semiconductor introduced FACT (Fairchild Advanced CMOS Technology) logic, a family of high speed advanced CMOS circuits, in 1985.

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor tech-

The 1.3-micron silicon gate CMOS process utilized in this family has been proven in the field of high performance gate arrays, CMOS ASIC, and FACT. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

In 1989, National Semiconductor introduced the FACT Quiet SeriesTM product line. This line of mostly octal bus-oriented logic functions is an enhancement of the original FACT line. Manufactured on a sub-micron silicon gate CMOS process, the FACT QS devices offer the lowest noise characteristics of any Advanced CMOS process with AC performance that is faster than FACT.

Also in 1989, National Semiconductor introduced its offering of fast CMOS technology or FACT FCT/FCTA. These product lines offer the fastest speeds of any TTL or CMOS logic, high DC output current drive, as well as the low noise design innovations of FACT QS.

For direct replacement of LS, ALS and other TTL devices, the 'ACT, 'ACTQ, 'FCT and 'FCTA circuits with TTL-type input thresholds are included in the FACT family.

#### Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX
- TTL Inputs on Selected Circuits
- High Performance Outputs
  - Common Output Structure for Standard Gates and Buffer/Drivers
  - Output Sink/Source Current of 24 mA on AC/ACT and ACQ/ACTQ
  - Output Sink/Source Current of 48/64 mA on FCT/FCTA
  - Transmission Line Driving  $50\Omega$  (Commercial)/75 $\Omega$ (Military) Guaranteed

- Operation from 2V-6V VDD Guaranteed ('AC/'ACQ)
- Temperature Range

— Commercial

-40°C to +85°C -55°C to +125°C

- Military

- Improved ESD Protection Network
- High Current Latch-Up Immunity
- Patented Noise Suppression Circuitry on ACQ/ACTQ and FCT/FCTA

#### Interfacing

FACT devices have a wide operating voltage range (VDD = 1) 2 VDC to 6 VDC, 'AC/'ACQ) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

'AC/'ACQ - These are high speed CMOS devices with CMOS input switching levels and buffered CMOS outputs that can drive ±24 mA of IOH and IOI current. Industry standard 'AC/ 'ACQ nomenclature and pinouts are used.

'FCT/'FCTA

'ACT/'ACTQ - These are high speed CMOS devices with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a  $V_{DD} = 5V$  $\pm 0.5V$  with  $V_{OH} = 2.4V$  and  $V_{OI} = 0.4V$ , but are functional over the entire FACT operating voltage range of 2.0 VDC to 5.5 V<sub>DC</sub>. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT/'ACTQ devices have the same output structures as 'AC/'ACQ devices. 'FCT/'FCTA can drive +64 mA of lot and -15 mA of lot current.

#### **Low Power CMOS Operation**

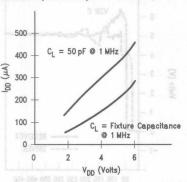
If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws 1000 times less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown be-

FACT = 0.1 mW/Gate = 1.2 mW/Gate LS = 2.0 mW/Gate

= 0.1 mW/Gate

|  | FACT Product Compar  | ISION  | LILLIA FERTS   |
|--|--|--|--|
| Feature  | FACT AC/ACT  | FACT ACQ/ACTQ  | FACT FCT/FCTA  |
| Dynamic line driving guaranteed to switch on incident wave into transmission line impedance as low as $50\Omega$ at $+85^{\circ}$ C; $75\Omega$ at $+125^{\circ}$ C  | Yes<br>I <sub>OLD</sub> /I <sub>OHD</sub> : ±75 mA             | Yes I <sub>OLD</sub> /I <sub>OHD</sub> : ±75 mA                                  | ALAM Semicond  |
| Guaranteed High Output Drive   | I <sub>OL</sub> /I <sub>OH</sub> : ±24 mA                      | I <sub>OL</sub> /I <sub>OH</sub> : ±24 mA  | I <sub>OL</sub> : +64 mA Commercial<br>(Buffers/Drivers)<br>+48 mA Military<br>I <sub>OH</sub> : -15 mA  |
| Very High Speed Frequency<br>(ODA*\OA*) begins reu0 ggV V8-V5 mon<br>spns Flee   | 1 ns Internal Gate Delay;<br>up to 100 MHz<br>Toggle Frequency | ≤1 ns Internal Gate Delay;<br>up to 100 MHz<br>Toggle Frequency                  | ≤1 ns Internal Gate Delay<br>up to 200 MHz<br>Toggle Frequency   |
| CMOS Power   | 5 μW/Gate  | 5 μW/Gate  | 5 μW Gate  |
| CMOS Input Loading   | ±1 μΑ  | ±1 μA Αμ 1±  | advanced OMOS Au 1±  |
| Extended Operating Voltage Range   | 2.0V to 6.0V   | 2.0V to 6.0V   | 2.0V to 6.0V   |
| DC/AC Characteristics Guaranteed   | 3V and 5V ±10%   | 3V and 5V ±10%   | 5V ±5% Commercial<br>5V ±10% Military  |
| Excellent Symmetrical Noise Margin (CMOS Inputs)   | 1.55V High; 1.55V Low  | 1.55V High; 1.55V Low  | neations as well as mall<br>flons and comparing the<br>nolonies.   |
| Dynamic Thresholds (TTL-Compatible Inputs)   | n this 2 Voc to 6 Voc gate interface with r an- Davice design  | Maximum 2.2V High (V <sub>IHD</sub> ); Minimum 0.8V Low (V <sub>ILD</sub> )      | Maximum 2.2V High<br>(V <sub>IHD</sub> ); Minimum 0.8V<br>Low (V <sub>ILD</sub> )  |
| Guaranteed Latchup Immunity  | ±100 mA at +125°C  | ±300 mA at +125°C  | TeACXX logic   |
| ESD Immunity evinb has lart alugho 20M0  | MIL Class 2 (2,000V - 3,999V); Typical 6,000V                  | MIL Class 2 (2,000V - 3,999V); Typical 6,000V                                    | MIL Class 3 (4,000V or Greater); Typical 6,000   |
| Pin-to-Pin Output Propagation Delay Skew<br>(Maximum)  | ARDI<br>Saro- 'FOT/'ACTO<br>Saro- 'FOT/'ECTA                   | 1.0 ns (t <sub>OS</sub> ); Typical 0.5 ns  | ed logic runctions is an eline. Manufactured on a sone the FACT OS deviced in the FACT OS d |
| Wafer Fabrication   Dengleeb ens alugal solv   | JAN Class S<br>DESC Certified                                  | CMOS process with AC per<br>ACT.   | teristics of any Advanced<br>ance that is faster than F  |
| Guaranteed Output Noise Levels (Maximum) V DS to egnist egisticy grifting suction benefited event equipment against a company on this section of the company | iering<br>priod-<br>logio,<br>exign<br>rices,<br>-type         | 1.5V V <sub>OLP</sub> (ground<br>Bounce); -1.2V V <sub>OLV</sub><br>(Undershoot) | FCTA: -1.2V V <sub>OLV</sub><br>(Undershoot)<br>FCT: 2.0V V <sub>OLP</sub><br>(Ground Bounce)<br>-1.2V V <sub>OLV</sub><br>(Undershoot)  |
| Driving Force for JEDEC Standard for Advanced CMOS   | Yes  | ded in the FACT family.  | input thresholds are inclu   |
| Inherently Radiation Tolerant  | Yes  | Yes  | Yes Full Logic Product SeY   |
| Inputs Compatible with: CMOS<br>TTL  | AC ACT   | ACQ 2 2 2000 One and to<br>ACTQ  | FCT, FCTA ISJ bas  |
| Ful Compatibility (Function, Part Number, Pinout) with Standard 54/74 Functions  | Yes 21 Inel  | Yes (≥8 Bits)  | Yes (≥8 Bits)  |

## Low Power CMOS Operation (Continued)



TL/F/10158-1

FIGURE 1-1. I<sub>DD</sub> vs V<sub>DD</sub>

Figure 1-1 illustrates the effects of  $I_{DD}$  versus power supply voltage ( $V_{DD}$ ) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

#### **AC Performance**

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The examples below describe typical values for a 74XX138, 3-to-8 line decoder and a 74xx244 line driver.

```
'138

FACT AC = 6.0 \text{ ns } @ \text{ C}_L = 50 \text{ pF}

ALS = 12.0 \text{ ns } @ \text{ C}_L = 50 \text{ pF}

LS = 22.0 \text{ ns } @ \text{ C}_L = 15 \text{ pF}

HC = 17.5 \text{ ns } @ \text{ C}_L = 50 \text{ pF}
```

```
'244

FACT FCTA = 3.0 ns @ C<sub>L</sub> = 50 pF

FACT ACQ = 4.0 ns @ C<sub>L</sub> = 50 pF

FACT AC = 5.0 ns @ C<sub>L</sub> = 50 pF

ALS = 7.0 ns @ C<sub>L</sub> = 50 pF

LS = 12.0 ns @ C<sub>L</sub> = 45 pF

HC = 14.0 ns @ C<sub>L</sub> = 50 pF
```

AC performance specifications are guaranteed at 5.0V  $\pm 0.5$ V and 3.3V  $\pm 0.3$ V. For worst case design at 2.0V VDD on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0V  $\rm V_{DD} = 1.9 \times AC$  specification at 3.3V.

#### **Multiple Output Switching**

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and  $5.0V \pm 10\% \ V_{DD}$ .

#### Noise Immunity of sucto O simenvo

The DC noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage,  $|V_{IL} - V_{OL}|/|V_{IH} - V_{OH}|$  at 4.5V  $V_{DD}$ .

FACT = 1.25V/1.25V ALS = 0.4V/0.7V LS = 0.3V/0.7V @ 4.75V V<sub>DD</sub> HC = 0.8V/1.25V

#### **Output Characteristics**

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC/'ACQ and 'ACT/'ACTQ device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times. All SSI and MSI devices ('AC, 'ACT, 'ACQ or 'ACTQ) are guaranteed to source and sink 24 mA. FACT FCT and FACT FCTA are guaranteed to sink 64 mA (comm)/48 mA (mil) and source 15 mA (comm)/12 mA (mil). Commercial devices, 74AC/ACTXXX, are capable of driving 50Ω transmission lines, while military grade devices, 54AC/ACTXXXX, can drive 75Ω transmission lines.

#### I<sub>OL</sub>/I<sub>OH</sub> Characteristics

FACT AC/ACT = 24 mA/-24 mA
FACT ACQ/ACTQ = 24 mA/-24 mA
FACT FCT/FCTA = 64 mA/-15 mA
ALS = 24 mA/-15 mA
LS = 8 mA/-0.4 mA @ 4.75V V<sub>DD</sub>
HC = 4 mA/-4 mA

#### **Dynamic Output Drive**

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied "typical" output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these "typical" performance values across the operating voltage and temperature limits. Fortunately for the system designers, FACT has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as  $50\Omega$  for the commercial temperature range and  $75\Omega$  for the military temperature range.

Figure 1-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ( $I_{OUT} > 0$ ), are the  $V_{OH}$  and  $I_{IH}$  curves for FACT logic while on the left side ( $I_{OUT} < 0$ ), are the curves for  $V_{OL}$  and  $I_{IL}$ . Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

#### Dynamic Output Drive (Continued)

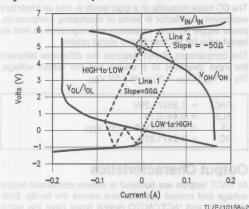


FIGURE 1-2. Gate Driving  $50\Omega$  Line Reflection Diagram is a second to the

Begin analysis at the VOL (quiescent) point. This is the intersection of the VOL/IOL curve for the output and the VIN/IIN curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a  $50\Omega$  load line from this intersection to the  $V_{\mbox{OH}}/I_{\mbox{OH}}$  curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95V. Then draw a line with a slope of  $-50\Omega$  from this first intersection point to the V<sub>IN</sub>/I<sub>IN</sub> curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the VOH/IOH curve should have positive slopes while lines terminating on the V<sub>IN</sub>/I<sub>IN</sub> curve should have negative slopes. Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the VOH/IOH curve will be waves travelling from the driver to the receiver while intersection points on the V<sub>IN</sub>/I<sub>IN</sub> curve will be waves travelling from the receiver to the driver.

Figures 1-3a thru 1-3d show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

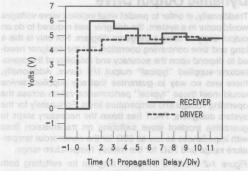


FIGURE 1-3a. Resultant Waveforms Driving
50Ω Line—Theoretical

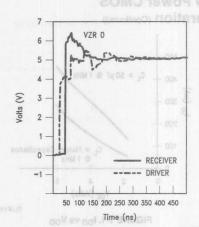


FIGURE 1-3b. Resultant Waveforms Driving
50Ω Line—Actual

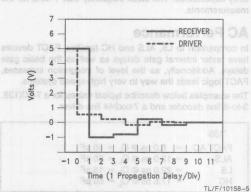


FIGURE 1-3c. Resultant Waveforms Driving 50Ω Line—Theoretical

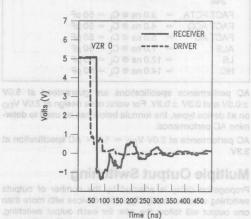


FIGURE 1-3d. Resultant Waveforms Driving 50Ω Line—Actual

#### **Dynamic Output Drive (Continued)**

While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V $_{DD}$ . The formula for calculating the current and voltage required is  $|(V_{QQ}-V_I)/Z_O|$  at  $V_I$ . For  $V_{QQ}=100$  mV,  $V_{IH}=3.85$ V,  $V_{DD}=5.5$ V and  $Z_{Q}=50\Omega$ , the required  $I_{QH}$  at 3.85V is 75 mA. For the HIGH-to-LOW transition,  $V_{QQ}=5.4$ V,  $V_{IL}=1.65$ V and  $Z_{Q}=50\Omega$ ,  $I_{QL}$  is 75 mA at 1.65V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than  $50\Omega$ , the current requirements are less and switching is still quaranteed.

It is important to note that the typical 24 mA DC drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid  $V_{\mbox{\scriptsize IN}}$  level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

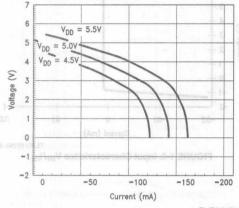


FIGURE 1-4a. Output Characteristics V<sub>OH</sub>/I<sub>OH</sub>, 'AC00

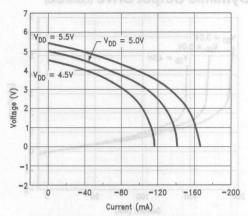


FIGURE 1-4b. Output Characteristics
VoH/IoH, 'ACTQ244

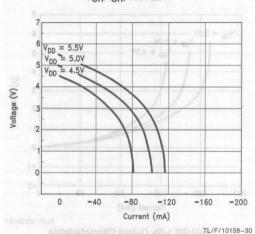


FIGURE 1-4c. Output Characteristics V<sub>OH</sub>/I<sub>OH</sub>, 'FCT244A

#### **Dynamic Output Drive (Continued)**

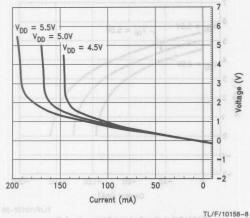


FIGURE 1-5a. Output Characteristics V<sub>OL</sub>/I<sub>OL</sub>, 'AC00

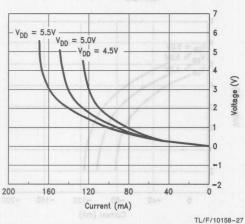


FIGURE 1-5b. Output Characteristics V<sub>OL</sub>/I<sub>OL</sub>, 'ACTQ244

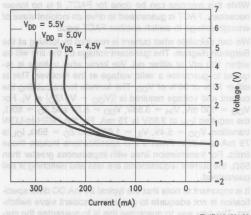


FIGURE 1-5c. Output Characteristics V<sub>OL</sub>/I<sub>OL</sub>, 'FCT244A

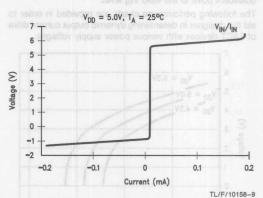


FIGURE 1-6. Input Characteristics V<sub>IN</sub>/I<sub>IN</sub>

#### **Choice of Voltage Specifications**

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3V  $\pm$ 0.3V. To this end, National Semiconductor guarantees all of its devices operational at 3.3V  $\pm$ 0.3V. Note also that AC and DC specifications are guaranteed between 3.0V and 5.5V. Operation of FACT logic is also guaranteed from 2.0V to 6.0V 'AC/'ACQ on V\_DD.

#### **Operating Voltage Ranges**

FACT = 2.0V to 6.0V ('AC/'ACQ)

FACT = 5.0V ±10% ('ACT/'ACTQ)

FACT = 5.0V ±5% ('FCT/'FCTA)

ALS = 5.0V ±10%

LS = 5.0V ±5%

HC = 2.0V to 6.0V

#### **FACT Replaces Existing Logic**

National Semiconductor's Advanced CMOS family is specifically designed to outperform existing CMOS and Bipolar logic families. *Figure 1-7* shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1  $\mu$ W of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

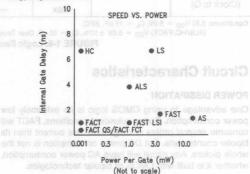


FIGURE 1-7. Internal Gate Delays

#### General Characteristics (All Max Ratings)

| Symbol                   | Characteristics                                      | ALS                     | нсмоѕ                        | at (Note: In many data:TSAT log. Algo, logr. and V |                             |                         |      |
|--------------------------|--|-------------------------|------------------------------|--|-----------------------------|-------------------------|------|
| Symbol                   | Characteristics                                      | (/ALS/TO                | OS HOMOS                     | 'AC/'ACQ   | 'ACT/'ACTQ                  | 'FCT/'FCTA              | Unit |
| V <sub>CC/EE/DD</sub>    | Operating Voltage Range                              | 5 ±10%                  | 5 ± 10%                      | 5 ±5%  | 5 ± 10%                     | 5 ±5%                   | V    |
| T <sub>A</sub> 74 Series | Operating Temperature Range                          | 0 to +70<br>-55 to +125 | -40 to +85<br>-55 to +125    | -40 to +85<br>-55 to +125                          | -40 to +85<br>-55 to +125   | 0 to +70<br>-55 to +125 | °C   |
| V <sub>IH</sub> (Min)    | Input Voltage  | 2.0                     | 3.15                         | 3.85   | 2.0                         | 2.0                     | ٧    |
| V <sub>IL</sub> (Max)    | (Limits) qui in 101 eloyo                            | DH 8.0 DU               | 0.9                          | a sint 1.65 lioson                                 | lemet 0.8                   | ab bn 0.8               | V    |
| V <sub>OH</sub> (Min)    | Output Voltage                                       | 2.7                     | V <sub>DD</sub> - 0.1        | V <sub>DD</sub> - 0.1                              | V <sub>DD</sub> - 0.1       | V <sub>DD</sub> - 0.2   | V    |
| V <sub>OL</sub> (Max)    | (Limits) to MJH) tis9 notice                         | 161T 0.5                | 0.1                          | 0.1  | 0.1                         | 0.2                     | ٧    |
| IH Genive                | Input Current  | 20                      | +1.0                         | +1.0   | +1.0                        | +5.0                    | μΑ   |
| I <sub>IL</sub>          | t Frequency  | -200 M                  | -1.0                         | -1.0   | -1.0 sqisel0                | -5.0                    | μΑ   |
| Гон                      | Output Current                                       | -0.4                    | −4.0 @ V <sub>DD</sub> − 0.8 | -24 @ V <sub>DD</sub> - 0.8                        | -24 @ V <sub>DD</sub> - 0.8 | -15 mA @ 2.4V           | mA   |
| loL                      | at V <sub>0</sub> (Limit)                            | 8.0                     | 4.0 @ 0.4V                   | 24 @ 0.44V   | 24 @ 0.44V                  | 64 mA @ 0.5V            | mA   |
| DCM nso ell              | DC Noise Margin<br>LOW/HIGH (V <sub>DD</sub> = 4.5V) | 0.4/0.7                 | 0.8/1.25                     | 1.25/1.25  | 0.7/2.4                     | 0.6/2.3                 | V    |

Note: All DC parameters are specified over the commercial temperature range.

#### Speed/Power Characteristics (All Typical Ratings)

| Symbol           | Characteristics               | ALS | HCMOS  | FACT AC | FACT FCTA | Units |
|------------------|-------------------------------|-----|--------|---------|-----------|-------|
| IG               | Quiescent Supply Current/Gate | 0.2 | 0.0005 | 0.0005  | 0.0005    | w mA  |
| PG               | Power/Gate (Quiescent)        | 1.2 | 0.0025 | 0.0025  | 0.0025    | mW    |
| t <sub>Pd</sub>  | Propagation Delay ('244 Typ.) | 7.0 | 14.0   | 5.0     | 3.0       | ns    |
|                  | Speed Power Product           | 8.4 | 0.04   | 0.01    | 0.008     | рЈ    |
| f <sub>max</sub> | Clock Frequency D/FF          | 50  | 50     | 160     | 225       | MHz   |

FIGURE 1-8. Logic Family Comparisons

| י פיניבורי ירחביים                 | VIDENT STANDING VI    | - Swally Barney St. On IV.V |           | -muro.0 07 8t | 0.U 18 8314 | ph beiD.Uathi to | anois ns mib |  |
|------------------------------------|-----------------------|-----------------------------|-----------|---------------|-------------|------------------|--------------|--|
| nance, FACT ex                     | paed/power perform    | Max                         | ous logic | 11.0          | 23.0        | 8.5              | ns red       |  |
| t <sub>PLH</sub> /t <sub>PHL</sub> | 74XX74                | Тур                         | 30.0      | 12.0          | 12.0        | 8.0 yd ba        | bloob nsw fi |  |
| (Clock to Q)                       | sparisons table below | Max                         | The Logi  | 18.0          | 44.0        | 10.5             | ns ns        |  |
| t <sub>PLH</sub> /t <sub>PHL</sub> | 74XX163               | Тур                         | 27.0      | 10.0          | 20.0 s s s  | 1 10.5.0 10.0    | tenoinsago   |  |
| (Clock to Q)                       | grawno av graga       | Max                         | _         | 20.0          | 52.0        | 10.0             | ns           |  |

Conditions: (LS)  $V_{DD} = 5.0V$ ,  $C_L = 15 pF$ ,  $25^{\circ}C$ ;

(ALS/HC/FACT) VDD = 5.0V ±10%, CL = 50 pF, Over Temp, Max values at 0°C to +70°C for ALS, -40°C to +85°C for HC/FACT.

FIGURE 1-8. Logic Family Comparisons (Continued)

#### Circuit Characteristics

#### POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of FACT device under AC conditions is a function of three basic sources, guiescent power, internal dynamic power, and output dynamic power dissipation. Firstly, a FACT device will dissipate power in the quiescent or static condition. This can be calculated by using the formula: (Note: In many datasheets IDD, ΔIDD, IDDT, and VDD are referred to as ICC, AICC, ICCT, and VCC, respectively. There are no differences.)

Eq. 1 PDQ = IDD • VDD

PDO = Quiescent Power Dissipation

IDD = Quiescent Power Supply Current Drain V<sub>DD</sub> = Power Supply Voltage

Secondly, a FACT device will dissipate power dynamically by charging and discharging internal capacitance. This can

be calculated by using one of the following two formulas: Eq. 2A (AC/ACQ)

PDINT = (CPD • VS • f) • VDD

PDINT = Internal Dynamic Power

Dissipation

Am VAS CPD = Device Power Dissipation

Capacitance

Va V<sub>S</sub> = Output Voltage Swing

= Internal Frequency of Operation

V<sub>DD</sub> = Power Supply Voltage

Cpn values are specified for each FACT device and are measured per JEDEC standards as described later on in Section 2. On FACT device data sheets, CPD is a typical value and is given either for the package or for the individual stages with the device. (See Section 2). For FACT devices, VS and VDD are the same value and can be replaced by V<sub>DD</sub><sup>2</sup> in the above formula.

Eg. 2B (ACT/ACTQ)

 $PD_{INT} = [(I_{DDT} \bullet D_{H} \bullet N_{T}) \bullet V_{DD}] +$ [ (CPD • Vs • f) • VDD]

PDINT = Internal Dynamic Power Dissipation

IDDT = Power Supply Current for a TTL HIGH

Input  $(V_{IN} = 3.4V)$ 

DH = Duty Cycle for TTL Inputs HIGH NT = Number of TTL Inputs at DH

V<sub>DD</sub> = Power Supply Voltage

= Device Power Dissipation Capacitance CPD

= Output Voltage Swing

= Internal Frequency of Operation

Eq. 2C (FCT/FCTA)

 $PD_{INT} = [(\Delta I_{DD} \bullet D_{H} \bullet N_{T}) \bullet V_{DD}] + [(I_{DD} \bullet \{f_{CP}/2\})]$ + fIN · NIN ) · VDD] ONBARGO GOVERNOO

PDINT = Internal Dynamic Power Dissipation V<sub>DD</sub> = Power Supply Voltage

ΔI<sub>DD</sub> = Power Supply Current for a TTL HIGH Input  $(V_{IN} = 3.4V)$ 

DH = Duty Cycle for TTL Inputs HIGH

= Number of TTL Inputs at DH NT

I<sub>DDD</sub> = Dynamic Current Caused by an Input

Transition Pair (HLM or LHL)

= Clock Frequency for Registered Devices (Zero for Non-Registered Devices)

f<sub>IN</sub> = Input Frequency

N<sub>IN</sub> = Number of Inputs at f<sub>IN</sub>

See Section 3 for more information on IDDT or AIDD. Thirdly, a FACT device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Eq. 3 PDOUT = (CL • VS • f) • VDD

PD<sub>OUT</sub> = Output Power Dissipation

C<sub>L</sub> = Load Capacitance = Output Voltage Swing

= Output Operating Frequency

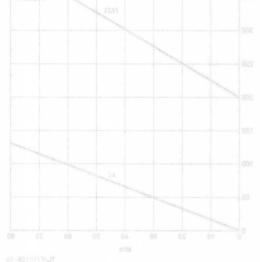
V<sub>DD</sub> = Power Supply Voltage

Eq. 5 
$$PD_{TOTAL} = PD_Q + PD_{DYNAMIC}$$
 or  $PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$ 

The following is an exercise in calculating total dynamic Ind for the FACT Advanced CMOS family. The device used as an example is the ACTQ374. Static IDD, IDDT and CPD numbers can be found in the ACTQ374 data sheet. Inc numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worstcase calculations.

The following assumptions have been made:

- 1. IDD will be calculated per input/output (as per JEDEC CPD calculations). The total for the ACTQ374 will be the calculated Inn × 8.
- 2. Worst case conditions and JEDEC would require that the data is being toggled at the clock frequency in order to change the outputs at the maximum rate (1/2 CP).
- 3. The data and clock input signals are derived from TTL level drivers (0V to 3.0V swing) at 50% duty cycle.
- 4. The clock frequency is 16 MHz.
- 5.  $I_{DD}$  will be calculated for  $C_{L} = 50$  pF, 100 pF and 150 pF.
- 6.  $V_{DD} = 5V$ .
- 7. Total POWER dissipation can be obtained by multiplying total IDD by VDD (5.0V).
- 8. Quiescent IDD will be neglected in the total IDD calculation because it is 1000 times less than dynamic IDD.
- 9. There is no DC load on the outputs, i.e. outputs are either unterminated or terminated with series or AC shunt termi-



(IDDT) × (number of TTL inputs) × (Duty ITIPUL IDD Cycle)

 $= (1.5 \times 10^{-3}) \times (1) \times (0.50)$ 

= 0.75 mA per input being toggled at TTL lev-

Internal IDD = (VSWING) × (CPD) × (CP freq)

 $= (5.0) \times (42 \times 10^{-12}) \times (16 \times 10^{+6})$ 

= 3.36 per mA per input being toggled by CP

Output  $I_{DD} = (V_{SWING} \times (C_I) \times (Q \text{ freq})$ 

a)  $C_1 = 50 pF$ 

 $= (5.0) \times (50 \times 10^{-12}) \times (8 \times 10^{+6})$ 

= 2 mA per output toggled at 1/2 CP

b)  $C_L = 100 pF$ 

 $= (5.0) \times (100 \times 10^{-12}) \times (8 \times 10^{+6})$ 

= 4 mA per output toggled at 1/2 CP

c)  $C_1 = 150 pF$ 

 $= (5.0) \times (150 \times 10^{-12}) \times (8 \times 10^{+6})$ 

= 8 mA per output toggled at 1/2 CP

Adding Input, Internal and Output IDD together and multiplying by 8 I/O per ACTQ374, the approximate worst-case IDD calculations are as follows:

 $C_L = 50 \, pF \, I_{DD} \, total = 48.9 \, mA \, or \, 244.5 \, mW^* \, at \, CP$ 

0 15W09 8-1 3RU019 = 16 MHz

 $C_L = 100 \, pF$   $I_{DD} \, total = 64.9 \, mA \, or 324.5 \, mW^* \, at \, CP$ 

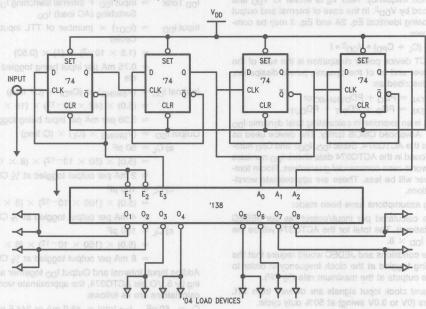
= 16 MHz

IDD total = 96.9 mA or 484.5 mW\* at CP  $C_{I} = 150 pF$ 

= 16 MHz

(\*Power is obtained by multiplying I<sub>DD</sub> by V<sub>DD</sub>)

#### Circuit Characteristics (Continued)



#### 81 = FIGURE 1-9. Power Demonstration Circuit Schematic

TL/F/10158-11

The circuit shown in *Figure 1-9* was used to compare the power consumption of FACT versus FAST devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a '138 decoder. This generated eight non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. Figure 1-10 illustrates the results of these measurements.

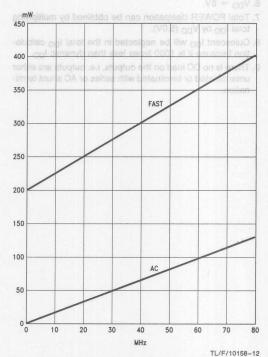


FIGURE 1-10. FACT vs FAST Circuit Power

#### Circuit Characteristics (Continued)

The FACT circuit dissipates much less power than the FAST version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the FAST circuit continued to dissipate 200 mW

#### SPECIFICATION DERIVATION

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 1-11a through 1-11i illustrate how the data from the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'XX244.

Figure 1-11a shows the data taken (from one part) on a typical, single path,  $t_{\rm PHL}$ , over temperature at 5.0V; there is negligible variation in the value of  $t_{\rm PHL}$ . The next set of graphs, Figure 1-11b through 1-11d, depict data taken on the same device; these sets of curves represents the data on all paths. The data on this plot indicates only a small variation for  $t_{\rm PHL}$ .

The graphs in *Figures 1-11a-d* include data at 5.0V; *Figure 1-11e* shows the variation of delay times over the standard  $5.0V \pm 0.5V$  voltage range. Note there is only a  $\pm 6\%$  variation in delay time due to voltage effects.

Now refer to Figure 1-11f which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ±3 standard deviations, this guarantees an increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guard-bands are incorporated.

With voltage and process effects added (Figures 1-11g, 1-11h, and 1-11i), the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

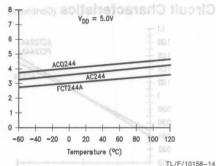
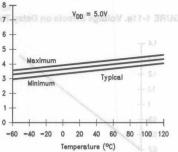
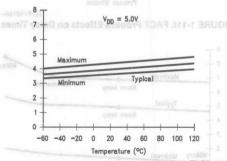


FIGURE 1-11a. tpHL Single Path



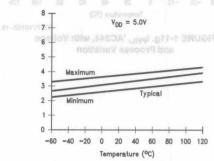
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FIGURE 1-11b. tpHL, 'AC244, All Paths



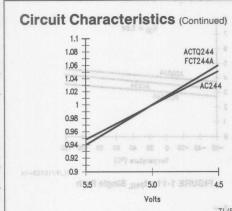
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FIGURE 1-11c. tpHL, 'ACQ244, All Paths



TL/F/10158-32

FIGURE 1-11d. t<sub>PHL</sub>, 'FCT244A, All Paths



TL/F/10158-16
FIGURE 1-11e. Voltage Effects on Delay Times

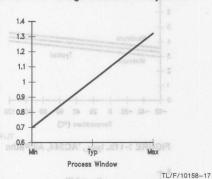


FIGURE 1-11f. FACT Process Effects on Delay Times

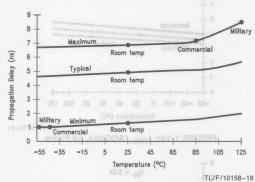
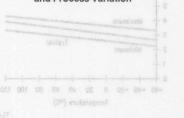


FIGURE 1-11g. t<sub>PHL</sub>, 'AC244, with Voltage and Process Variation



PIGURE 1-11d, total, 'PC7244A, All Paths

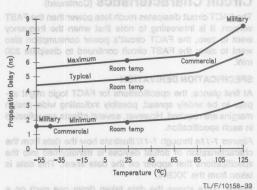


FIGURE 1-11h. tpHL, 'ACQ244, with Voltage and Process Variation

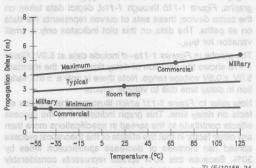


FIGURE 1-11i. t<sub>PHL</sub>, 'FCT244A, with Voltage and Process Variation

ands are incorporated.

With voltage and process effects added (Figures 1-11g, 11h, and 1-11h, the full range of the specification can be sen. For reference, the data sheet values are shown on a graph.

It CMOS. Although the graphs are drawn for a specific decide, other part types have very similar graphical representation, other part types have very similar graphical representations. Therefore, for performance-critical applications, there are can narrow the specifications. For example, need, the user can narrow the specifications. For example, it puts in a critically timed subcircuit are together on a card, so it may be assumed the devices are at the same upply and temperature.

#### Circuit Characteristics (Continued)

The same reasoning can be applied to setup and hold times. Consider the 'AC74. The setup time is 3.0 ns while the hold time is 0.5 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5.0V, the setup time is 1.0 ns while the hold time is -1.5 ns. They are virtually the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true "critical" time where the input is actually sampled is extremely short: less than 50 ps. By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (2.5 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

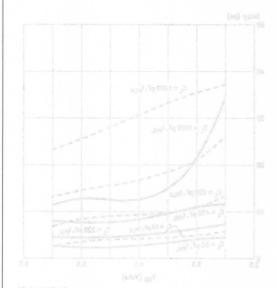
#### **CAPACITIVE LOADING EFFECTS**

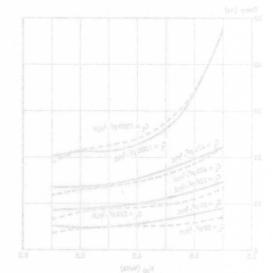
In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delay are measured to the 50% point of the output waveform.

| D                | anamatari = 0 | V   | Units |     |       |
|------------------|---------------|-----|-------|-----|-------|
| Parameter        |               | 3.0 | 4.5   | 5.5 | Units |
| tplH             | FACT AC       | 31  | 22    | 19  |       |
|                  | FACT QS       | 34  | 19    | 19  | ps/pF |
|                  | FACT FCTA     | 45  | 29    | 27  |       |
| tpHL             | FACT AC       | 18  | 13    | 13  |       |
| easy or a second | FACT QS       | 32  | 22    | 20  | ps/pF |
|                  | FACT FCTA     | 17  | 13    | 12  |       |

TA = 25°C

Figures 1-12 and 1-13, describe propagation delays on FACT devices as affected by variations in power supply voltage ( $V_{\rm DD}$ ) and lumped load capacitance ( $C_{\rm L}$ ). Figures 1-14 and 1-15 show the effects of lumped load capacitance on rise and fall times for FACT devices.





1,000 Telestration Dalay vs Vee (ACTO244)

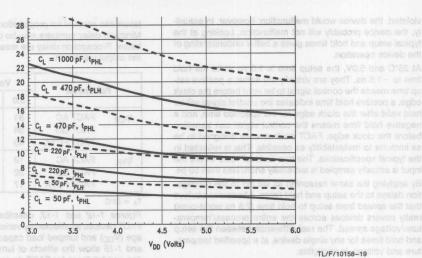


FIGURE 1-12a. Propagation Delay vs V<sub>DD</sub> ('AC00)

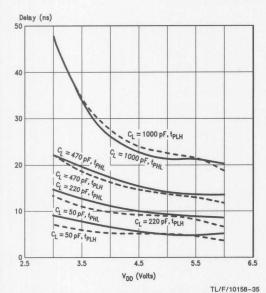


FIGURE 1-12b. Propagation Delay vs V<sub>DD</sub> ('ACTQ244)

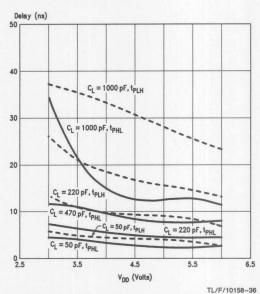


FIGURE 1-12c. Propagation Delay vs V<sub>DD</sub> ('FCT244A)

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#### Circuit Characteristics (Continued)

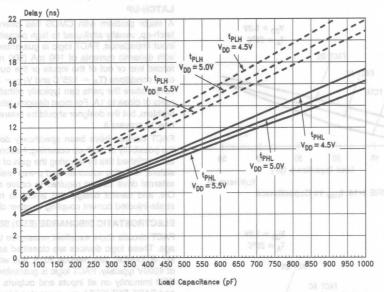
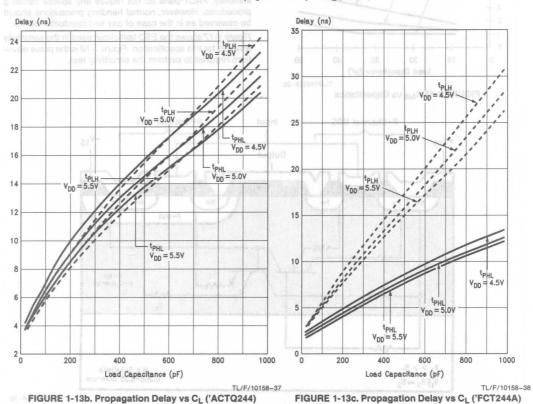


FIGURE 1-13a. Propagation Delay vs C<sub>L</sub> ('AC00)



1-17

#### Circuit Characteristics (Continued)

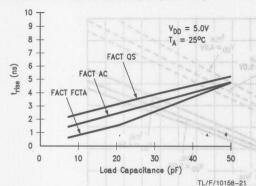


FIGURE 1-14. trise vs Capacitance

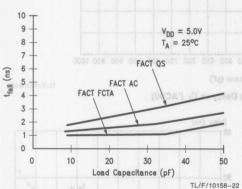


FIGURE 1-15. t<sub>fall</sub> vs Capacitance

#### LATCH-UP

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA (300 mA for FACT QS) forced into or out of the inputs or the outputs under worst case conditions ( $T_A=125^{\circ}C$  and  $V_{DD}=5.5\ V_{DC}$ ). At room temperature the parts can typically withstand dynamic currents of close to 1A. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

FACT devices have been specifically designed to reduce the possibility of latch-up occurring; National Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

#### **ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY**

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category "B" of MIL-STD-883C, test method 3015, and withstand in excess of 4000V typically. FACT logic is guaranteed to have 2000V ESD immunity on all inputs and outputs. Some FACT QS and FACT FCT/FCTA are guaranteed to have 4000V ESD immunity. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 1-17 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 1-18 is the pulse waveform required to perform the sensitivity test.

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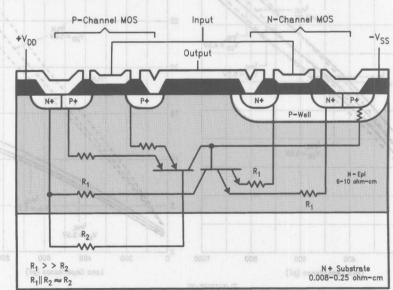


FIGURE 1-16. FACT EPI Process Cross Section with Latch-up Circuit Model

#### Circuit Characteristics (Continued)

The test procedure is as follows; five pulses, each of at least 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MILSTD-883C, TM-3015. Devices that result in ESD immunity in

the 2000V-3999V range are listed as ESD Class 2. Devices that result in ESD immunity in the 4000+V range are listed as ESD Class 3. Several devices on the FACT QS and FACT FCT/FCTA lines are guaranteed as Class 3 (see individual data sheets).

For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

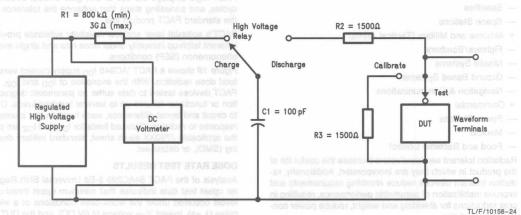


FIGURE 1-17, ESD Test Circuit

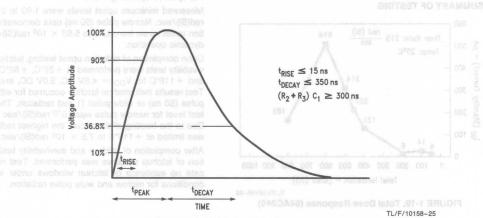


FIGURE 1-18. ESD Pulse Waveform

#### Circuit Characteristics (Continued)

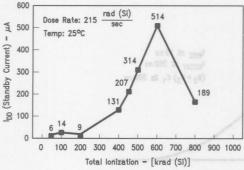
#### **RADIATION TOLERANCE**

Semiconductors subjected to radiation environments undergo degradation in operating life as their exposure to radiation increases. As technology advances, so does the demand for radiation-tolerant devices. National is meeting this challenge by developing the FACT family into a comprehensive radiation tolerant product for present and future radhard needs. Such applications include:

- Space (Commercial and Military)
- Satellites
- Space Stations
- · Airborne and Military (Tactical Arena)
- Fighters/Bombers
- Missile Systems
- Ground Based Systems
- Navigation & Communications
- Commercial
- Power Stations
- Medical
- Food and Bacterial Control

Radiation tolerant semiconductors increase the useful life of the product in which they are incorporated. Additionally, radiation tolerant devices reduce shielding requirements and improve stabilization of parametric performance, resulting in cost reductions for shielding and weight, reduce power consumption and size.

#### **SUMMARY OF TESTING**



TL/F/10158-26

FIGURE 1-19. Total Dose Response (54AC245)

Total dose irradiation is presently performed "in-house" using a AECL Gamma Cell 220, Cobalt-60, source (National Bureau of Standards certified). Step-stress radiation testing is performed on each part-type per MIL STD 883 Method 1019.3. After each total dose level, a complete parametric test (DC and AC) is done and the parametric values evaluated.

#### FACT IS RADIATION TOLERANT

FACT logic employs the use of thin gate oxides, oxidation cycles, and annealing steps that enhance the tolerance of the standard FACT product line.

FACT's epitaxial layer and low-resistivity substrate provide inherent latch-up immunity under dose rate and single event phenomenon (SEP) conditions.

Figure 19 shows a FACT 'AC245 I<sub>DD</sub> supply current versus total dose radiation. With the exception of I<sub>DD</sub> and I<sub>OZ</sub>, all FACT devices tested to date suffer no parametric degradation or functional failures up to several hundred krads. Due to circuit and layout differences, each function has a unique response to radiation. Relaxed limits for I<sub>DD</sub> and I<sub>OZ</sub> are per the applicable /750XX slash sheet, standard military drawing (SMD), or datasheet.

#### DOSE RATE TEST RESULTS

Analysis of the FACT 54AC299 8-Bit Universal Shift Register upset test data indicates that minimum upset threshold levels occurred under the worst-case conditions of a wide pulse (1  $\mu$ s), lowest V<sub>DD</sub> voltage (4.0V DC), and the DUT in the dynamic operating mode.

Measured minimum upset levels were 1.90 to 2.22  $\times$   $10^9$  rad(Si)/sec. Narrow pulse (50 ns) data demonstrated radiation upset levels from 4.40 to 5.66  $\times$   $10^9$  rad(Si)/sec under dynamic operation.

Upon completion of radiation upset testing, latchup and survivability tests were performed at  $+25^{\circ}\mathrm{C}, +80^{\circ}\mathrm{C}, +100^{\circ}\mathrm{C},$  and  $+116^{\circ}\mathrm{C}$  for  $V_{DD}=4.5V$  DC, 5.0V DC, and 5.5V DC. Test results indicated no latchup occurred for either narrow pulse (50 ns) or wide pulse (1 ms) radiation. The radiation test level for narrow pulse was  $10^{10}$  rad(Si)/sec at  $+25^{\circ}\mathrm{C}.$  Due to the heating of the circuit, the highest radiation level was limited at  $+116^{\circ}\mathrm{C}$  to  $7.5\times10^{9}$  rad(Si)/sec.

After completion of latchup and survivability tests, verification of latchup windows was performed. Test results indicate no existence of latchup windows under worst case conditions for narrow and wide pulse radiation.



Section 2

Ratings, Specifications, and Waveforms



## **Section 2 Contents**

| Introduction  | 2-3 |
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| Power Dissipation—Test Philosophy                         | -   |
| AC Loading and Waveforms                                  |     |
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| Rise and Fall Times                                       | 2-5 |
| Propagation Delays, f <sub>max</sub> , Set and Hold Times |     |
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2-2



## Ratings, Specifications, and Waveforms

### Specifying FACT<sup>TM</sup> Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. National Semiconductor realized and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specs, National Semiconductor devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits. With more than five years of experience manufacturing FACT logic, National Semiconductor can accurately predict how these wafer lots compare with the best and worse case lots that can possibly be expected.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

## Power Dissipation—Test Philosophy

In an effort to reduce confusion about measuring power dissipation capacitance, C<sub>PD</sub>, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison.

The following is a list of different types of logic functions, along with the input setup conditions under which the C<sub>PD</sub> was measured for each type of device. By understanding how the device was exercised during C<sub>PD</sub> measurements, the designer can understand whether the C<sub>PD</sub> specified for that particular device reflects the total power dissipation ca-

pacitance for either the entire device or for just a certain stage of that device. For example, from the following list, it is apparent that the C<sub>PD</sub> value specified for a counter reflects the internal capacitance for the entire device, since the entire device is being exercised during measurement. On the other hand, the C<sub>PD</sub> value specified for an octal line driver reflects the internal capacitance for only one of eight stages, since only one input was being switched during test. Therefore the octal's overall power dissipation should be calculated for each of the eight stages, individually.

During the  $C_{PD}$  measurements, each output that is being switched should be loaded with the standard 50 pF and  $500\Omega$  load. All device measurements are made with  $V_{DD}=5.0V$  at  $25^{\circ}C$ , with TRI-STATE® outputs enabled.

Gates/Buffers/ Line Drivers: Latches: Switch one input. Bias the remaining inputs such that one output switches. Switch the Enable and D inputs such

that the latch toggles.

Flip-Flops:

Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.

Decoders: Switch one address pin which changes two outputs.

Multiplexers: Switch

Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.

Counters:

Switch the clock pin with other inputs biased such that the device counts.

Shift Registers:

Switch the clock pin with other inputs biased such that the device shifts.

Transceivers:

Switch one data input. For bidirectional devices enable only one direction.

Parity Generator: Priority Encoders: Switch one input.
Switch the lowest priority input.

## **AC Loading and Waveforms**

#### LOADING CIRCUIT

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices ('AC and 'ACT) unless otherwise specified in the data sheet of a specific device.

omunity

#### AC Loading and Waveforms (Continued)

The use of this load, which is equivalent to the FAST® (Fairchild Advanced Schottky TTL) test jig, differs somewhat from previous (HCMOS) practice. This provides more meaninaful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance, allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the inloading to be expected in avarage applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The  $500\Omega$  resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the  $500\Omega$  resistor to ground can simply be a  $450\Omega$  resistor feeding into a  $50\Omega$  coaxial cable leading to a sampling scope input connector, with the internal  $50\Omega$  termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See Figure 1.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a  $50\Omega$  termination for the pulse generator that supplies the input signal.

Shown in Figure 1 is a second  $500\Omega$  resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/

TEST LOAD DUT  $\begin{array}{c}
t_{\text{PLH}} \\
t_{\text{PHL}} \\
t_{\text{PHZ}} \\
t_{\text{FLZ}}
\end{array}$   $\begin{array}{c}
t_{\text{PLS}} \\
t_{\text{PLZ}} \\
t_{\text{FLZ}}
\end{array}$   $\begin{array}{c}
t_{\text{PLZ}} \\
t_{\text{PLZ}}
\end{array}$ 

FIGURE 1a. AC Loading Circuit for AC, ACT, ACQ, ACTQ

Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of  $500\Omega$  resistors and the 2  $\times$  V<sub>DD</sub> supply voltage establish a quiescent HIGH level.

#### **Test Conditions**

Figures 2a and 2b describe the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring  $V_{\rm IN}$  to range from 0V for a logic LOW to 3.0V for a logic HIGH for 'ACT devices and 0V to  $V_{\rm DD}$  for 'AC devices. The DC parameters are normally tested with  $V_{\rm IN}$  at guaranteed input levels, that is  $V_{\rm IH}$  to  $V_{\rm IL}$  (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system

Noise immunity testing is performed by raising  $V_{IN}$  to the nominal supply voltage of 5.0V then dropping to a level corresponding to  $V_{IH}$  characteristics, and then raising again to the 5.0V level. Noise tests can also be performed on the  $V_{IL}$  characteristics by raising  $V_{IN}$  from 0V to  $V_{IL}$ , then returning to 0V. Both  $V_{IH}$  and  $V_{IL}$  noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output wave-

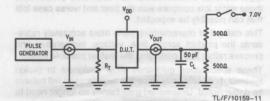


FIGURE 1b. AC Loading Circuit for FCT, FCTA

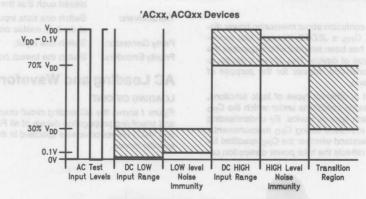
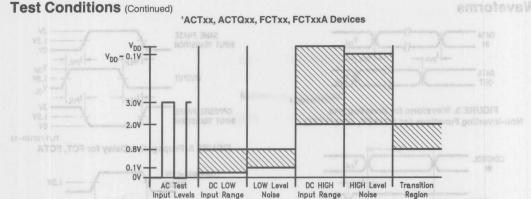


FIGURE 2a. Test Input Signal Levels

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Immunity
FIGURE 2b. Test Input Signal Levels

form transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V<sub>DD</sub> bypass capacitor should be provided at the test socket, also with minimum lead lengths.

#### **Rise and Fall Times**

Input signals should have rise and fall times of 3.0 ns and signal swing of 0V to 3.0V  $V_{DD}$  for 'ACT devices or 0V to  $V_{DD}$  for 'AC devices. Rise and fall times less than or equal to 1 ns should be used for testing  $f_{max}$  or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2–3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the VDD or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it recrosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have  $V_{\rm DD}$  and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5V swing on the output.

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### Propagation Delays, f<sub>max</sub>, Set and Hold Times

Immunity

A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f<sub>max</sub>. A 50% duty cycle should always be used when testing f<sub>max</sub>. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc. See *Figures 3, 4*, and *8*.

#### **Enable and Disable Times**

Figures 5, 6 and 11 show that the disable times are measured at the point where the output voltage has risen or fallen by 0.3V from VOL or VOH, respectively. This change enhances the repeatability of measurements, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 0.3V of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 0.3V is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable times and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled. Note that the measurement points have been changed from the previous 10% and 90% points. This better reflects actual test points and does not change specification limits.



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FIGURE 3. Waveform for Inverting and Non-Inverting Functions for AC/ACT, ACQ/ACTQ

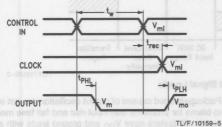


FIGURE 4. Propagation Delay, Pulse Width and trec Waveforms for AC/ACT, ACQ/ACTQ

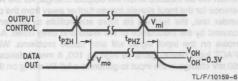


FIGURE 5. TRI-STATE Output High Enable and Disable Times for AC/ACT, ACQ/ACTQ

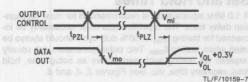
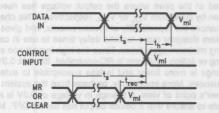


FIGURE 6. TRI-STATE Output Low Enable and Disable Times for AC/ACT, ACQ/ACTQ



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## FIGURE 7. Setup Time, Hold Time and Recovery Time for AC/ACT, ACQ/ACTQ

\*V<sub>mi</sub> = 50% V<sub>DD</sub> for 'AC/'ACQ devices; 1.5V for 'ACT/'ACTQ devices V<sub>mo</sub> = 50% V<sub>DD</sub> for 'AC/'ACT, 'ACQ/'ACTQ devices

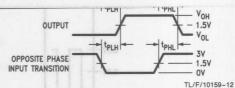


FIGURE 8. Propagation Delay for FCT, FCTA

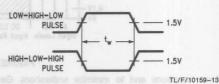


FIGURE 9. Pulse Width for FCT, FCTA

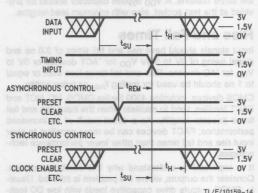
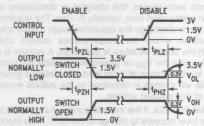


FIGURE 10. Set-Up, Hold and Release Times for FCT, FCTA



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#### FIGURE 11. Enable and Disable Times for FCT, FCTA

Note 1: Diagram shown for input Control Enable-LOW and input Control Disable-HIGH

Note 2: Pulse Generator for All Pulses: Rate  $\leq$  1.0 MHz; Z  $_0 \leq$  50  $\!\Omega$ ; t  $_F \leq$  2.5 ns; t  $_R \leq$  2.5 ns

come quicker, generating more induced vollage.

ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.

#### **FACT Noise Characteristics**

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

#### Equipment:

Hewlett Packard Model 8180A Word Generator PC-163A Test Fixture or Equivalent Tektronics Model 7854 Oscilloscope or Equivalent

#### Procedure:

- 1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
- 2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
- Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
- 4. Set V<sub>DD</sub> to 5.0V.
- Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
- Set the word generator input levels at 0V LOW and 3V HIGH for ACT/ACTQ/FCT/FCTA devices and 0V LOW and 5V HIGH for AC/ACQ devices. Verify levels with a digital volt meter.



#### FIGURE 12. Quiet Output Noise Voltage Waveforms

**Note A.**  $V_{OHV}$  and  $V_{OLP}$  are measured with respect to ground reference. **Note B.** Input pulses have the following characteristics: f=1 MHz,  $t_r=3$  ns,  $t_f=3$  ns, skew < 150 ps.

#### VOLP/VOLV and VOHP/VOHV:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V<sub>OLP</sub> and V<sub>OLV</sub> on the quiet output LOW during the HL transition. Measure V<sub>OHP</sub> and V<sub>OHV</sub> on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

#### VII D and VIHD:

- Monitor one of the switching outputs using a  $50\Omega$  coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V<sub>IL</sub>, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V<sub>IL</sub> limits, or on output HIGH levels that exceed V<sub>IH</sub> limits. The input LOW voltage level at which oscillation occurs is defined as V<sub>ILD</sub>.
- Next increase the input HIGH voltage level on the word generator, V<sub>IH</sub> until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V<sub>IL</sub> limits, or on output HIGH levels that exceed V<sub>IH</sub> limits. The input HIGH voltage level at which oscillation occurs is defined as V<sub>IHD</sub>.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

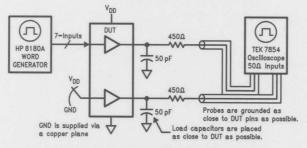


FIGURE 13. Simultaneous Switching Test Circuit

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## Electrostatic Discharge

Preceutions should be taken to prevent damage to devices by electrostatic discharge. Static charge lands to accumulate on insulated surfaces such as synthetic tabrics or carbeiting, plastic sinests, trays, form, tuben or bege, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere, in general, it is recommended that individuals take the preceution or loughing a known ground before handling devices. To affectively avoid that individuals wear a grounded what strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Snawre that all plassific parts of the testir, which are near the daylos, are considered and connected to ground.

#### FACT Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

#### dremglup

1ewlett Packard Model 8180A Word Generator 2G-183A Test Fixture or Equivalent

#### and the second

- 1. Verify Test Flature Loading: Standard Load 50 pF, 5000.
- 2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew unit all channels being used are within 150 ps. It is important to channels being used are within 150 ps. It is important to deskew the word generator channels before fusling. This will ensure that the outputs switch simultaneously.
- Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
  - L Set Vop to 5.0V.
- Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
- 5. Set the word generator input levels at 0V LOW and 3V HIGH for ACT/ACTO/FCTA devices and 0V LOW and 5V HIGH for AC/ACQ devices. Verify levels with a digital volt meter.



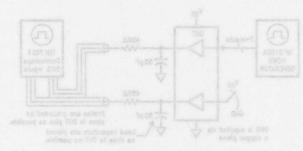
FIGURE 12. Quiet Quietral Noise Voltage Wareforms
Note A. Volty and Vogs are measured with respect to ground reterance.
Note B. Input pulses have the following characteristics: ( = 1 MHz, t, = 3 ns, user < 150 ps.

#### AOTE/AOTA surg AOHB/AOTA:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the eutput voltages using a 6011 oeasiel cable plugged into a standard MRB type connector on the test facture. Do not use an active FET orche.
- Messure Volp and Volly on the quiet output LOW during the HL transition. Measure Volp and Volly on the quiet output HIGH during the LH transition.
- Verify that the CND reference recorded on the oscilloscope has not drilled to ensure the accuracy and repeatability of the mensurements.

#### aud bas and

- Monitor one of the switching outputs using a 500 oceans cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level,  $V_{\parallel L}$  until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds  $V_{\parallel L}$  limits, or on output HIGH levels that exceed  $V_{\parallel L}$  limits. The input LOW voltage level at which oscillation occurs is defined LOW.
- Next increase the input HiGH voltage toyal on the word generator,  $V_{\rm HI}$  until the output begins to oscillate. Capillation is defined as notes on the output LOW level that exceeds  $V_{\rm HI}$  limits, or on output HIGH levels that exceed  $V_{\rm HI}$  limits. The input HIGH voltage level at which oscillation occurs is defined as  $V_{\rm HIG}$ .
- Verify that the GND reference recorded on the oscilloscope has not drilled to ensure the accuracy and repeatability of the mossurements.



ROURE 13, Simultaneous Switching Yest Circuit





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Design Considerations and Application Notes



## **Design Considerations**

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. National Semiconductor's advanced CMOS helps designers achieve these goals.

FACTTM (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a  $50\Omega$  transmission line drive capability (comparable to National Semiconductor's FAST bipolar technology family) to offer a complete family of 1.3-micron SSI, MSI, and LSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD, and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are six items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing—interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving—FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to system-generated problems.
- Board Layout—Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling—Maximize ground and V<sub>DD</sub> traces to keep V<sub>DD</sub>/ground impedance as low as possible; full ground/V<sub>DD</sub> planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.
- Electromagnetic Interference

## Interfacing

FACT and FACT QS devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink

24 mA of current under worst case conditions. FACT FCT is guaranteed to sink 64 mA and source 15 mA. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive FAST®, ALS, AS, LS, HC and HCT devices.

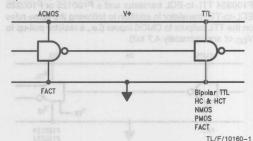


FIGURE 3-1. Interfacing FACT to NMOS, CMOS, and TTL

FACT devices can be directly driven by both NMOS and CMOS families, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1  $\mu$ A per input.

Some older technologies, including all existing TTL families, will not be able to drive FACT AC/ACQ circuits directly; this is due to inadequate output HIGH level capability, which is guaranteed to 2.4V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to  $V_{DD}$  of approximately 4.7  $k\Omega_{\rm h}$ , which is depicted in Figure 3-2. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.

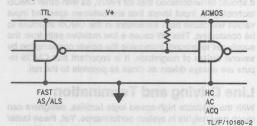
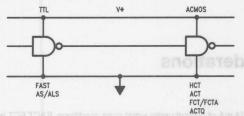


FIGURE 3-2. VIH Pull-Up on TTL Outputs

Unfortunately, there will be designs where including a pullup resistor will not be acceptable. In these cases, such as a terminated TTL bus, National Semiconductor has designed devices which offer thresholds that are TTL-compatible (Figure 3-3).

#### Interfacing (Continued)



TL/F/10160-3

#### FIGURE 3-3. TTL Interfacing to 'ACT

ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using a F100124 or F100324 TTL-to-ECL translator and a F100125 or F100325 ECL-to-TTL translator in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to  $V_{DD}$  of approximately 4.7 kΩ).

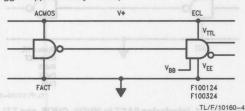


FIGURE 3-4a. FACT-to-ECL Translation

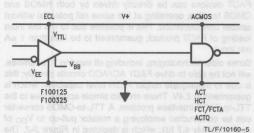


FIGURE 3-4b. ECL-to-FACT Translation

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

## **Line Driving and Termination**

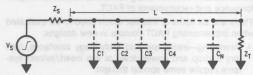
With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects. Although all circuit conductors have transmission line properties, these characteristics become more significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer:  $Z'_{0}$ , the effective equivalent impedance of the line, and  $t_{pde}$ , the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay,  $Z_{0}$  and  $t_{pd}$ , are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for  $Z'_{0}$  and  $t_{pde}$  can be calculated with:

$$Z'_{o} = \frac{Z_{o}}{\sqrt{1 + C_{D}/C_{L}}}$$
$$t_{pde} = t_{pd}\sqrt{1 + C_{D}/C_{L}}$$

where  $C_L=$  intrinsic line capacitance and  $C_D=$  additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; fone line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.



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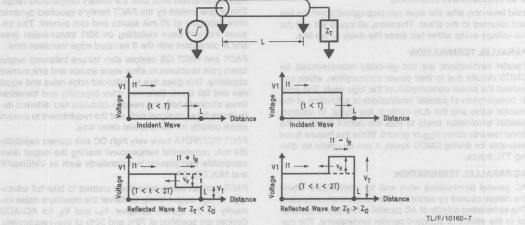
Length of Transmission Line = L  $\label{eq:length} \mbox{Distributed Load Capacitance per Unit Length} = \mbox{C}_D = \sum^{N} \mbox{C}_L/L$ 

Characteristic Impedance of a Transmission Line Altered by Distributed Loading  $= Z'_{O}$   $= \sqrt{\frac{L_{O}}{C_{O} + C}}$   $= \frac{Z_{O}}{\sqrt{1 + \frac{C_{D}}{C}}}$ 

Effective Reflection Coefficient at Termination =  $\rho = \frac{Z_T - Z'_C}{Z_T + Z'_C}$ 

FIGURE 3-5a. Transmission Line with Distributed Loading

## Line Driving and Termination (Continued)



- Length of Transmission Line = L
- Delay of Transmission Line = T
- Time of Sample = t seen 7 agest to Au 03 provints to prioritios
- Incident Wave Current = I<sub>1</sub>
- Incident Wave Voltage = V<sub>1</sub>
- Reflected Wave Current = I<sub>R</sub>
- Reflected Wave Voltage = V<sub>R</sub>
- Characteristic Impedance of Line = Z<sub>O</sub>
- Termination Impedance = Z<sub>T</sub>
- Voltage at Termination = V<sub>T</sub>

#### FIGURE 3-5b. Reflections Due to Impedance Mismatching

There are several termination schemes which may be used. Included are series, parallel, AC parallel, and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

#### **SERIES TERMINATIONS**

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line or especially for single point loads. Loads that are between the driver and the end of the line will receive a two-step waveform. The first step will be the incident wave, V<sub>i</sub>. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor, and the impedance of the line according to the formula

$$V_i = V_{DD} \cdot Z'_o/(Z'_o + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if  $R_S$  (the series resistor) plus the output impedance ( $Z_S$ ) of the driver is equal to the line impedance.  $Z_S$  for FACT is approximately  $17\Omega$ . The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a

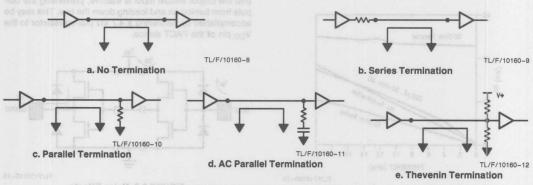


FIGURE 3-6a. Termination Schemes

## Line Driving and Termination (Continued)

valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

#### PARALLEL TERMINATION

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either  $V_{\rm DD}$  or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

#### **AC PARALLEL TERMINATION**

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The terminating effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

#### **Thevenin Termination**

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V<sub>DD</sub> or ground, increasing power consumption.

■ Parallel: Resistor =  $Z_0$ ■ Thevenin: Resistor =  $Z_0$ ■ Series: Resistor =  $Z_0$  -  $Z_0$ ■ AC: Resistor =  $Z_0$ Capacitor =  $Z_0$ 

Figure 3-6b. Suggested Termination Values

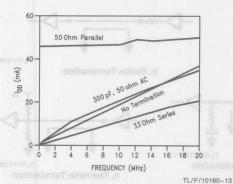


FIGURE 3-6c. FACT IDD vs Termination to a modern way and a structure

FACT circuits have been designed to drive  $50\Omega$  transmission lines over the full commercial temperature range and 75 $\Omega$  transmission lines over the military temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 75 mA source and sink current. This ensures incident wave switching on  $50\Omega$  transmission lines and is consistent with the 3 ns rated edge transition time.

FACT and FACT QS devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT FCT/FCTA have very high DC sink current capability (64 mA, commercial temperature) making the output drive compatible with popular bus standards such as VMEbus™ and MULTIBUS®.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer.  $V_{IH}$  and  $V_{IL}$  for AC/ACQ devices are specified at 70% and 30% of  $V_{DD}$  respectively. The corresponding output levels,  $V_{OH}$  and  $V_{OL}$ , are specified to be within 0.1V of the rails, of which the output is sourcing or sinking 50  $\mu A$  or less. These noise margins are outlined in Figure 3-7.



FIGURE 3-7. AC/ACQ Input Threshold

### **CMOS Bus Loading**

CMOS logic devices have clamp diodes from all inputs and outputs to  $V_{DD}$  and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 3-8 exemplifies the situation when power is removed. Any input driven above the V<sub>DD</sub> pin will forward-bias the clamp diode. Current can then flow into the device, and out V<sub>DD</sub> or any output that is HIGH. Depending upon the system, this current, I<sub>IN</sub>, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line. Another possible solution would be to ensure that the output enable input is inactive, preventing the outputs from turning on and loading down the bus. This may be accomplished by hardwiring a 4.7 kΩ pull-up resistor to the V<sub>DD</sub> pin of the FACT device.

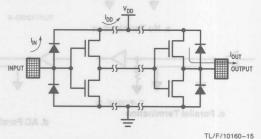


FIGURE 3-8. Noise Effects

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

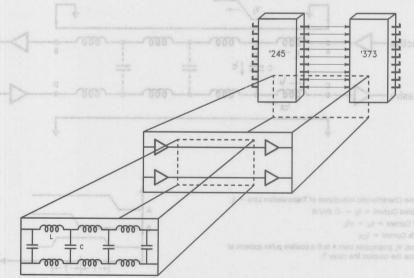
#### Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, *Figures 3-9b* and *3-9d*, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ( $\epsilon_{\rm F}=1.0$ ) and epoxy glass ( $\epsilon_{\rm F}=4.7$ ). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, *Figures 3-9c* and *3-9e*, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in Figures 3-10a through 3-10f, exemplify the outstanding immunity to everyday noise which can effect system reliability.



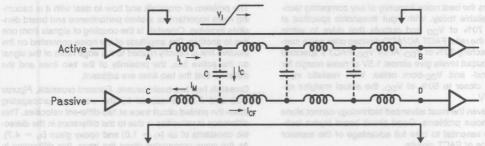
■ Two parallel signal lines provide mutual inductance and shunt capacitance

FIGURE 3-9a. Where Does Crosstalk Take Place?

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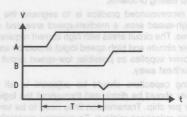
3

## Crosstalk (Continued)



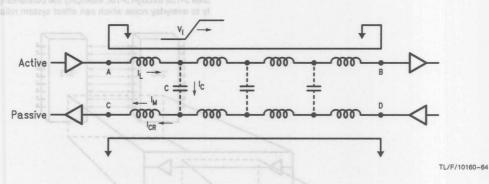
TL/F/10160-62

- Current through the Characteristic Inductance of Transmission Line = IL
- Capacitively Coupled Current = I<sub>C</sub> = -C dV<sub>i</sub>/dt
- Mutually Induced Current = I<sub>M</sub> = mI<sub>L</sub>
- Forward Crosstalk Current = I<sub>CF</sub>
- $\blacksquare$  As the active signal, V<sub>i</sub>, propagates from A to B a negative-going spike, V<sub>f</sub>, propagates from C to D, coincident with V<sub>i</sub>.

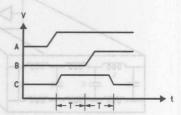


TL/F/10160-63

FIGURE 3-9b. Forward Crosstalk—Refresher

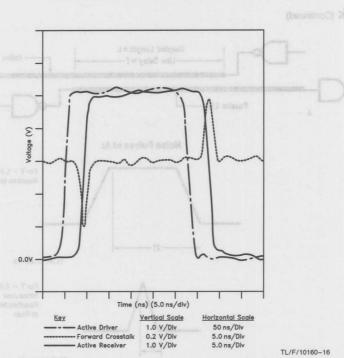


- Current through the Characteristic Inductance of Transmission Line = I<sub>L</sub>
- Capacitively Coupled Current = I<sub>C</sub> = -C dV<sub>i</sub>/dt
- $\blacksquare$  Mutually Induced Current  $= I_M = mI_L$
- Reverse Crosstalk Current = I<sub>CR</sub>
- $\blacksquare$  As the active signal,  $V_i$ , propagates from A to B a positive pulse appears at C for a duration twice the coupled line delay T.



TL/F/10160-65

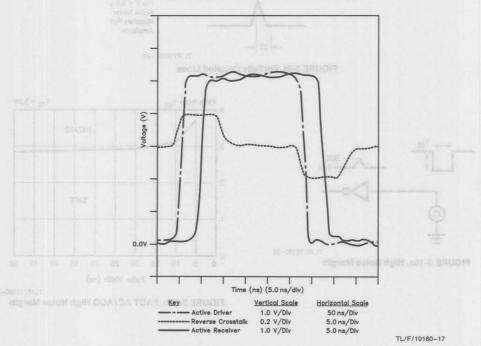
FIGURE 3-9c. Reverse Crosstalk—Refresher



Crosstalk (Continued)

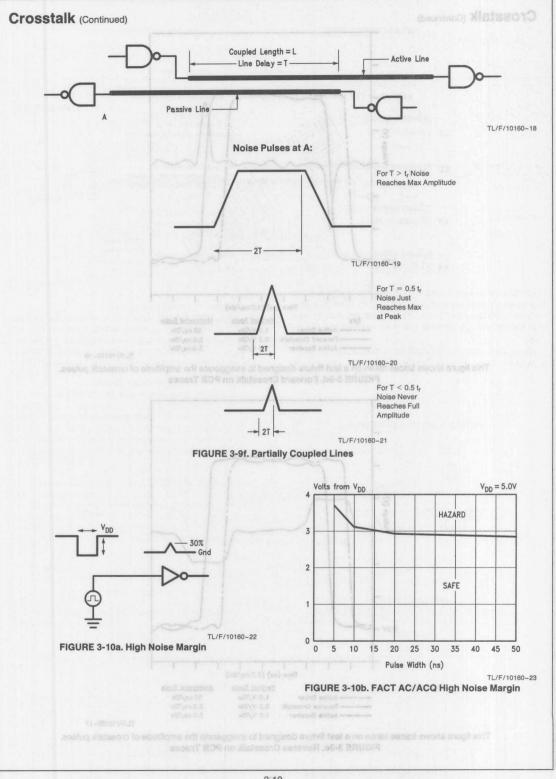
This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 3-9d. Forward Crosstalk on PCB Traces



This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

FIGURE 3-9e. Reverse Crosstalk on PCB Traces



## Crosstalk (Continued)

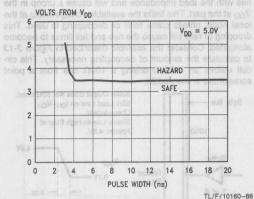
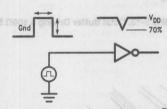


FIGURE 3-10c. FACT ACT/ACTQ/FCT/FCTA
High Noise Margin



TL/F/10160-24 FIGURE 3-10d. Low Noise Margin

With over 2.0V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of cross-

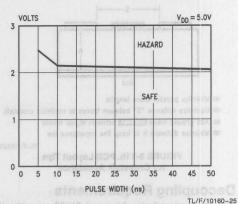
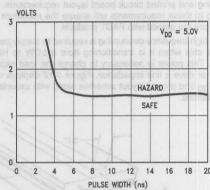


FIGURE 3-10e. FACT AC/ACQ Low Noise Margin



TL/F/10160-26

## FIGURE 3-10f. FACT ACT/ACTQ/FCT/FCTA Low Noise Margin

talk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

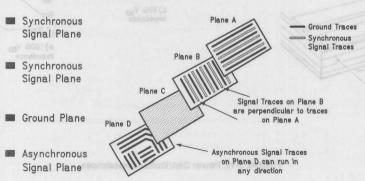
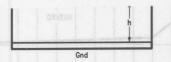


FIGURE 3-11a. Recommended Crosstalk—Avoidance Structure

TL/F/10160-27



- Minimize parallel trace lengths
- Maximize distance "S" between traces to minimize crosstalk
- Add ground trace between signal traces
- Minimize distance h to keep line impedance low

TL/F/10160-32

FIGURE 3-11b. PCB Layout Tips for Crosstalk Avoidance

## **Decoupling Requirements**

National Semiconductor Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. *Figure 3-12* displays various V<sub>DD</sub> and ground layout schemes along with associated impedances.

drooping of rails will cause the rise and fall times to become elongated. Consider the example described in *Figure 3-13* to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a  $100\Omega$  bus from a point somewhere in the middle.

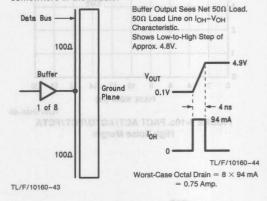
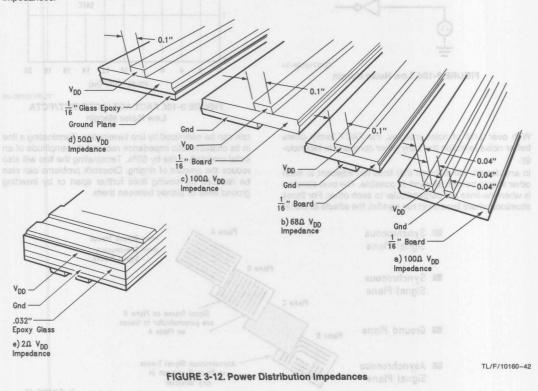
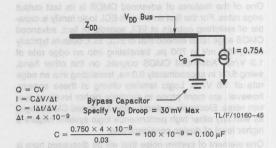


FIGURE 3-13. Octal Buffer Driving a 100 $\Omega$  Bus



Being in the middle of the bus, the driver will see two  $100\Omega$ loads in parallel, or an effective impedance of  $50\Omega$ . To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines. causing the actual VDD at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 3-14. In this example, if the VDD droop is to be kept below 30 mV and the edge rate equals 4 ns, a 0.10 µF capacitor is needed.

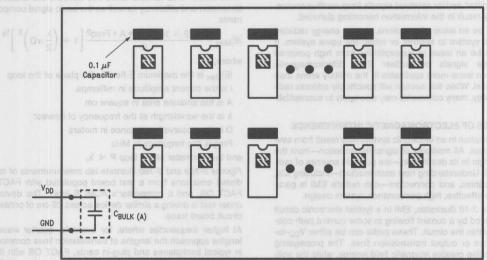
It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.



Select C<sub>B</sub> ≥ 0.10 µF FIGURE 3-14. Formula for Calculating **Decoupling Capacitors** 

### **Capacitor Types**

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50 μF-100 μF)

FIGURE 3-15. Board-Level Decoupling Capacitor

TI /F/10160-28

### **Electromagnetic Interference**

One of the features of advanced CMOS is its fast output edge rates. For the first time a non-ECL logic family is capable of switching outputs at ECL speeds. In fact, advanced CMOS edge rates exceed that of ECL. ECL outputs typically swing 900 mV in 700 ps, translating into an edge rate of 1.3 V/ns. Advanced CMOS outputs, on the other hand, swing 5.0V in approximately 3.0 ns, translating into an edge rate of 1.6 V/ns. Logic families driving at these speeds, however, are more prone to generate higher levels of system noise. Electronic systems using advanced CMOS logic, as with any other high performance logic system, require a higher level of design considerations.

One element of system noise that will be discussed here is referred to as Electromagnetic Interference, or EMI. The level of EMI generated from a system can be greatly reduced with the use of proper Electromagnetic Compatibility (EMC) design techniques. These design considerations begin at the circuit board level and continue through the system level to the enclosures themselves; EMC needs to be a concern at the initial system design stage.

#### WHAT IS EMI/RFI?

Electromagnetic Interference, or EMI, is an electrical phenomenon where electric field energy and magnetic field energy are transmitted from one source to create interference of transmitted and/or received signals from another source. This may result in the information becoming distorted.

EMI can be an issue of emissions, that is, energy radiated from one system to another or within the same system. It can also be an issue of susceptibility, from high powered microwave signals or nuclear EMP (Electromagnetic Pulse)—an issue more applicable in the military arena than commercial. While this section will specifically address radiated energy, many comments may also apply to susceptibility.

#### SOURCES OF ELECTROMAGNETIC INTERFERENCE

EMI generation in an electronic system may result from several sources. All mediums of signal transmission—from the signal origin to its destination—are possible sources of radiated EMI. Understanding how each medium—including ICs, coaxial cables, and connectors—can radiate EMI is paramount in effective, high performance system design.

As Figure 3-16 illustrates, EMI in a typical electronic circuit is generated by a current flowing in some current path configured within the circuit. These paths can be either V<sub>DD</sub>-to-GND loops or output transmission lines. The propagating current pulse creates magnetic field energy, while the voltage drop across the loop area creates electric field energy. The current path material itself acts as an antenna radiating—or receiving—both the electric and magnetic fields.

EMI generation is a function of several factors. Transmitted signal frequency, duty cycle, edge rate, and output voltage swings are the major factors of the resultant EMI levels. Figure 3-17 illustrates a generalized Fourier transformation of the transmitted signal from the time domain to the fre-

quency domain. To think in terms of EMI, one must think in terms of the frequency domain. This illustration helps to realize the role of the time domain signal components in the frequency domain. Notice that as the signal's period decreases, duty cycle decreases, or rise/fall time decreases that the radiated bandwidth increases.

On the circuit level, in addition to the signal component factors mentioned earlier, radiating area, and the resultant antenna's radiating efficiency also play an important role in EMI generation. Also, current spikes, power line noise, and output ringing caused by outputs switching also contribute to the overall EMI. Good design techniques that moderate this noise will play a major role in minimizing radiated EMI.

#### **OVERALL SYSTEM EMI**

System EMI is a function of the current loop area. Some of the largest loop areas in a system consist of circuit board signal transmission lines, backplane transmission lines, and I/O cables. The current loop areas of the integrated circuit packages—VDD-to-GND loops—are small in comparison to those of the transmission lines and I/O cables. Differences in IC package pinout schemes are much less noticeable in terms of overall system radiated EMI.

The formula used to model the maximum electric field is listed below. This formula takes into account the antenna dimension and efficiency as well as the basic signal components.

$$|E|_{\text{Max}} = \frac{1.32 \times 10^{-3} \bullet I \bullet A \bullet \text{Freq}^2}{D} \left[ 1 + \left( \frac{\lambda}{2} \pi D \right)^2 \right]^{1\!\!/2} \frac{\mu V}{m}$$

where

|E|<sub>Max</sub> is the maximum E-field in the plane of the loop

I is the current amplitude in milliamps

A is the antenna area in square cm

 $\lambda$  is the wavelength at the frequency of interest

D is the observation distance in meters

Freq is the frequency in MHz

and the perimeter of the loop  $P \ll \lambda$ .

Figures 3-18a and 3-18b illustrate lab measurements of radiated emissions from a test board populated with FACT, FACT QS, and a competitor's ACMOS logic. The device under test is driving a similar device across 26 cm of printed circuit board trace.

At higher frequencies where, for example, quarter wavelengths approach the lengths of transmission lines common in typical backplanes and plug-in cards, FACT QS with its innovative noise supressions circuitry radiates substantially less EMI than other ACMOS logic.

#### CIRCUIT BOARD DESIGN CONSIDERATIONS

Original equipment manufacturers cannot afford to fail electromagnetic emissions tests. Since these tests are measured outside of the system, precautions to shield the enclosures, I/O cables, and connections are paramount. However, EMI within a system may also cause errors in data trans-

Designing a system free of all EMI is an overwhelming task. However, considering the following design recommendations at the circuit board level forms a good foundation on which to design a system with good EMC.

- The use of multilayer printed circuit board is a virtual necessity. Two-sided printed circuit board and wire-wrap boards provide no shielding of EMI. Two-sided boards also do not allow the use of power and ground planes. Instead they require the use of high impedance power and ground traces. Planes provide impedances several orders of magnitude lower than that of traces, reducing transient voltage drops in the power distribution and return loops. As a result of these lower voltage drops, power supply induced EMI can also be reduced.
- In addition to the reduced impedance, these power and ground planes have an inherent EMI shielding effect that the large areas of copper provide. With the use of striplines or signal transmission lines sandwiched between the power and ground planes, the designer can take full advantage of the planes' shielding capabilities. To maximize this shielding effect, keep the power and ground plane areas as homogeneous as possible.
- Since plastic provides no EMI shielding, and sockets of any profile provide plenty of lead length, ICs should be soldered directly to the board. Solder power and ground pins directly to the power and ground planes, respectively. Minimize the IC and associated component lead lengths wherever possible.
- Minimizing the number of simultaneously switching outputs will also help to moderate the current pulse amplitude and output ringing.
- Terminating signal traces longer than 8 inches (typical) will minimize reflections and ringing due to those reflections.
- Avoid capacitively coupling signals from one transmission line to another—crosstalk—by avoiding long parallel signal transmission lines. If parallel transmission lines are unavailable, maximize the distance between the two lines, or insert a ground trace. Minimizing the spacing between the signal plane and ground plane will also help reduce crosstalk. For more details, see section on Crosstalk.

#### POWER SUPPLY DECOUPLING CONSIDERATIONS

Much of a system's radiated EMI may originate from the power supply itself. Propagation of power supply noise throughout a system is a very undersirable situation in any respect, including EMI. Suppression of this power supply noise is highly recommended. Decoupling the power supply at every level, from the system supply distribution network, down to the individual IC, is also a necessity when designing for low noise—and low EMI.

 On the system level, the use of a tantalum or aluminum electrolytic capacitor in the power supply distribution network is recommended.

- multilayer ceramic capacitor, 50  $\mu F$  to 100  $\mu F$ , provides good low to medium frequency filtering and EMI suppression.
- To further suppress power supply noise and associated EMI throughout the circuit board itself, the use of a low ESL chip capacitor for each IC is highly recommended. Because the location of any transient noise on a power or ground plane would be impossible to predict, and the IC density of different circuit boards vary dramatically, every IC on these circuit boards should be adequately decoupled. A 0.10  $\mu {\rm F}$  chip capacitor, located as close to each ground pin as possible, will provide good high frequency power supply noise filtering and added EMI suppression.

#### **BACKPLANE CONSIDERATIONS**

The above discussion emphasized design techniques for printed circuit boards. However, because the backplane may, and usually does, consist of several long signal transmission lines, the same low noise design techniques should be used

- Multilayer board techniques should also be applied to the backplane. If possible, these transmission lines should be shielded individually. This would allow for a denser parallel layout of transmission lines as well as providing good EMC.
- Use multiple ground and power connections from the backplane to the circuit boards' power and ground planes to minimize the connection impedance. This will help to further suppress any source of power supply generated EMI.

#### SYSTEM CONSIDERATIONS

One of the major sources of radiated system EMI are the edge connectors, I/O cables, and their associated connectors.

- Use care to ensure that, not only the cables are shielded and the shield properly grounded, but that the shield totally envelopes both the cable and its connectors. The shield should seat firmly into a grounded chassis and touch the chassis a full 360° around the connection. An open ended cable or an improperly grounded connector shield will be a prime suspect for out-of-spec EMI emissions and should be avoided. Use shielded coaxial cables whenever possible. If ribbon cable is preferred, shield all ribbon cables with commercially available ribbon cable shielding. Again, ensure that this shield is properly attached to the connector shield by a full 360°.
- In choosing or designing the enclosure for the system, minimize the number of openings in the enclosure. Since high performance logic now deals with smaller wavelengths than the older technologies, enclosure opening sizes should also be considered. Keep openings as small as possible. If openings are necessary (displays, controls, fans, etc.) there are commercially available accessories that offer good built-in EMI shielding.
- If access panels are necessary, ensure that these panels are properly sealed with some sort of shielding material (gaskets, copper brushes, etc.).
- Of course, the enclosure itself should be of a material that provides good shielding against electric fields.

### Electromagnetic Interference (Continued)

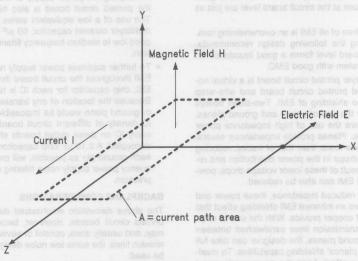
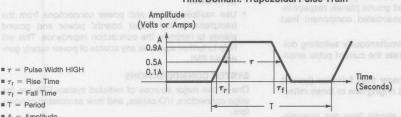


FIGURE 3-16. EMI is Generated by a Current Flowing along Some Path (Loop)

Time Domain: Trapezoidal Pulse Train



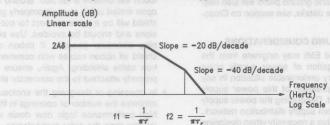
τ = Pulse Width HIGH

 $\mathbf{r}_{r} = \text{Rise Time}$ 

■  $\tau_{\rm f}$  = Fall Time ■ T = Period

■ A = Amplitude

Frequency Domain: Worst-Case Upper Bound Approximation



■ f<sub>1</sub> = 1st Breakpoint

■ f<sub>2</sub> = 2nd Breakpoint

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FIGURE 3-17. Time Domain to Frequency Domain Conversion at a self played metals with nO

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### **Electromagnetic Interference (Continued)**

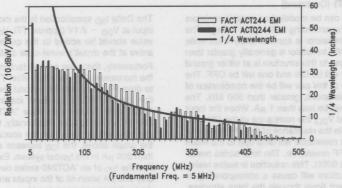


FIGURE 3-18a. FACT Radiation—ACTQ244 versus ACT244

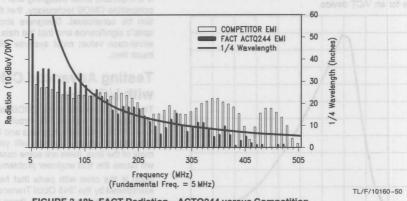


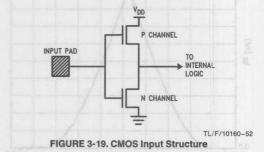
FIGURE 3-18b. FACT Radiation—ACTQ244 versus Competition

## TTL-Compatible CMOS Designs Require Delta I<sub>DD</sub> Consideration

The FACT product line is comprised of two types of advanced CMOS input circuits: 'AC/'ACQ and 'ACT/'ACTQ/'FCT/'FCTA devices. 'ACT/'ACTQ/'FCT/'FCTA indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As these 'ACT/'ACTQ/'FCT/'FCTA series are used to replace TTL, the I<sub>DDT</sub> or Delta I<sub>DD</sub> specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS. In many datasheets I<sub>DDT</sub> or Delta I<sub>DD</sub> are also referred to as I<sub>CCT</sub> or Delta I<sub>CC</sub>. There are no other differences.

It is important to understand the concept of Delta  $I_{DD}$  and how to use it within a design. First, consider where Delta  $I_{DD}$  initiates. Most CMOS input structures are of the totem pole

type with an n-channel transistor in a series with a p-channel transistor as illustrated below.



## TTL-Compatible CMOS Designs Require Delta I<sub>DD</sub>

Consideration (Continued)

These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 4  $k\Omega$  while the resistance of an OFF transistor is generally greater than 500 M $\Omega$ . When the input to this structure is at either ground or VDD, one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 500 M $\Omega$ . The leakage current will then be less than 1  $\mu$ A. When the input is between ground and  $V_{\mbox{\scriptsize DD}}$ , the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as  $600\Omega$ . This reduction in series resistance of the input structure will cause a corresponding increase in IDD as current flows through the input structure. The following graph depicts typical IDD variance with input voltage for an 'ACT device.

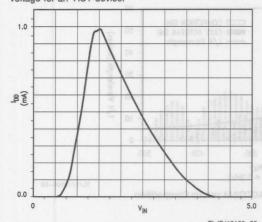


FIGURE 3-20. IDD versus Input Voltage for 'ACT Devices

5.0 (AE) 0.0 0 V<sub>IN</sub> 5.0

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FIGURE 3-21. IDD versus I<sub>IN</sub> for 'AC Devices

The Delta  $I_{DD}$  specification is the increase in  $I_{DD}$ . For each input at  $V_{DD}-2.1V$  (approx. TTL  $V_{OH}$  level), the Delta  $I_{DD}$  value should be added to the quiescent supply current to arrive at the circuit's worst-case static  $I_{DD}$  value.

Fortunately, there are several factors which tend to reduce the increase in  $I_{DD}$  per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive 'ACT-type inputs down to 200 mV and up to 3.5V. Additionally, the typical  $I_{DD}$  increase per input will be less than the specified limit. As shown in the graph above, the  $I_{DD}$  increase at  $V_{DD}-2.1V$  is less than 200  $_{\mu}A$  in the typical system. Experiments have shown that the  $I_{DD}$  of an 'ACT240 series device typically increases only 200  $_{\mu}A$  when all of the inputs are connected to a FAST device instead of ground or  $V_{DD}$ .

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta  $I_{\rm DD}$  specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

## Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for  $I_{\rm DD}$  and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static  $I_{DD}$  specification orders of magnitude less than standard load currents. Most CMOS  $I_{DD}$  specifications are usually less than 100  $\mu A.$  When conducting an  $I_{DD}$  test, greater care must be taken so that other currents will not mask the actual  $I_{DD}$  of the device. These currents are usually sourced from the inputs and outputs.

Since the static  $I_{DD}$  requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an  $I_{DD}$  test. Even a standard  $500\Omega$  load resistor will sink 10 mA at 5V, which is more than twice the  $I_{DD}$  level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during  $I_{DD}$  tests.

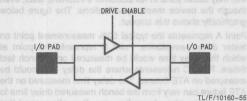
Another area of concern is identified when considering the inputs of the device. When the input is in the transition region,  $I_{\text{DD}}$  can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from  $V_{\text{DD}}$  to ground. This conduction path

## 3

## Testing Advanced CMOS Devices with I/O Pins (Continued)

leads to the increased  $I_{DD}$  current seen in the  $I_{DD}$  vs  $V_{IN}$  curve. When the input is at either rail, the input structure no longer conducts. Most  $I_{DD}$  testing is done with all of the inputs tied to either  $V_{DD}$  or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual  $I_{DD}$  of the device under test which is being measured by the tester.

When testing the  $I_{DD}$  of a CMOS '245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.



#### FIGURE 3-22. '245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the  $I_{DD}$  of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from  $V_{DD}$  to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an  $I_{DD}$  test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined  $l_{\text{IN}}$  specification of the input and the  $l_{\text{OZ}}$  specification of the output. This combined leakage test is defined as IOZ<sub>T</sub>. For FACT devices,  $l_{\text{IN}}$  is specified at  $\pm 1~\mu\text{A}$  while  $l_{\text{OZ}}$  is specified at  $\pm 5~\mu\text{A}$ . Combining these gives a limit of  $\pm 6~\mu\text{A}$  for I/O pins. Usually, I/O pins will show leakages that are less than the  $l_{\text{OZ}}$  specification of the output alone.

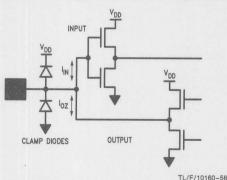


FIGURE 3-23. I/O Pin Internal Structure

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

# Testing Disable Times of TRI-STATE® Outputs in a Transmission Line Environment

Traditionally, the disable time of a TRI-STATE buffer has been measured from the 50% point on the disable input, to the  $(V_{OL}+0.3V)$  or  $(V_{OH}-0.3V)$  point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.

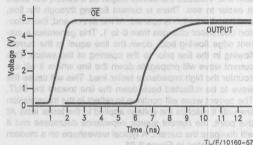


FIGURE 3-24. Typical Bench TRI-STATE Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

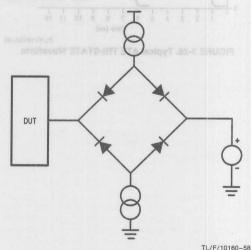


FIGURE 3-25. MCT Wheatstone Bridge Test Load

## Testing Disable Times of TRI-STATE® Outputs in a Transmission Line Environment (Continued)

The voltage source provides a pull-up/pull-down voltage while the current sources provide  $I_{OH}$  and  $I_{OL}$ . When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the  $(\mathrm{V_{OL}}\,+\,0.3\mathrm{V})$  level or fallen to the  $(\mathrm{V_{OH}}\,-\,0.3\mathrm{V})$  level.

Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in Figure 3-26.

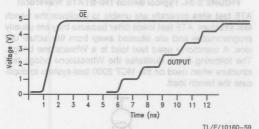


FIGURE 3-26. Typical ATE TRI-STATE Waveform

Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of  $50\Omega$  to  $60\Omega$ , this voltage step can be as minimal as 250 mV. If the comparator was programmed to the disable measurement points, it would be looking for a step of approximately 575 mV at  $5.5\mathrm{V}$  VpD. Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customer's incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.

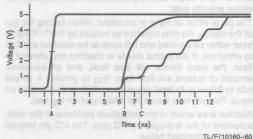


FIGURE 3-27. Measurement Stepout

## **Understanding Latch-Up** in Advanced CMOS Logic

National Semiconductor Application Note 600

Latch-up has long been a bane to CMOS IC applications; its occurence and theory have been the subjects of numerous studies and articles. The applications engineer and systems designer, however, are not so much concerned with the theory and modeling of latch-up as they are with the consequences of latch-up and what has been done by the device designer and process engineer to render ICs resistant to latch-up.

Of equal interest are those precautions, if any, which must be observed to limit the liability of designs to latch-up.

#### WHAT IS LATCH-UP?

Latch-up is a failure mechanism of CMOS (and bipolar) integrated circuits characterized by excessive current drain coupled with functional failure, parametric failure and/or device destruction. It may be a temporary condition that terminates upon removal of the exciting stimulus, a catastrophic condition that requires the shutdown of the system to clear or a fatal condition that requires replacement of damaged parts. Regardless of the severity of the condition, latch-up is an undesirable but controllable phenomenon. In many cases, latch-up is avoidable.

The cause of the latch-up exists in all junction-isolated or bulk CMOS processes: parasitic PNPN paths. Figure 1, a basic CMOS cross section, shows the parasitic NPN and PNP bipolar transistors which most frequently participate in latch-up. The P+ sources and drains of the P-channel MOS devices act as the emitters (and sometimes collectors) of lateral PNP devices; the N-substrate is the base of this device and collector of a vertical NPN device. The P-well acts as the collector of the PNP and the base of the NPN. Finally, the N+ sources and drains of the N-channel MOS devices serve as the emitter of the NPN. The substrate is normally connected to V<sub>CC</sub>, the most positive circuit voltage, via an N+ diffusion tap while the P-well is terminated at Gnd, the most negative circuit voltage, through a P+ diffusion. These power supply connections involve bulk or spreading resistance to all points of the substrate and P-well.

Normally, only a small leakage current flows between the substrate and P-well causing only a minute bias to be built up across the bulk due to the resistivity of the material. In this case the depletion layer formed around the reverse-biased PN junction between P-well and the substrate supports the majority of the V<sub>CC</sub>-Gnd voltage drop. As long as the MOS source and drain junctions remain reverse-biased, CMOS is well behaved. In the presence of intense ionizing radiation, thermal or over-voltage stress, however, current can be injected into the PNP emitter-base junction, forwardbiasing it and causing current to flow through the substrate and into the P-well. At this point, the NPN device turns on, increasing the base drive to the PNP. The circuit next enters a regenerative phase and begins to draw significant current from the external network thus causing most of the undesirable consequences of latch-up. Once established, a latchup site, through the fields generated by the currents being conducted, may trigger similar action in both elements of the IC.

#### WHAT TO DO

As might be expected, latch-up is highly dependent on the characteristics of the bipolar devices involved in the latchup loop. Device current gains, emitter efficiencies, minority carrier life times and the degree of NPN-PNP circuit coupling are all important factors relating to both the sensitivity of the particular latch-up device and to the severity of the failure once it has been excited. Layout geometry and process both contribute significantly to these parameters; CMOS, like other technologies, has been shrunk to provide more function per unit area, increasing susceptibility to latch-up. All major CMOS vendors have upgraded their processes and/or design rules to compensate for this increased susceptibility, some with more success than others. The lateral PNP is typically the weak link in the latch-up loop. As such, various devices can be exploited toward reducing the effectiveness of the PNP to participate in latchup. Guard banding, device placement, the installation of pseudo-collectors between the P-channel devices and the P-well, and the use of a low resistivity substrate under an epitaxial layer are a few of the IC design tactics now being practiced to reduce the current gain or to control the action of the lateral PNP structures in state-of-the-art CMOS devic-

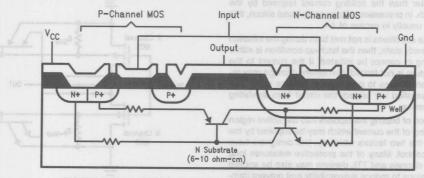


FIGURE 1. Basic CMOS Inverter Cross Section with Latch-Up Circuit Model

or UMOS ICS may still pose problems that the CMOS vendor has little control over. Hence, CMOS users must be aware of what they are doing and those measures which must be taken to reduce the susceptibility to latch-up. The use of CMOS at or beyond its rated maximum voltage range and the presence of inductive transients are applications-related situations which can trigger latch-up. Environment, including thermal stress, poorly regulated or noisy supplies and radiation incidence can also contribute to or cause latch-up. The system engineer must consider these situations when using CMOS in designs.

While latch-up is generally recognized as resulting from regenerative switching along a PNPN path, many designers incorrectly assume that this regenerative action places the device in a state that can only be recovered from if the system is powered down. The fact is that there is probably an equal, if not greater, chance that the regenerative switching, when encountered, will be non-sustaining (the condition, more accurately referred to as current amplification, will disappear when the triggering stimulus is removed); over-voltage applied to properly designed input protection networks is one example of controlled current amplification. For sustained latch-up to occur, the regeneration loop must have sufficient gain and the power source must be able to supply a minimum current. From this we can see that current-limited power supplies might be used to recover from or reduce the effects of latch-up. Another method uses current-limiting series resistors in the power connections of offending ICs in conjunction with storage capacitors shunting the devices. Normal switching current will be drawn from the capacitors while DC current will be limited by the resistors.

In the loop of positive current feedback formed by the parasitic PNP and NPN transistors of the latch-up structures, regenerative switching may result if sufficient loop gain is available. One must remember, though, that three conditions are necessary for latch-up to occur.

- 1) both parasitic bipolars must be biased into the active state:
- the product of the parasitic bipolar transistor current gains (Bnpn•Bpnp) must be sufficient to allow regeneration, i.e., greater than or equal to one;
- the terminal network must be capable of supplying a current greater than the holding current required by the PNPN path. In processes utilizing an epitaxial silicon, this current is usually in excess of 1A.

If any of these conditions is not met both during the initiation and in the steady state, then the latch-up condition is either non-sustaining or cannot be initiated. If the current to the latched structure is not limited, permanent damage may result. Again, any means to prevent any of these conditions from being satisfied will protect the circuit from exhibiting sustained latch-up.

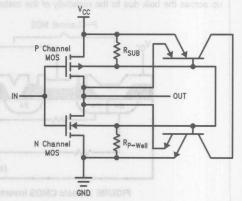
The prevention of biasing the bipolars into the active region and the limiting of the current which may be supplied by the network are the two factors which system designers have under their control. Many of the protective measures long exercised in discrete and TTL designs may also be applied to CMOS designs to reduce susceptibility and prevent damage to these systems. Diode clamping of inductive loads, signal and supply level regulation, and sharing of large DC loads by several devices with suitable series limiting resistance.

CMOS ICs which have latch-up paths associated with them; these are the inverter or gate and the transmission switch. Both structures may be susceptible under the right conditions. While the CMOS inverter can exhibit latch-up independent of circuit configuration, the transmission switch usually has lower holding current, and thus, a lower threshold for latch-up, but is dependent on its external connections for latch-up to occur. Figure 2 shows the lumped equivalent circuit of the inverter. Notice the shunting resistors across the base-emitter junctions of the bipolar transistors: these resistors divert base drive from the bipolars and as a result increase both the trigger current and holding current levels required for the structures to participate in latch-up. A further increase in these current levels can be achieved by further decreasing the shunt resistance. Diffusing all active components into an epitaxial silicon, under which would lie a substrate of substantially less resistivity, will have a dramatic effect on decreasing the shunt resistance, therefore increasing the trigger current and holding current levels required for latch-up.

#### THE CIRCUIT CONNECTION

As we have seen above, the external circuit connections are regular participants in the latch-up process. The current for latch-up comes from these connections and often the triggering mechanism is external to the latching device. All three classes of external connections (power, input and output) are important in latch-up. We will now look at how these connections relate to this process.

Current injection through the power terminals when the power supply voltage is beyond the maximum rated for the CMOS device can directly cause latch-up through base collector leakage or breakdown mechanisms. One aspect of high power supply voltages that is not often recognized is the effect of field-aiding lateral currents under the emitters of the PNP devices. This can effect a significant increase in the beta of these devices, making internally trigger latch-up much more prevalent. Again, the warning to the the system designer is to avoid using CMOS at maximum rated supply voltages unless precautions are taken to insure latch-up is unlikely or is at least acceptable and recoverable. Switching transients coupled onto power lines has become a problem



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FIGURE 2. CMOS Inverter with Parasitic Bipolars

en just the same.

Latch-up involving input terminals, next to gate oxide rupture, used to be one of the most common failure mechanisms of CMOS. Transients exceeding the power supply routinely caused either or both of these effects to occur. Fortunately, CMOS vendors have learned to make better input protection networks and have learned that proper placement of these components with respect to the rest of the chip circuitry is necessary to reduce susceptibility to latch-up. The system designer should review foreign input signals to CMOS systems and take precautions necessary to limit the severity of over/undershoot from these sources. Measures which could be used to reduce the possibility of latch-up induced by input signals are: proper termination of transmission lines driving CMOS, series current limiting resistors, AC coupling with DC restoration to the CMOS supplies, and the addition of Schottky diode clamps to the CMOS power rails. As an additional measure there are several CMOS circuits which have input protection networks that can handle overvoltage in one direction or the other and which are specifically designed to act as interface circuits between other logic families and CMOS. Judicious application of these will also aid in suppressing any tendencies of CMOS systems to latch-up.

Finally, attention to CMOS outputs, their loading and the stresses applied to them will also enable the designer to generate latch-up free systems. Historically, output terminals of CMOS have been least likely to cause latch-up though they can participate in latch-up once it is initiated. The normal mode of failure in this respect is, again, the application of voltages beyond the CMOS supplies or the maximum limit for the devices though excessive current has also been linked to latch-up failure at elevated temperatures. Inductive surges and transmission line reflections are the most likely sources of output latch-up in CMOS and should be attended to in the most applicable method, i.e., by clamping, termination or through dissipative measures.

#### WHAT WE HAVE DONE

National Semiconductor, as an important supplier of advanced CMOS to all segments of the industry, has made a commitment to provide IC designs which make use of state-of-the-art latch-up suppression techniques in an effort to support its customers before they need support. The three most important actions which we have taken to guard our customers from latch-up are in the areas of layout, power distribution and process design. These techniques, along with recognized good design practice, yield a product line that lives up to the intent of an advanced CMOS family. In brief review, National Semiconductor's attack on latch-up is summarized in the following.

less troublesome. All devices are scrutinized for potential latch-up sites and are protected by similar geometries where any risk is significant.

#### **Power Distribution**

Careful attention to on-chip power distribution and enhanced termination of P-wells and substrate is used by National Semiconductor to improve latch-up resistance. Our double metal process affords the advantage in maintaining low impedance distribution of power and ground potentials over the entire chip; the potential gradient-caused fields which often induce or enhance latch-up are thus minimized while functional performance is enhanced by cleaner on-chip power supplies.

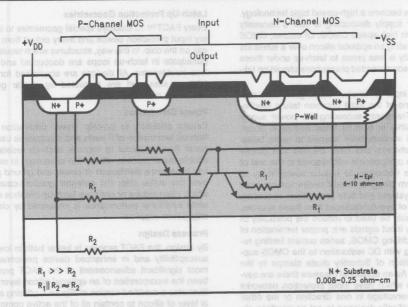
#### **Process Design**

By design, the FACT process is better both in low latch-up susceptibility and in enhanced device performance. The most significant advancement of the FACT process has been the incorporation of an epitaxial silicon layer. Figure 3 illustrates a modified version of Figure 1, utilizing an epitaxial layer of silicon to contain all of the active components of the CMOS circuit. This epitaxial layer allows the use of a separate layer of substrate silicon, of a resistivity some three orders of magnitude lower than the epitaxial layer. The effect is also modeled in Figure 3.

As illustrated, the resistivity of the epitaxial silicon,  $R_1$ , is on the order of 6 ohm-cm to 10 ohm-cm. The underlying substrate resistivity,  $R_2$ , is as low as 0.008 ohm-cm to 0.025 ohm-cm. The result is a parallel combination of resistivities,  $R_1$  and  $R_2$ , that is equivalent to  $R_2$ . What has now happened is that the gain of the parasitic PNP-NPN circuit has been dramatically slashed. Under the same latch-up conditions described earlier, the introduction of the low resistivity substrate now means that at least 10 times more current is needed to trigger the parasitic PNP-NPN combination.

The active components within the epitaxial layer maintain the same performance characteristics as those of the active area illustrated in the non-epitaxial CMOS circuit of Figure 1. Therefore the introduction of the epitaxial layer to the FACT process does not reduce any AC, DC, functional or ESD performance. However, what we have is an advanced CMOS logic family that is now virtually latch-up immune.

Thus, through innovative and careful layout, attention to eliminating circuit situations which could be latch-up prone and by careful selection and maintenance of our advanced CMOS process, FACT sets the standard for latch-up resistance.



#### TL/F/10192-3

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Finally, attention to CMOS outputs, their loading and the

#### WHAT WE HAVE DONE

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#### INTRODUCTION

Advanced CMOS logic such as National Semiconductor's FACT (Fairchild Advanced CMOS Technology) logic, has extended CMOS performance to the level of advanced bipolar technologies. While high-performance design rules that are currently utilized for bipolar designs are also applicable to CMOS, power consumption becomes a new area of concern in high-performance system designs.

One advantage of using advanced CMOS logic is its low power consumption. However careless circuit design can increase power consumption, possibly by several orders of magnitude. A simple FACT gate typically consumes 625  $\mu \text{W/MHz}$  of power; at 10 MHz, this translates to 6.25 mW. A 50 $\Omega$  parallel termination on the line will use over 361 mW with a 50% duty cycle.

The use of high-performance system board design guidelines is important when designing with advanced CMOS families. Because of advanced CMOS logic edge rates (less than 3 ns-4 ns), many signal traces will exhibit transmission line characteristics.

A PCB trace begins to act as a transmission line when the propagation delay (t<sub>pd</sub>) across the trace approaches one third of the driver's edge rate. For advanced CMOS, lines as short as 6 to 8 inches may exhibit these effects. This rule

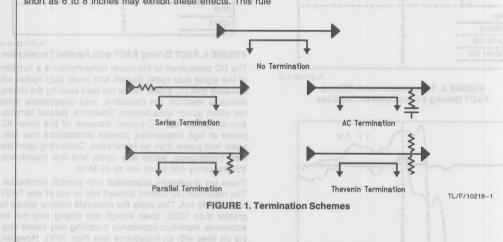
because the high-power disalpation of this termination

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encompasses many traces on a standard PCB. With older CMOS technologies which have lower edge rates, this critical length is much longer: 18 inches for 74HC and 5 feet for CD4000 series and 74C devices. A transmission line terminating into a mismatched impedance could result in transient noise which adversely affects signal integrity.

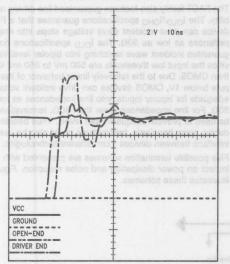
The FACT family also features guaranteed line driving capability. The  $I_{\rm OLD}/I_{\rm OHD}$  specifications guarantee that a FACT device can drive incident wave voltage steps into line impedances as low as  $50\Omega$ . The  $I_{\rm OLD}$  specifications do not guarantee incident wave switching into bipolar level inputs since the input low thresholds are 500 mV to 850 mV lower than CMOS. Due to the relatively linear behavior of the outputs below 1V, CMOS devices can drive incident voltages, adequate for bipolar inputs, into line impedances as low as  $80\Omega$ . For line impedances lower than  $80\Omega$ , termination can be used to provide adequate input levels. Thus besides reducing noise transients, terminations could also be used to interface between devices from different technologies.

Five possible termination schemes are presented with their impact on power dissipation and noise reduction. *Figure 1* illustrates these schemes.



#### NO TERMINATION

No termination is the lowest cost option and features the easiest design. For line lengths 8 inches or less, this is often the best choice. For lines longer than 8 inches, transmission line effects (line delays and ringing) may exist. Figure 2 illustrates the effect of a FACT device driving a 3-foot open-ended coaxial line. Clamp diodes at the inputs of most logic devices tend to reduce the ringing and overshoots. Often, these clamp diodes are sufficient to insure reliable system operation. Figure 3 illustrates the impact of these diodes on the same 3-foot coaxial line. However, it is not uncommon to find logic devices like DRAMs, D-to-A converters and PLDs, that have no input clamp diodes.



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FIGURE 2. Transmission Line Effects

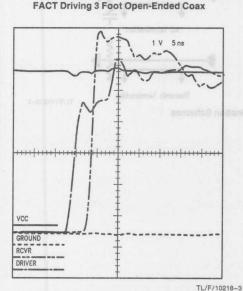
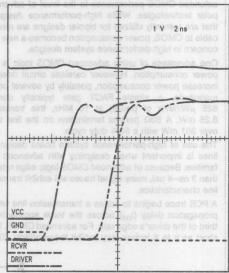


FIGURE 3. Effects of Input Clamp Diodes FACT Driving FACT with no Termination

## PARALLEL TERMINATION

Parallel termination provides an AC and DC current path back to the power supply for switching currents. While it effectively reduces ringing (Figure 4), the DC path to ground or to  $V_{\rm CC}$  will dissipate power. The power consumption for this type of a termination scheme has some important implications. For proper impedance matching the value of this terminating resistor should be equal to the characteristic impedance of the line.



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## FIGURE 4. FACT Driving FACT with Parallel Termination

The DC component to the power consumption is a function of the signal duty cycle. Signals with lower duty cycles will dissipate less DC power. Since the load seen by the driving device is resistive, not capacitive, load capacitance does not affect power consumption. Therefore, parallel termination dissipates less AC power. Because of this lower AC power at high frequencies, parallel terminations may consume less power than no termination. Depending upon the load capacitance, signal duty cycle, and line impedance, this frequency can be as low as 40 MHz.

There are drawbacks associated with parallel termination. The maximum DC current allowed into or out of any FACT output is 50 mA. This limits the allowable resistor values to greater than 100 $\Omega$ . Even though this ringing may not be excessive, imperfect impedance matching may cause ringing on lines with an impedance less than 100 $\Omega$ . However, because the high-power dissipation of this termination scheme negates the advantages of advanced CMOS logic, this is not an intended advanced CMOS application.

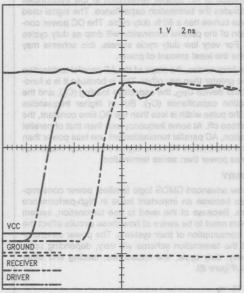
Parallel termination tends to unbalance CMOS outputs. Using a resistor to ground, the CMOS device will achieve a 0.0V output low voltage ( $V_{OL}$ ). But due to the high DC load in the logic HIGH state, the output high voltage ( $V_{OH}$ ) will be degraded (*Figure 4*). This degraded high level output will be above the input high voltage ( $V_{IH}$ ) of both CMOS and bipolar inputs due to the guaranteed dynamic current ( $V_{OHD}$ ) specifications (75 mA @ 3.85V,  $V_{CC} = 5.5$ V). This lower  $V_{OH}$  level may cause an increase in  $I_{CC}$  if the driven device is CMOS; however, this increase should be minimal.

# 3

#### THEVENIN TERMINATION

Thevenin termination is similar to parallel termination, except that both pull-up and pull-down resistors are used. Power consumptions are also similar for both of these schemes. The difference is that the DC power consumption is a function of duty cycle and resistor ratios. If the resistors are matched, DC power consumption is not dependent upon duty cycle. One advantage Thevenin termination has over parallel termination is that lines with impedances as low as  $50\Omega$  can be terminated in their characteristic impedances. For proper impedance matching, the equivalent thevenin resistance should be the same as the line characteristic impedance.

Thevenin termination does not create unbalanced CMOS outputs, although it reduces the output swing (Figure 5). This limited output swing may increase current consumption in a driven CMOS device however this increase is minimal.



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# FIGURE 5. FACT Driving FACT with Thevenin Termination

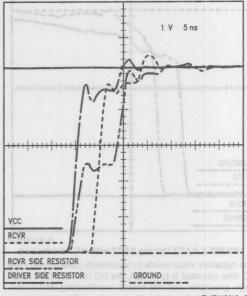
Busses using Thevenin termination should not be left floating. A floating bus level is determined by the ratio of the resistors. If this level is close to any input threshold, output oscillations and  $I_{\rm CC}$  increase may occur. If the bus must be left floating, the resistor ratio should be chosen so that an adequate noise margin is insured. The bus could be left floating by either turning off the driver or by placing the bus in a high impedance state.

Other terminations which do not introduce DC current paths may be more suitable to CMOS systems. These include series and AC parallel terminations.

# SERIES TERMINATION

Series termination works by limiting the current that is put into a line. While other termination circuits dissipate extra power, series termination reduces power consumption and dissipates less energy than no termination. This is a recommended termination scheme for the FACT family because of its low power dissipation.

Series termination assumes that any voltage step driven into a transmission line will double at the receiver. Therefore, the initial voltage step driven into the line is one-half of the receiver input voltage. The resistor value can be computed by  $R_{\rm S} = Z_{\rm O} - R_{\rm D}$ , where  $R_{\rm S}$  is the resistor value,  $Z_{\rm O}$  is the line impedance and  $R_{\rm D}$  is the driver resistance. Figure & illustrates the waveforms associated with series termination.



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## FIGURE 6. FACT Driving FACT with Series Termination

While the device output produces a full output step, only half of that is driven into the line. At the receiver end, the edge doubles, thus recreating the full output swing. The initial step then reflects back, fixing the full output voltage applied on the entire line. A voltage plateau is created at the input to the line whose width will be twice the line tpd.

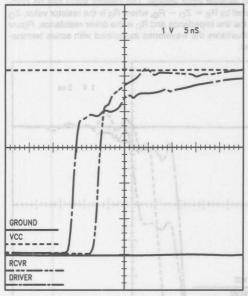
Series termination is well suited for lines with a single driver receiver pair. Series termination limits the initial voltage step, which offers several benefits: reduced power consumption and decreased cross-coupled radiated noise.

One possible drawback to series termination is that any other receiver located near the driver will see the voltage plateau. Because the plateau level may be very close to the typical CMOS threshold (50% of V<sub>CC</sub>), any such input could see multiple input switching. Combinatorial outputs may oscillate, or clocked inputs may experience multiple clocking. One solution is to choose the resistor value that keeps the initial voltage step away from the input thresholds. Larger resistor values will require one or more reflections to settle out, while still maintaining valid V<sub>IN</sub> levels at the inputs. Smaller values will generate overshoot and undershoot.

## AC PARALLEL TERMINATION

AC Parallel termination is another technique which blocks the DC path to ground. A capacitor in series with the parallel termination resistor blocks the DC path, while maintaining the AC path. This is a highly recommended termination scheme for the FACT family because of its negligible DC power consumption.

After the initial voltage step, the capacitor will charge up to the rail voltage at a rate determined by the RC time constant of the circuit (Figure 7).



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FIGURE 7. FACT Driving FACT with AC Termination

The capacitor value needs to be carefully determined. If the RC time constant is too small, the RC circuit will act as an

edge generator and will create overshooting and undershooting. While increasing the capacitor reduces overshoot, it also increases power consumption. As a rule, the RC time constant should be greater than 3 times the line delay.

When driving TTL-level inputs, the same threshold concerns arise as with no termination. The  $I_{OLD}$  current specifications guarantee incident wave switching into CMOS inputs on line impedances as low as  $50\Omega.$  For TTL-level inputs, this minimum line impedance rises to  $80\Omega.$  When the line impedance is less than  $80\Omega,$  a termination value greater than the line impedance will increase the amplitude of the initial voltage step; this can be used to guarantee incident wave switching into both TTL and CMOS-level inputs. Large resistor values will cause ringing on the line, but the amplitude should be small and not present any problems.

At lower frequencies, this termination capacitance increases the total signal trace impedance; therefore, it also increases the slope of the power consumption curve. At higher frequencies, the capacitor is unable to fully charge or discharge, and the slope of the curve falls off. At very high frequencies, AC parallel termination acts like a parallel resistor tied to an intermediate voltage supply, with the voltage level determined by the signal duty cycle. The slope of the power consumption curve is dependent on CpD (Power dissipation capacitance) of the device. The power crossover point between no termination and AC termination may be as low as 15 MHz, depending upon the system capacitive loading and the signals' duty cycle.

## POWER CONSUMPTION

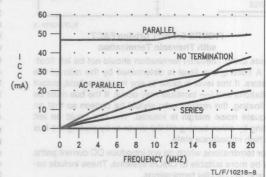
The use of one of these termination schemes will affect the power consumption of the system. Power consumption depends upon the circuit used, signal frequency, device and signal trace loads, signal duty cycle, system V<sub>CC</sub> and component values.

Figure 8 shows the power consumption of each type of termination circuit over a frequency range. For low frequency signals, termination circuits without DC components will usually use less power (no termination, series termination and AC parallel termination). At higher frequencies, parallel termination or AC termination may consume less power because of lower AC power consumption. The AC power consumption of these two termination schemes is a function of the device CPD, while the AC power consumption of the other termination schemes is a function of both the device CPD and the system capacitive loading (CI). The AC power consumption of AC parallel termination at low frequencies also includes the termination capacitance. The signal used for these curves has a 50% duty cycle. The DC power consumption of the parallel termination will drop as duty cycles drops. For very low duty cycle signals, this scheme may consume the least amount of power.

For low frequencies, the slope of the AC parallel termination curve is greater than any other. This is because it is a function of the device  $C_{\text{PD}}$ , the capacitive loading  $(C_L)$ , and the termination capacitance  $(C_T)$ . But at higher frequencies where the pulse width is less than the RC time constant, the slope drops off. At some frequency less than that of parallel termination, AC parallel termination will use less power than using no termination. At some higher frequency, this circuit uses less power than series termination.

#### SUMMARY

With new advanced CMOS logic families, power consumption has become an important issue in high-performance systems. Because of the need to use termination, system designers need to be aware of how these circuits affect the power consumption of their systems. The power consumption of the termination scheme will vary, depending upon frequency, duty cycle, line impedance, loading and other factors (Figure 8).



**FIGURE 8. Power Consumption** 

Parallel: Resistor = Z<sub>O</sub>
 Thevenin: Resistor = 2 x Z<sub>O</sub>

• Parallel: Resistor =  $Z_O$ • Thevenin: Resistor =  $2 \times Z_O$ • Series: Resistor =  $Z_O - Z_{OUT}$ • AC: Resistor =  $Z_O - Z_{OUT}$ Capacitor =  $Z_O - Z_{OUT}$ 

For additional information on terminations, refer to these National Semiconductor publications.

Active: Resistor = 2 x Z<sub>O</sub>

1. FAST Applications Handbook, 1987.

2. F100K ECL User's Handbook, 1986.

entals.

Tyure 1e shows a simple circuit model for a CMOS device in a leadframe cirving a standard test test. The inclusion Lt appreciation is the inclusion Lt appreciation in the power lead of the provider the inclusion of the standards in the power lead of the package; inductor the represents the power lead of the package; inductor the represents the sesistor R1 represents the output impedence of the device standard eat load on the output impedence of the device the standard eat load on the output of the device. The first waveform shows the standard eat load on the output of the standard eat load on the device. The first waveform shows the voltage (V) across the load as it is switched from a logic than the characteristics of the output slew rate is dependent represented the standard than a logic than the characteristics of the output literals and the respection shows the output stant is generated as the capacitance. The the capacition decharges (I) = -O<sub>L</sub> \* dV/dI). The third waveform shows the voltage that is induced across the interval and the restandard one the entanding currents because the standard contractions shows the voltage that is induced across the interval and the standard contractions of the changing currents because the standard contractions of the standard contractions and the standard contractions of the standard contractions of the standard contractions and the standard contractions of the standard contractions of the standard contractions and the standard contractions of the standard contractions of the standard contractions of the standard contractions.

Power consumption is not the only concern when choosing a termination circuit. Part-count and board space are also

important concerns. It is up to system designers to choose

which, if any, termination circuit is best suited to their circuit.

Table I shows the recommended values for the various ter-

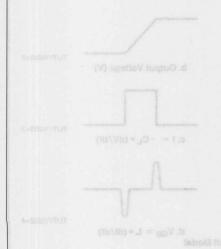
mination schemes. It is highly recommended that the designer use these values as a starting point and adapt it for

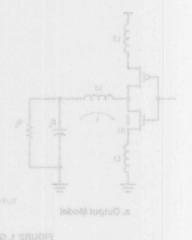
the most feasible and optimum results.

While these diagrams and figures are useful in explaining the origins of ground bounce, they are highly theoretical and the original ground bounce, they are highly theoretical idealistic. There are many second and third order absorbed which would need to be considered for a complete theoretical analysis. Considering these effects, though, would lead to highly complex second and third order differential aquestions which are difficult to solve. The purpose of this application note is to develop a fundamental understanding of

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In 1982, National Senticonductor, formerly Fairchild Senticonductor, began to develop FACTM (Fairchild Advanced
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divertibles considerations.





# Understanding and Minimizing Ground Bounce

National Semiconductor Application Note 640



As system designers begin to use high performance logic families to increase system performance, they may run into new problems which previously did not raise concern when lower performance devices were utilized. These problems can generally be avoided by following a few simple rules. This application note discusses the subject of ground bounce with respect to high performance CMOS logic families and offers a set of simple guidelines that will eliminate system problems due to this phenomenon.

Ground bounce has been a concern to some system designers for many years. Its effects can be found in most bipolar and CMOS logic families. However, ground bounce has recently become a major issue. Although new advanced CMOS logic families have edge rates comparable to advanced bipolar logic devices, CMOS outputs swing almost from rail to rail while bipolar outputs swing from ground to approximately 3.0V. These edge rates, coupled with the greater voltage swings found in today's advanced CMOS logic devices, tend to generate more ground bounce noise than their bipolar counterparts.

In 1982, National Semiconductor, formerly Fairchild Semiconductor, began to develop FACTTM (Fairchild Advanced CMOS Technology) logic incorporating more than three years of experience gained with FAST® (Fairchild Advanced Schottky TTL) logic into the groundwork. As a result, Fairchild was able to understand the important trade-offs associated with high performance in a logic family. In the bipolar world, these trade-offs were between speed and power; in the CMOS world, the trade-offs are between speed and ease of use. Utilizing experience gained from FAST products, the FACT family objectives were defined to provide the optimum solution, allowing greater system performance while minimizing system design problems. Using FACT devices does require more attention toward circuit design and board layout than older, slower technologies. The resulting advantages—low power and high performance—greatly outweigh these considerations.

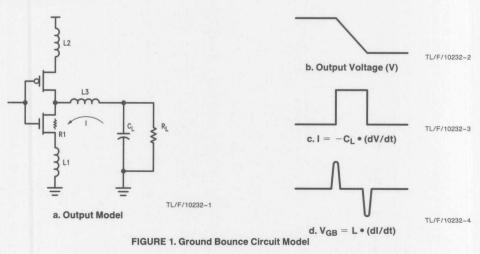
#### **DEFINING GROUND BOUNCE**

As edge rates and drive capability increase in advanced logic families, the effects of intrinsic electrical characteristics become more pronounced. One of these intrinsic electrical characteristics is the inductance found in all leadframe materials

Figure 1a shows a simple circuit model for a CMOS device in a leadframe driving a standard test load. The inductor L1 represents the intrinsic inductance in the ground lead of the package; inductor L2 represents the intrinsic inductance in the power lead of the package; inductor L3 represents the intrinsic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor  $C_{\rm L}$  and  $R_{\rm L}$  represent the standard test load on the output of the device.

The three waveforms shown in Figures 1b, c, and d depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, and the inductors L1 and L3, and  $C_L$ , the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [I =  $-C_L \bullet \text{dV/dt}$ ]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [VGB = L  $\bullet$  (dI/dt)].

While these diagrams and figures are useful in explaining the origins of ground bounce, they are highly theoretical and idealistic. There are many second and third order effects which would need to be considered for a complete theoretical analysis. Considering these effects, though, would lead to highly complex second and third order differential equations which are difficult to solve. The purpose of this application note is to develop a fundamental understanding of ground bounce and to provide a useful set of design guide-

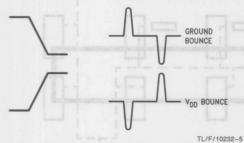


rent, as it changes, causes a voitage to be generated across the inductances in the circuit. The formula for the voltage across an inductor is V = L • (dl/dt). This induced voltage creates what is known as ground bounce. Because the inductor is between the external system ground and the internal device ground, the induced voltage causes the internal ground to be at a different potential than the external ground. This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the external system ground. External to the device, ground bounce causes input thresholds to shift and output levels to change. This situation is very similar to that of large systems where voltages can develop across expansive ground networks.

## OTHER CAUSES OF GROUND BOUNCE

Although this discussion is limited to ground bounce generated during HIGH-to-LOW transitions, it should be noted that the ground bounce is also generated during LOW-to-HIGH transitions. This ground bounce is created by the large gate capacitances associated with the output transistors on the die. Because these gate capacitances are larger than the gate capacitances of earlier-stage transistors, more current is generated when they switch. The output buffer stages of CMOS devices are inverters; thus their inputs are switching HIGH-to-LOW when their outputs are switching LOW-to-HIGH. It is the currents associated with switching these inputs to the output transistors that generate ground bounce when the output switch LOW-to-HIGH. This LOW-to-HIGH ground bounce has a much smaller amplitude and therefore does not present the same concern.

We should also note that everything discussed here concerning ground bounce can be applied to the opposite effect,  $V_{DD}$  bounce.  $V_{DD}$  bounce is the inverse of ground bounce. As one would expect, there is an intrinsic inductance in the  $V_{DD}$  lead as well as the ground lead. The internal  $V_{DD}$  potential will collapse toward ground at the beginning of a LOW-to-HIGH transition and then bounce above the external  $V_{DD}$  potential at the end of the transition.



- V<sub>DD</sub> bounce (droop) is the voltage drop across the package
- Inductance (to VDD) is caused by charging load capacitances
- V<sub>DD</sub> bounce is less of a concern than ground bounce because TTL-level inputs have greater high noise immunity

# FIGURE 2. Ground Bounce/V<sub>DD</sub> Bounce

In addition, V<sub>DD</sub> bounce is generated during HIGH-to-LOW transitions for the same reasons that ground bounce is generated during LOW-to-HIGH transitions.

gin. For CMOS driving TTL, the input high noise margin approaches 3.5V, and for CMOS driving CMOS, the input high noise margin approaches 2.5V. In either case, the input high noise margin is 3 to 5 times greater than any expected V<sub>DD</sub> bounce.

#### CONTRIBUTING FACTORS OF GROUND BOUNCE

While our circuit diagrams shown above are useful for explaining the origins of ground bounce, they are too idealistic to be used for modeling. In the real world, there are many other variables which affect the actual shape and amplitude of the induced voltage. To develop an accurate model, the resistor must be replaced with a model of the actual transistor. In addition, the period where the transistors are turning on and off would need to be taken into account. Including these variables, plus others, would lead to highly complex differential equations that are nearly impossible to solve except by the most advanced computer programs. Since theoretical analysis of ground bounce is difficult to perform, we will use empirical data to develop an understanding of ground bounce and how it is effected.

There are several factors which affect ground bounce: the number of outputs switching simultaneously; the location of the output pin; the location and type of load on the line; the  $V_{DD}$  voltage; the device technology; and the output and ground inductances. Each of these factors play a critical role in the generation of ground bounce.

## GROUND BOUNCE DEMONSTRATION BOARD

In order to evaluate ground bounce and the factors which affect it, Fairchild designed a board which allowed side-by-side evaluation of ground bounce under varying conditions.

Figure 3 shows the functional block diagram of the board. A counter generates the changing data lines by counting from 0 to 127. The counter can also be configured to count down from 127 to 0 so that  $V_{\rm DD}$  bounce may be evaluated. This changing data is clocked into an 'AC374 and then passed into both another 'AC374 and an 'AC244. This was done for two reasons.

First, the noise generated by the first 'AC374 represents gound bounce generated by a lightly-loaded circuit. Secondly, being able to choose between either the 'AC374 or the 'AC244 to drive the system bus allows us to evaluate both devices under heavy load conditions. The quiet output from these two devices drives a line that is connected to the clock inputs of eight '74 D-type flip-flops and two inverter inputs. Each flip-flop is configured so that if a valid clock was encountered, the Q output will go from a "0" to a "1"; each flip-flop acts as qlitch catcher, detecting any ground bounce noise which violates the flip-flop clock thresholds. Devices from several common logic families are connected to this quiet output so that the effect on different technologies can be evaluated.

The seven other outputs of the 'AC374 or the 'AC244 drive a 7-bit data bus. This data bus is loaded with fourteen devices, which represents a typical heavily-loaded system bus and allows us to evaluate ground bounce under these conditions.

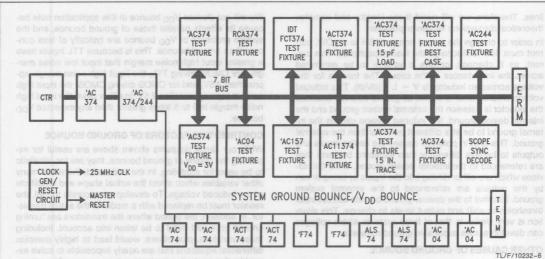


FIGURE 3. Ground Bounce Demonstration Board Block Diagram TABLE I Critical Signal Statistics

| TABLE I. Officer Signal Statistics |          |        |        |      |         |       |                     |                      |
|------------------------------------|----------|--------|--------|------|---------|-------|---------------------|----------------------|
| Signal                             | Length   | со     | LO     | RO   | # Loads | CL    | Termination<br>Type | Termination<br>Type  |
| DATA BUS                           | 30 Inch  | 107 pF | 565 nH | 1.3Ω | 14      | 70 pF | PARALLEL            | 50Ω                  |
| CLOCK*                             | 28 Inch  | 103 pF | 445 nH | 1.0Ω | 16      | 80 pF | THEVENIN            | $71\Omega/120\Omega$ |
| GROUND BOUNCE                      | 7.5 Inch | 30 pF  | 117 nH | 0.2Ω | 10      | 50 pF | AC                  | $26\Omega/200\Omega$ |

• Clock generated from seven (7) stage ring oscillator ('AC240)—approximately 25 MHz

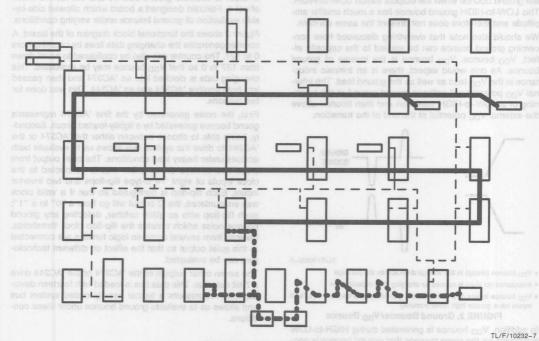


FIGURE 4. Critical Signal Paths

3

Each device on the bus is configured equivalent to a standard test fixture. Conditions such as output loading, load placement, power supply voltage, and quiet output pin location were varied to compare ground bounce under different conditions. Also, some device locations were populated with different device types and devices from other logic families to evaluate ground bounce across technologies.

Table I lists the important electrical characteristics for the critical signal paths. *Figure 4* shows the physical layout of the board and the critical paths. This board was used to generate the data and waveforms presented in this application note unless otherwise noted.

#### LEAD INDUCTANCE

The impact of the ground inductance on ground bounce seems to be obvious. For a given dl/dt value, the greater the inductance, the greater the ground bounce. While this would imply that reducing the ground inductance should reduce the ground bounce, this is not always the case. The explanation is fairly straightforward.

Ground bounce tends to limit the available AC current in CMOS outputs by reducing the voltage across the output impedance, and therefore, reduces the current that will flow. When the ground lead inductance is reduced, a corresponding increase in the output edge rate of the device occurs. This is due to the fact that by reducing the inductance in the ground lead we have increased the available AC current. This greater dl/dt tends to reduce any improvement that the reduced ground inductance may have generated.

National tested FACT to investigate the effect of ground inductance on ground bounce. This was accomplished by assembling die from the same manufacturing lot in plastic DIPs; some were assembled using the standard pinout and some were assembled with the ground and power pads connected to the center pins. When the data was analyzed, it was found that the die assembled with center pin V<sub>DD</sub> and ground averaged approximately 10%–15% less ground bounce than the die assembled with the standard pinouts. Along with the small reduction in ground bounce, they also exhibited somewhat faster edge rates with corresponding decreases in propagation delays.

# OTHER PACKAGES

The inductance in the ground lead is not the only inductance in the package; all of the output pins have an associated inductance. The inductances in the outputs also contribute to ground bounce, especially any oscillatory effects. While just reducing the ground or V<sub>DD</sub> does not significantly reduce ground bounce, reducing the inductance in both the power leads and the outputs does reduce ground bounce.

Figure 5 outlines the effect that packaging has on ground bounce. In order to make the comparison as valid as possible, die from the same wafer were used. This was necesary because the effect of process variations on ground bounce is greater than the effect of packaging. It can be seen that packages with smaller power and signal lead inductances tend to reduce ground bounce. It is important to note that the difference between CDIP and LCC package ground lead inductance is approximately one order of magnitude (20 nH versus 2 nH), yet the difference in ground bounce is less than 35%.

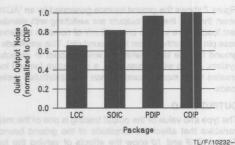


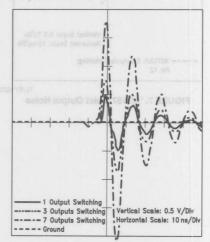
FIGURE 5. Noise vs Package Configuration

Reducing the ground lead inductance is not "the" solution to ground bounce problems. While a small reduction in ground bounce can be realized, additional problems, like increased crosstalk, may occur. A better solution is to reduce the inductance in all leads. Smaller packages, such as SOIC and LCC/PLCC packages, do reduce ground bounce over both standard and center-V<sub>DD</sub>/ground-pinned DIP packages.

#### NUMBER OF OUTPUTS SWITCHING

The number of outputs switching simultaneously affects the amplitude of ground bounce. For a simple model, treat the output impedances of each active output as resistors and inductors in parallel. For resistors of equal value in parallel, the formula for the net resistance is R/n, where R is the output impedance of each transistor, and n is the number of resistors. Therefore, as more outputs switch at the same time, the output resistance is reduced and more ground bounce will be generated.

Again, it is very difficult to model this effect so we will rely on empirical results for our analysis. Figure 6 illustrates the effect of increasing the number of outputs switching at the same time. We can see that as the number goes up, the amplitude and duration of the ground bounce pulse also increases. Therefore, devices that have fewer outputs will have less ground bounce.



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FIGURE 6. Number of Outputs Switching

Figure 7 shows the ground bounce generated by an 'AC157 when three of the four outputs are switching with standard test loads. Here we see only 475 mV of noise on the worst-case pin (pin furthest from the ground pin). This amplitude of ground bounce is not what we would expect in an actual system. As we will discuss later, a test fixture lumped load creates much more ground bounce than distributed system loads.

#### OUTPUT LOAD

The type and value of the output loading is one of the major variables that affect the amplitude of the ground bounce. Figures 8, 9 and 10 show the effects of varying the load capacitance in a standard test fixture.

In Figure 8, the ground bounce amplitude peaks for a load capacitance of approximately 60-70 pF, and then drops off as the capacitance is increased. This drop off is caused by the filtering effect of the larger capacitors.

For Figure 9, only the load capacitors on the active outputs were varied. The load on the quiet output was maintained at 50 pF. The amplitude of the ground bounce amplitude increased with increased capacitive loading. However, the slope of the curve drops off as the capacitance increases. This is due to the amount of energy that is discharged from the capacitor during the time that the output transistor is turning on.

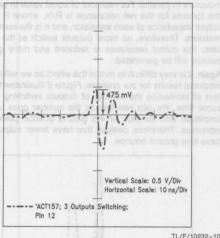
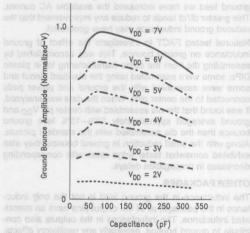


FIGURE 7. 'AC157 Quiet Output Noise

Smaller capacitors contain less energy than larger capacitors, and therefore, a larger change in the voltage across them will occur during the time that the output is turning on. Because of this, the size of the capacitance tends to limit the maximum amount of current sinking throughout the output and therefore, the amount of ground bounce. Larger capacitors, however, do not experience such a large change in voltage as the outputs turn on. For very large capacitances, there is almost no change in the voltage across them, and they behave much like a power supply. Under these conditions, the maximum amount of current that will sink through the outputs is limited by the outputs themselves. Increasing the capacitance does not increase the ground bounce.

Figure 10 shows the effect of varying only the capacitive loading on the active output. Here, the filtering effect of the load can be observed clearly. As the load capacitance is increased, it filters the signal and reduces the amplitude of the ground bounce.

Because they generate more AC current during switching, capacitive loads tend to generate more ground bounce noise than resistive loads. Fortunately, most actual PCB traces will be long enough so that they react like an impedance and not lumped capacitive loads.



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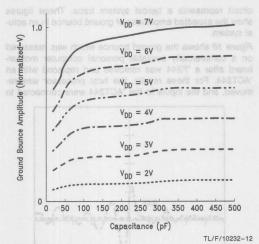
Quiet Output Switching Using 'AC241

7 Outputs Driving Lumped Capacitive Loads

Monitoring Pin 18.

FIGURE 8. Quiet Output Noise vs Capacitive Loading





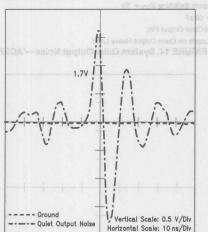
Quiet Output Switching with 'AC241

7 Outputs Driving Lumped Capacitive Loads

Monitoring Pin 18

# FIGURE 9. Fixed Quiet Load

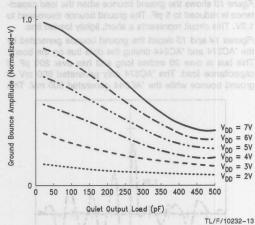
Figure 11 displays ground bounce when the device is loaded with standard 50 pF/500 $\Omega$  test loads. Each load was connected directly to the output pin. Under these conditions, which are considered worst case, the measured ground bounce amplitude was 1.7V.



7 Outputs Switching  $V_{DD} = 5V$  $C_L = 50 pF$ 

Worst-Case Output Pin

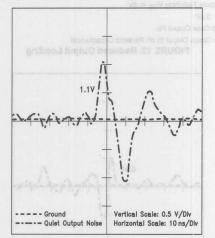
FIGURE 11. Standard Test Fixture



Ground Bounce Varying Quiet Output Load Only Other 7 Loads are Standard 5000/50 pF

# FIGURE 10. Fixed Active Load

Figure 12 illustrates what happens when the test load is moved away from the device output. A standard test load was connected to the output via 15 inches of circuit trace. The amplitude of the ground bounce was reduced to 1.1V. While this loading is closer to an actual system trace than a test load, it still generates more ground bounce noise because of the lumped load that is still on the line.



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7 Outputs Switching V<sub>DD</sub> = 5V  $C_L = 50 pF$ 

Worst-Case Output Pin

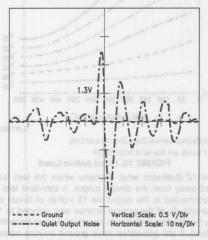
15" PCB Trace Separating Load from Device

FIGURE 12. Test Fixture Emulating **Transmission Line Effect** 

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Figure 13 shows the ground bounce when the load capacitance is reduced to 5 pF. The ground bounce decreased to 1.3V. This circuit represents a short, lightly loaded line.

Figures 14 and 15 depict the ground bounce generated by the 'AC374 and 'AC244 driving the data bus on the board. This bus is over 30 inches long and has over 200 pF of capacitance load. The 'AC374 only generated 600 mV of ground bounce while the 'AC244 generated 500 mV. This



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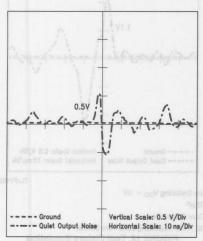
7 Outputs Switching  $V_{DD} = 5V$ 

 $C_L = 5 pF$ 

Worst-Case Output Pin

Open Circuit Output (5 pF Parasitic Capacitance)

FIGURE 13. Reduced Output Loading



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7 Outputs Switching  $V_{DD} = 5V$ 

 $C_L = 50 pF$ 

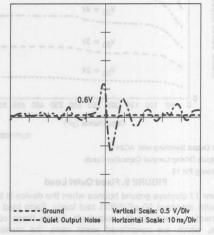
Worst-Case Output Pin;

Ten Loads on Quiet Output Heavy Load

FIGURE 15. System Quiet Output Noise—'AC244

circuit represents a typical system trace. These figures show the expected amplitudes of ground bounce in an actual system.

Figure 16 shows the ground bounce which was measured on a commercially available personal computer mother-board after a 'F244 was removed and replaced with an 'ACT244. For these results, the host processor was removed, and the inputs to the 'ACT244 were connected to



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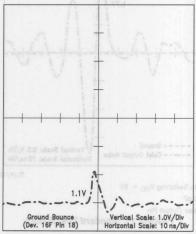
7 Outputs Switching  $V_{DD} = 5V$ 

 $C_L = 50 pF$ 

Worst-Case Output Pin;

Ten Loads on Quiet Output Heavy Load

FIGURE 14. System Quiet Output Noise—'AC374



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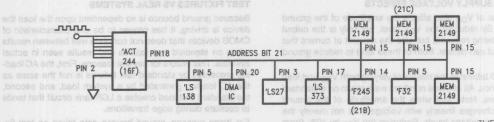
7 Outputs Switching V<sub>DD</sub> = 5V

 $C_L = 50 pF$ 

Worst-Case Output Pin

'AC244 Driving 10 Distributed Loads on an Unterminated Address Bus FIGURE 16. Quiet Output Noise in

Personal Computer Application

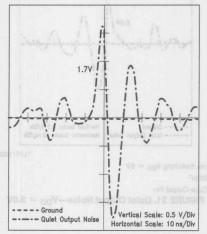


- Commercial PC Address Bus
- Approximately 50 pF Capacitance Loading
- Replaced 'F244 with 'ACT244
- With 7 Outputs Switching, Quiet Output Noise = 1.1V

# FIGURE 17. PC Circuit Diagram and control better self-based on so sented

the board clock source. The logic diagram for this line is represented in *Figure 17*. An address bus driver was chosen because of the length of the line and the number of loads on it. Here, the ground bounce amplitude was 1.1V. We can see that this signal line is connected to devices of many different technologies and functions, including LS and memory products. After the host processor was replaced, the system exhibited no performance degradation due to the device replacement.

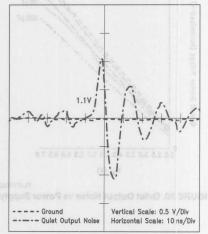
It can be seen from the previous figures that the type and location of the output loads have a major effect on ground bounce. It is also obvious that standard test loads generate the most ground bounce. Even reducing the capacitive load, or moving it away from the output still generates more noise than a typical application.



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# OUTPUT PIN LOCATION

The location of the output pin with respect to the device ground also affects the magnitude of ground bounce. Tests have shown that outputs located closer to the ground lead generally have 30% to 50% less noise than pins further away. The effects of pin location are portrayed in *Figures 18* and 19. *Figure 18* shows the ground bounce on the worst-case pin, which is the one farthest away from ground. *Figure 19* shows the ground bounce on the best-case pin, the one closest to ground. By choosing outputs close to ground, the amount of ground bounce may be reduced by nearly half.



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7 Outputs Switching  $V_{DD} = 5V$  $C_L = 50 \text{ pF}$ 

> FIGURE 19. Quiet Output Noise— Best-Case Output Pin (Pin 9)

7 Output Switching  $V_{DD} = 5V$  $C_{L} = 50 \text{ pF}$ 

CL = 50 pr

Standard Test Setup

FIGURE 18. Quiet Output Noise— Worst-Case Output Pin

## POWER SUPPLY VOLTAGE EFFECTS

The value of  $V_{DD}$  also affects the amplitude of the ground bounce. By reducing the  $V_{DD}$  level, not only is the output voltage swing reduced, but also the amount of current that the output can deliver. Both of these tend to reduce ground bounce

Figure 20 tabulates the results of varying both  $V_{DD}$  and load capacitance. All of these numbers were taken on a standard test fixture. Note that while the amplitude of the ground bounce changes linearly with voltage, it is not merely the ratio of the voltage levels. Reducing the  $V_{DD}$  by 40% (from 5.0V to 3.0V) reduces the ground bounce by almost 60%. Since the amplitude of the ground bounce decreases faster than the input threshold, there is a net gain in the noise margin.

Figure 21 represents the same results taken on the ground bounce demo board. The ground bounce was measured with  $V_{DD}=3.0$ V. The amount of ground bounce was reduced to 800 mV, even with standard test loads. It should be pointed out that 'ACXXX devices can be used in a 5V TTL system with a  $V_{DD}$  of  $3.3V\pm0.3$ V. Under these conditions, the outputs will still drive an incident wave on a 75 $\Omega$  transmission line for the commercial temperature range and  $100\Omega$  for the military temperature range. With  $V_{DD}$  equal to 3.3V, FACT 'ACXXX devices have TTL-compatible inputs and outputs.

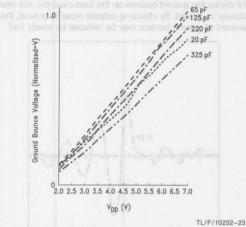


FIGURE 20. Quiet Output Noise vs Power Supply

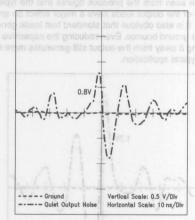
# **TEST FIXTURES VS REAL SYSTEMS**

Because ground bounce is so dependent upon the load the device is driving, it has proven to be one characteristic of CMOS devices that does not correlate well between results taken on standard test fixtures and results seen in actual systems. This occurs for several reasons. First, the AC loading presented by standard text fixtures is not the same as the AC loading generated by a system load, and second, the standard test load creates a LCR tank circuit that tends to oscillate during edge transitions.

For these reasons, ground bounce data taken on test fixtures is useful for comparative analysis, but is not valid for predicting actual system performance.

# **AC LOADING EFFECTS**

Standard text fixtures use 50 pF of capacitance and  $500\Omega$  of resistance to simulate a "typical load," as shown in Figure 22. It is possible to achieve good correlation between propagation delay data taken using these test loads and data taken in real systems. Unfortunately, this is not true for ground bounce. While this lumped load testing was adequate for older, slower technologies, it is not as useful for the newer, faster logic families. As edge rates go up, more and more circuit traces react like transmission lines, not lumped loads. For devices having edge rates of approximately 3 ns, traces longer than 6–8 inches will exhibit transmission line characteristics and cannot be treated as lumped loads.

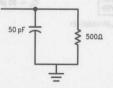


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7 Outputs Switching  $V_{DD} = 5V$  $C_L = 50 \text{ pF}$ 

Worst-Case Output Pin

FIGURE 21. Quiet Output Noise—V<sub>DD</sub> = 3.0V

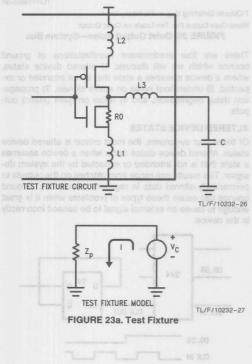


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FIGURE 22. Standard Test Load

Figures 23a and 23b are models of a capacitive load and a transmission line load, respectively. In Figure 23a, we replace the capacitor with a power supply. This simulates our circuit at the time when the output transistor has just turned on, and the full capacitor voltage is applied across the device. In Figure 23b, the transmission line is replaced with a resistor to the power supply. This simulates the AC characteristics of the transmission line.

Comparing the two figures, we notice that while the capacitive load applies the full voltage directly to the device output, the transmission line acts like an additional resistance between the voltage and the device output. Clearly, one would expect more current to flow with the capacitive load than with the resistive load. Since the output transistor turns on just as fast in both cases, the capacitive load will create a greater dl/dt, causing more voltage to be induced across the ground lead inductance. Because of this, standard test fixtures tend to generate two to three times more ground bounce noise than system printed circuit traces. This is still true for traces that may have more capacitance than the 50 pF lumped load used in standard test fixtures.



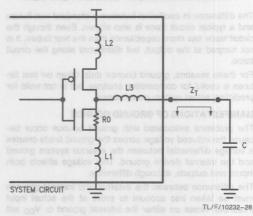
#### LCR TANK EFFECTS

Referring back to *Figure 1a*, notice the LCR tank circuit that is formed by the load capacitance, parasitic inductances and output resistance. Imagine each edge transition as a single impulse into this tank circuit; it would be expected to oscillate. Theoretically, the frequency of the oscillation should be somewhere in the range around 1.3 GHz. Typically, oscillations are observed in the frequency range of 100 MHz to 200 MHz. There are several reasons for this discrepancy.

The output transistor does not behave like a pure resistance. The transistor tends to limit the available current to less than 160 mA to 180 mA. Additionally, there are other parasitic elements associated with the output transistor affecting the frequency of oscillation.

Because most circuit traces react like impedances and not capacitances, this type of oscillation is not seen when FACT devices drive typical circuit traces.

Figures 22 and 23 highlight the differences between ground bounce in a standard test fixture and in a comparable PCB trace. The results of the test fixture (Figure 24) are much greater than the results of the PCB circuit trace (Figure 25). This is due to the greater current requirements caused by the lumped capacitive load versus a distributed load.



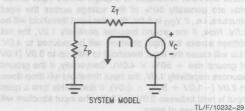
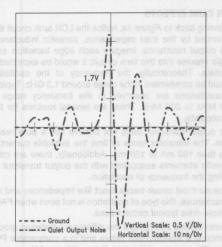


FIGURE 23b. System Models



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7 Outputs Switching  $V_{DD} = 5V$   $C_L = 50 pF$ 

Worst Case Output Pin; Ten Loads on Quiet Output

# FIGURE 24. Quiet Output—Standard Test Fixture

The difference in oscillation between a standard test fixture and a typical circuit trace is also shown. Even though the circuit trace has more capacitance than the test fixture, it is not lumped at the output, but distributed along the circuit trace.

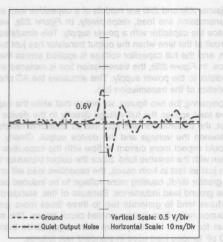
For these reasons, ground bounce data taken on test fixtures is useful for comparative analysis, but is not valid for predicting actual system performance.

# MANIFESTATIONS OF GROUND BOUNCE

The problems associated with ground bounce occur because the induced voltage across the ground leads creates a voltage differential between the external system ground and the internal device ground. This voltage affects both inputs and outputs, although differently.

The difference between the external and internal grounds must be taken into account to arrive at the actual input threshold. Noise on either the internal ground or  $V_{DD}$  will cause the input thresholds to change. CMOS input thresholds are generally 50% of the voltage across the input structure, i.e., if  $V_{DD}$  is 5.0V, then the input threshold will be 2.5V. Now, if the ground bounces positively 1.0V, the net voltage across the input structure will be reduced to 4.0V. This will cause the input threshold to shift up to 3.0V (1.0V of ground rise  $\pm$  50%  $\times$  4.0V). Conversely, if the ground bounces negatively 1.0V, the input threshold will drop down to 2.0V (-1.0V  $\pm$  50%  $\times$  6.0V). If during this time a quiet input is held between 2.0V and 3.0V, the input structure will detect a change of state.

Regarding the outputs, the effect is somewhat different. Any output that is LOW is essentially tied to the internal ground through a very low impedance: approximately  $10-12\Omega$ . Therefore, any output will tend to follow the internal ground as it shifts with respect to the external ground. This causes any LOW outputs to also shift with respect to external ground.



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7 Outputs Switching V<sub>DD</sub> = 5V; Heavy Load

Worst-Case Output Pin; Ten Loads on Quiet Output

# FIGURE 25. Quiet Output Noise—System Bus

There are four predominant manifestations of ground bounce which we will discuss: 1) altered device states, where a device assumes a state that is not intended or expected, 2) undershoot noise on active signals, 3) propagation delay degradation, and 4) noise on quiet (static) outputs.

#### ALTERED DEVICE STATES

Of these four symptoms, the most critical is altered device states. Altered device states occur when a device assumes a state that is not intended or expected by the system designer. The results can range from glitches on the outputs to permanently-altered data in registers or counters. Ground bounce can cause these types of problems when it is great enough to cause an external signal to be sensed incorrectly in the device.

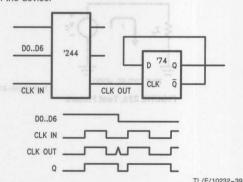


FIGURE 26. Example of Ground Bounce

In CMOS devices, the input thresholds are generally a percentage of the voltage across the input structure. Generally, the input levels are 50% for CMOS level inputs and 30% for TTL-level inputs. As the internal ground and power levels shift with respect to the external power and ground planes, the input thresholds will also shift. If the shift is great enough to cause the input threshold to go above an external HIGH signal (so that the input signal looks LOW) or below an external LOW signal (so that the input looks HIGH), the input will detect a change of state. Depending upon the input type, several results can occur.

If the input is a synchronous one, such as the data input into a D-type flip-flop, then the device should not be affected. If the input is combinatorial, or the data input to a transparent latch, the output may glitch.

The effects may be more damaging if the input is asynchronous, such as a clock, preset, set, load, or clear. With these inputs, data in the internal counters or registers may be corrupted. Most likely, this type of data corruption can usually cause a system to fail, or generate invalid results.

FACT devices are characterized during initial device evaluation to ensure that the device will not exhibit this problem.

## PROPAGATION DELAY DEGRADATION

Propagation delay degradation is a phenomenon familiar to most system designers. As more than one output on a single device is switched, the propagation delay, as measured to the input threshold level, will become longer. To understand how this happens with CMOS devices, consider Figure 27; any voltage developed across the inductor L1 will reduce the voltage across the output impedance R1. This, in turn reduces the current through R1. Since the rate of voltage change across the load capacitance is directly related to the current available, a decrease in current reduces the rate at which the output voltage changes, i.e., the edge rate slows down. This, in turn, slows down the propagation delay because more time is required for the output to go from one rail to the input threshold. As additional outputs are switching simultaneously, the voltage across the inductor increases, and the current available to charge or discharge the load capacitance will be less.

L2

V<sub>GB</sub>

L1

V<sub>GB</sub>

V

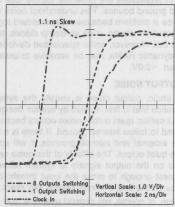
FIGURE 27. Output Model

Figure 28 illustrates the effects of multiple output switching on the propagation delay of a FACT device. Here we see that as more outputs switch, the edge rate of those outputs drops off.

While it is not possible to test this type of parameter in an ATE environment, National understands its importance to system designers. Since this type of measurement can be made in a bench environment, FACT devices are evaluated during initial device characterization to insure that this propagation delay degradation is less than 250 ps per additional output switched.

# **UNDERSHOOT ON ACTIVE SIGNALS**

Undershoot noise on active signals is generally created by impedance mismatches in transmission lines. Yet, it can also be created by ground bounce. Figure 29 shows the voltage that is generated across the inductor during the edge transition. While at the beginning of the transition the ground bounce is positive, at the end it is negative. This is due to the currents turning off as the output reaches the end of its voltage swing.



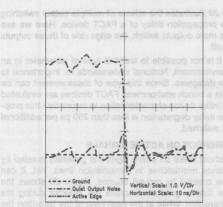
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# FIGURE 28. Propagation Delay vs Superpose Number of Outputs Switching

Unfortunately, the negative ground bounce occurs when the output is finishing its transition. The output will follow the internal ground as a quiet output would. This results in the output undershooting and then returning to ground.

2

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# FIGURE 29. Quiet Output Noise Concurrent with Active Edge

Undershoot amplitudes are generally slightly less than the associated ground bounce. This undershoot noise will generally not be a problem because most standard logic families have input structures, such as clamp diodes, that tend to damp it out. However, some specialized devices, exemplified by dynamic RAMs, may be sensitive to undershoots greater than -2.0V.

#### QUIET OUTPUT NOISE

Quiet, or static, output noise is usually the symptom of ground bounce that is first noticed by system designers. As pointed out earlier, quiet output noise occurs because LOW outputs tend to follow internal ground. If there is a shift between the external and internal grounds, it will appear as noise on a quiet output. The effects of this noise can range from noise on the output signals to system failure. If the noise is great enough to cross the input threshold on the next device on the line, this next device may react.

The reaction, of course, will depend upon the type of input. If the input is synchronous, the ground bounce noise will not propagate through the input into the device. If the input is combinatorial or asynchronous, output glitches or corrupted counters or registers may result. In order to predict the effects of this noise, it is necessary to consider some typical applications.

As shown earlier, ground bounce amplitude is dependent upon the number of outputs switching. Therefore, devices which have fewer outputs will have less noise. Because of this, our discussions will be limited to octal devices and their applications.

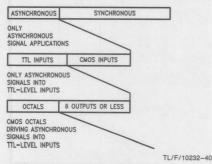


FIGURE 30. Application Segments

#### SYNCHRONOUS DATA/ADDRESS BUSSES

One of the largest application segments for octal devices is driving/receiving data and address busses. In these bus applications, the receiver is usually synchronous and latches in the data on a clock edge. In *Figure 29*, notice that the quiet output noise exists only when the active outputs are switching. In addition, both quiet and active outputs achieve this stable and valid state within the propagation delay time specified in the FACT Data Book.

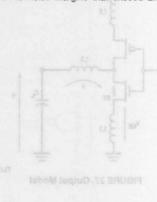
During the time that the data or address is latched in (when the data is expected to remain stable and valid) the quiet outputs are as stable and valid as the active outputs. Therefore, valid data will always be clocked in, and in these systems, no additional work is required to achieve maximum system performance and reliability.

## **ASYNCHRONOUS CONTROL LINES**

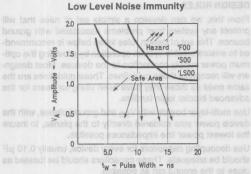
A much smaller application segment is driving asynchronous signals. Octal devices, like the '240 series, offer eight buffers in a 20-pin package. This feature can be useful to the system designer trying to reduce board size and part count. It is in these applications that problems are most likely to occur. However, there are several factors that work in the designer's favor.

It is important to look at the type of input that is being driven. CMOS-level inputs have much greater low noise margins than TTL-level inputs. Standard CMOS inputs have input thresholds set to 50% of  $V_{\rm DD}.$  This means that if  $V_{\rm DD}$  equals 5.0V, there is 2.5V of low noise margin. Test results show that the ground bounce will never be this great in a system. In addition, as noted above, the actual ground bounce noise expected in a real system is less than the AC noise margins of most TTL families.

Finally, it is very important to note that the duration of the ground bounce noise spike is short (tyically 2–3 ns @ 0.8V). Typically, AC noise margins increase with decreasing pulse width. This is more pronounced in slower technologies. Figure 31 shows the typical low level input noise thresholds of FAST, Schottky, and Low Power Schottky. For pulse width typically seen with ground bounce noise, the AC noise margins of FAST and Schottky approach 2.0V and 1.5V respectively. Even LS devices, which have the lowest input thresholds, have AC noise margins that exceed 2.0V for pulse







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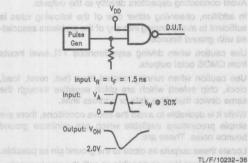


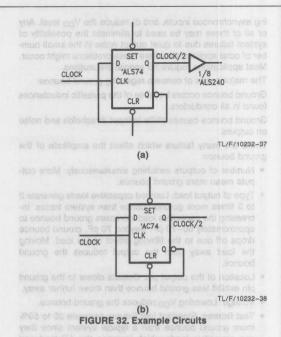
FIGURE 31. AC Noise Thresholds

widths as great as 8 ns. For ground bounce type noise pulses, with widths of 2-3 ns, the LS AC thresholds are well above 2.0V.

There are also several design techniques under the system designer's control which can be used to minimize ground bounce noise, thereby eliminating ground bounce-induced problems.

The first factor that should be considered, in many cases, is that the need for a buffer can be eliminated. This is due to the fact that all FACT logic devices feature the same 24 mA output stages. A quick example will help to clarify this. For the example, a divide-by-2 clock generator drives a clock onto a large processor board. Figure 32a shows the circuit built with ALS devices while Figure 32b shows the same circuit built with FACT devices. The difference is obvious: the ALS circuit required a buffer to drive the clock line because the 'ALS74 does not have enough output drive to drive the line. On the other hand the 'AC74 has the same drive capability as the 'AC240, so adding the buffer is redundant. In addition, the output of the 'AC74 is double buffered to isolate the internal logic from noise on the outputs. Removing an additional propagation delay gains performance advantages besides board space and part count savings. If it is not possible to remove the buffer, the designer can still insure minimum noise on the output. This can be accomplished with several methods, some of which are discussed

Board-level timing analysis may show that not all of the outputs can switch at the same time. Under these conditions, the worst-case ground bounce will be reduced (Figure 6). As



mentioned earlier, outputs closer to the ground pin may have up to 50% less noise than outputs further away. Therefore, asynchronous lines should be driven from outputs closer to the device ground pin whenever possible.

Some other methods, which may be more difficult to implement, include reducing the power supply voltage or using two power supply voltages. Running the system  $V_{\rm DD}$  lower (closer to 4.5V) will reduce the ground bounce noise levels of the CMOS devices while not affecting the input thresholds of the TTL devices. In addition, as we stated earlier, the  $V_{\rm DD}$  value for the CMOS devices can be lowered to 3.3V. This reduces the ground bounce by 60% while maintaining TTL-compatible inputs and outputs. For a small number of CMOS devices, a standard zener diode regulated circuit may be used. For larger numbers of devices, a second (3.3V) power plane may be added.

Take a moment to summarize the material covered thus far. While at first glance, the problems associated with quiet output noise may seem to be the most precarious to system designers, there are many issues that affect them. First, a large percentage of the octal applications are synchronous busses. In these applications, quiet output noise will not be a problem.

It is the smaller segment of asynchronous applications that are most suspect. Fortunately, only octal devices generate enough ground bounce noise to be of serious concern. Secondly, if the inputs are CMOS, the input noise margins are greater than any ground bounce. If the inputs are TTL, the ground bounce will generally be less than the TTL AC input noise margins. Additionally, designers have several techniques available to reduce the ground bounce. These include: a) use logic devices that provide buffer-type drive capability, thereby eliminating the need for these octal buffers (all FACT devices have the same 24 mA outputs); b) do not have all of the outputs on an octal device switch simultaneously; c) select outputs closer to the ground pin for drive

ing asynchronous inputs, and d) reduce the  $V_{DD}$  level. Any or all of these may be used to eliminate the possibility of system failures due to quiet output noise in the small number of octal applications where these problems might occur. Most applications require no special precautions.

The major points of concern regarding ground bounce:

Ground bounce occurs because of the parasitic inductances found in all conductors.

Ground bounce causes shifts in input thresholds and noise on outputs.

There are many factors which affect the amplitude of the ground bounce:

- Number of outputs switching simultaneously: More outputs mean more ground bounce.
- Type of output load: Lumped capacitive loads generate 2 to 3 times more gorund bounce than system traces. Increasing the capacitive load increases ground bounce to approximately 60–70 pF. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: Outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: Lowering VDD reduces the ground bounce.
- Test fixtures: Standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are characterized not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise: FACT's worst case quiet output noise has been measured to be around 500-1100 mV in real system applications.

# DESIGN RULES I MANUAL MODERN SERVED WOOD

From this, we can develop a simple set of rules that will protect any system from problems associated with ground bounce. This set of design rules listed below is recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines. These guidelines are the same ones as those they have been using for years for the advanced bipolar logic families.

Use multi-layer boards with  $V_{DD}$  and ground planes, with the device power pins soldered directly to the planes, to insure the lowest power line impedances possible.

Use decoupling capacitors for every device, usually 0.10  $\mu$ F should be adequate. These capacitors should be located as close to the ground pin as possible.

Avoid using sockets or wirewrap boards.

Avoid connecting capacitors directly to the outputs.

In addition, observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce.

Use caution when driving asynchronous TTL-level inputs from CMOS octal outputs.

Use caution when running control lines (set, reset, load, clock, chip select) which are glitch sensitive through the same device that drive data or address lines.

While it is desirable to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

Locate these outputs as close to the ground pin as possible.

Use the lowest  $V_{\mbox{\scriptsize DD}}$  as possible or split the power supply.

Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Ground bounce is an unwanted noise source that is found in most logic families available today. Due to increased edge rates and voltage swings, ground bounce can be more of a problem with new Advanced CMOS logic families. National, with the vast experience in high performance logic design gained from its leadership position with the FAST family, defined FACT logic so that high performance problems, as exemplified by ground bounce, were minimized while not sacrificing performance. By following the simple design guidelines outlined, designers can use FACT logic to maximize system performance while ensuring their systems are free from the problems associated with ground bounce.

# Dynamic Threshold for Advanced CMOS Logic

# INTRODUCTION

Most users of digital logic are quite familiar with the threshold specifications found on family logic data sheets. Designers using products with TTL level input thresholds will see numbers like V<sub>IH</sub> = 2.0V and V<sub>IL</sub> = 0.8V. These threshold guarantees are static, a part's response to these levels during switching transients can be undesirable. Through the course of this paper the reader should gain an understanding for the difference between a static threshold and a dynamic threshold. This paper will also discuss how various products respond dynamically, how dynamic thresholds are tested, and specified. Lastly, this paper will look at how FACT Quiet Series™ has addressed and specified dynamic threshold characteristics.

# WHAT IS A DYNAMIC THRESHOLD?

If National Semiconductor were able to package its I.C.'s in "ideal" packages, then dynamic and static thresholds would be one and the same. However, our package, like that of all our competitors, is not "ideal" and has a finite amount of inductance associated with each signal lead. As will be shown later, it is the inductance in the power leads which are the primary cause for the non-ideality.

To understand the phenomena of dynamic thresholds the properties of ground bounce must first be examined. Figure 1 is a representation for a 74XX00 product which includes package inductance. Figure 2a shows an output pulldown making an HL/ZL transition. In discharging the load capacitor a current I<sub>C</sub> equaling C\*dv/dt flows into the chip, this current is approximated versus time in Figure 2b. The changing current, I<sub>C</sub>, generates a voltage across the ground inductor represented in Figure 2c through the equation L\*di/dt. It is the voltage across the ground inductor, commonly known as ground bounce, which is the cause for static and dynamic thresholds to differ.

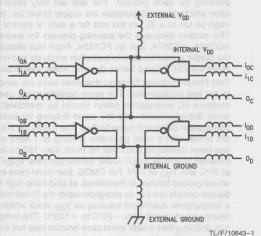
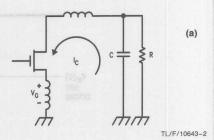


FIGURE 1. A Typical "00" 2-Input Quad NAND Gate

National Semiconductor Application Note 680 Ray Mentzer





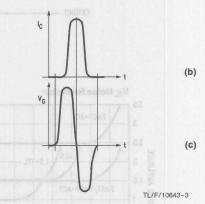
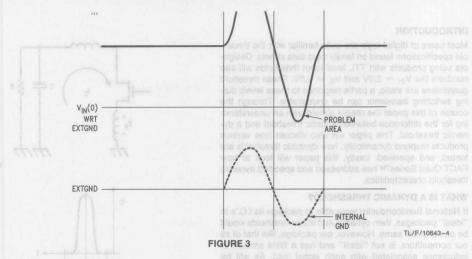
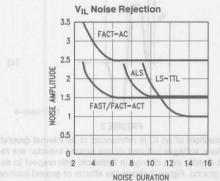


FIGURE 2

The threshold of an IC is referenced to its internal ground. Therefore, voltages induced on the ground inductor are reflected directly as a change in threshold with respect to external ground. Figure 3 shows the effects of ground bounce on an input threshold. If when the threshold is moving it crosses the input voltage levels, a problem area exists. However, having the threshold cross the input level does not necessarily induce a product failure. The threshold must cross the input level for a period of time for a false switch to occur. (Figure 4 shows the voltage time relationship). Note that in the high speed technologies two things have come together, faster delays and output edge rates, generally meaning larger di/dt's, and an ability to react to narrower pulses.





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In the example discussed above, ground bounce was outlined as the cause for the threshold change. For bipolar TTL technologies, this is the only noise source of concern since the threshold is created by a VBE stack referenced to ground. As Vnn changes in a bipolar circuit, the threshold will change logarithmically as the currents in the transistors change, i.e., a 1V change in VDD creates approximately a 34 mV shift in threshold. CMOS thresholds are set up as a percentage of VDD and track linearly with VDD changes. Therefore, a noise spike on VDD from an LH/ZH transition generates dynamic threshold characteristics which must be considered along with those of the HL/ZL edges. In this example let internal ground bounce to a 1V peak; the bipolar threshold will peak to approximately 2.5V while the CMOS circuit will peak to ((Vth/VDD\*(VDD - Vbounce) + 1.0V) = ((0.3\*(4.0) + 1.0) = 2.2V. Consider a negative bounce of 1V on the internal VDD bus, the threshold delta for the bipolar product will be negligible, but the CMOS chip's threshold will change as follows: ((Vth/VDD\*(VDD - $V_{\text{bounce}}) = (0.3*(4)) = 1.2V.$ 

# HOW ARE DYNAMIC THRESHOLDS SPECIFIED?

A circuits dynamic threshold characteristics are quantified with the specifications  $V_{IHD}$  and  $V_{ILD}$ , where the "D" appendage stands for "dynamic". The definitions are as below,

- V<sub>IHD</sub>— The minimum HIGH input level such that normal switching/functional characteristics are observed during output transients.
- V<sub>ILD</sub>— The maximum LOW input level such that normal switching/functional characteristics are observed during output transients.

#### HOW ARE DYNAMIC THRESHOLDS CHARACTERIZED?

The characterization of dynamic thresholds requires some planning for each product. The test will vary depending upon which edge will generate the supply noise; i.e., is the edge an LH or a ZL? Is the test for a data or control pin? This section discusses the planning process for testing an ACQ244, ACQ374, and an FCT534. From this discussion the reader should be able to test other products and understand the FACT Quiet Series dynamic noise specifications.

Test Fixturing/Setup: Dynamic threshold tests are sensitive to the test configuration. The same considerations used to measure AC propagation delays should be exercised. National Semiconductor uses the same fixturing for both AC propagation delay and noise testing. The inputs for this test are driven with a word generator running at 1 MHz which has been deskewed such that no more than 150 ps exists between channels. FACT Quiet Series specifies  $V_{\rm IHD}/V_{\rm ILD}$  at 25°C with  $V_{\rm DD}$  at 5.0V. For CMOS, true worst case exists where ground bounce is maximized, at cold temp high  $V_{\rm DD}$  alpolar circuits are not as straightforward; the threshold has a temperature coefficient tracking its  $V_{\rm BE}$  stack which can change nearly a volt from  $-55^{\circ}{\rm C}$  to  $+125^{\circ}{\rm C}$ . The temperature and  $V_{\rm DD}$  that create worst case bounce may not induce worst case  $V_{\rm IHD}/V_{\rm ILD}$ .

transitions.

The algorithm for this test is as follows. Maximize the number of outputs switching, N, in this case 8. N - 1 of the inputs will be transitioning to and from nonthreshold levels, 0V–3V. The last input will transition from 3V to  $V_{ILD}$  or from 0V to  $V_{IHD}$ . Figure 5 shows the four combinations of tests. It should be noted that values of  $V_{ILD}$  and  $V_{IHD}$  that induce failure will vary as a function of the test pin. This is due mostly to voltage drops on the internal power bussing. As a result, pins farthest from the ground pin, and sometimes the  $V_{CC}$  pin, are likely to be worst case pins.

Case 2: Product = ACTQ244 test data pins with ZL/ZH transitions.

This test will ramp the enable pin from 3V–0V while holding the input under test at threshold, i.e., have all outputs transitioning ZL, with N-1 inputs at 0V and the input under test at VI<sub>LD</sub>. The other tests are as follows, N-1 transitioning ZL pin under test (PUT) at VI<sub>HD</sub>, all outs going ZH PUT at VI<sub>HD</sub>, and N-1 a ZH switch and PUT at VI<sub>LD</sub>.

Case 3: Product = ACTQ244 test OE pin with HL/LH transitions.

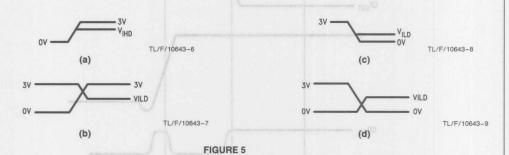
 $V_{ILD}$  is the parameter to check here. Data inputs should be switching 0V–3V while the OE pin is being stepped up from 0V to  $V_{ILD}$ . While testing the OE pin with an LH output tran-

by the device. With standard AC loading, their transients are much less than those of the other edges. Therefore,  $V_{IHD}$  for the chip is guaranteed by the data pins.

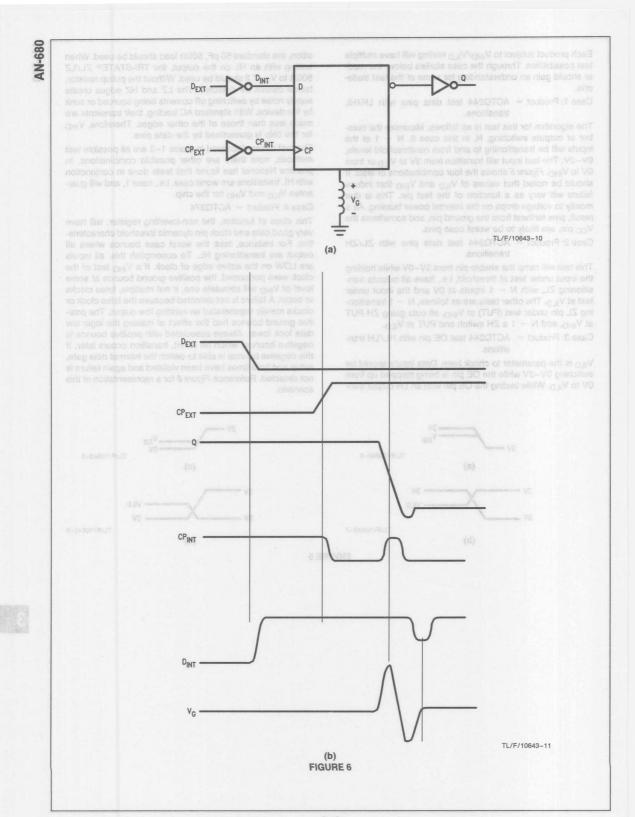
The test cases discussed in cases 1–3 are all possible test methods, note there are other possible combinations. In practice National has found that tests done in conjunction with HL transitions are worst case, i.e., case 1, and will guarantee  $V_{\rm IID}$  and  $V_{\rm IHD}$  for the chip.

Case 4: Product = ACTQ374

This class of function, the non-inverting register, will have very good data and clock pin dynamic threshold characteristics. For instance, take the worst case bounce where all output are transitioning HL. To accomplish this, all inputs are LOW on the active edge of clock. If a VIHD test of the clock were performed, the positive ground bounce at some level of VIHD will stimulate one, if not multiple, false clocks to occur. A failure is not detected because the false clock or clocks merely regenerated an existing low output. The positive ground bounce had the effect of making the logic low data look lower. Always associated with positive bounce is negative bounce, which on an HL transition occurs later. If this negative bounce is able to switch the internal data gate, setup and hold times have been violated and again failure is not detected. Reference Figure 6 for a representation of this scenario.



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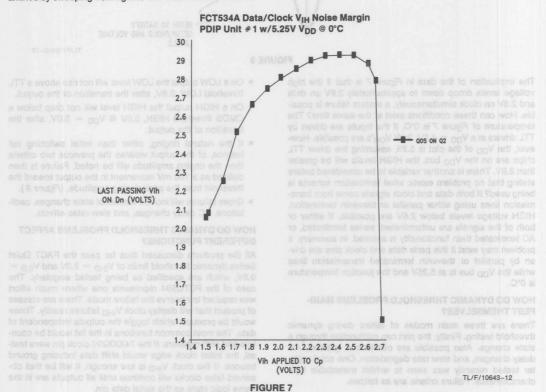


Case 5: Product = FCTQ534

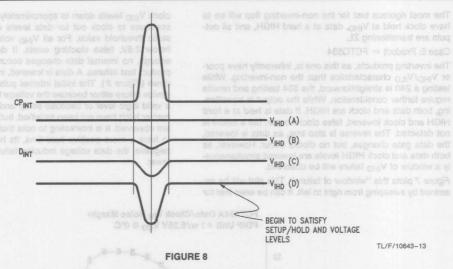
The inverting products, as this one is, inherently have poorer  $V_{IHD}/V_{ILD}$  characteristics than the non-inverting. While testing a 240 is straightforward, the 534 testing and results require further consideration. While the output is transitioning, both data and clock are HIGH. If data is held at a hard HIGH and clock lowered, false clocks occur, but a failure is not detected. The reverse is also true, as data is lowered, the data gate changes, but no clocks occur. However, as both data and clock HIGH levels are lowered simultaneously a window of  $V_{\rm IHD}$  failure will be observed.

Figure 7 plots this "window of failure". This plot will be examined by sweeping from right to left. It can be seen that for

clock V<sub>IHD</sub> levels down to approximately 2.6V, proper data continues to clock out for data levels down to 1.5V, the static threshold value. For all V<sub>IHD</sub> voltages of the clock below 2.6V, false clocking exists. If data is raised high enough, no internal data changes occur and therefore no product test failures. A data is lowered, internal data pulses down (*Figure 8*). The initial internal pulses may not cause device failure either because the voltage has not dropped to a valid logic level or because setup and hold times to the master latch have not been satisified, but eventually failures are observed. It is interesting to note that were the FCT534 to have a more positive hold time, its hold time is slightly lower.



3



The implication of the data in Figure 7 is that if the high voltage levels droop down to approximately 2.9V on data and 2.6V on clock simultaneously, a system failure is possible. How can these conditions exist at the same time? The temperature of Figure 7 is 0°C, if the inputs are driven by TTL drivers at a V<sub>DD</sub> = 4.5V, 2.6V V<sub>OH</sub>'s are possible. However, the VDD of the plot is 5.25, assuming the driver TTL chips are on the VDD bus, the HIGH levels will be greater than 2.6V. There is another variable to be considered before stating that no problem exists: what termination scheme is being used? If both data and clock signals come from transmission lines using either parallel or thevenin termination, HIGH voltage levels below 2.6V are possible. If either or both of the signals are unterminated, series terminated, or AC terminated then functionality is assured. In summary, a problem may exist if this parts data and clock pins are driven by parallel or thevenin terminated transmission lines while the V<sub>DD</sub> bus is at 5.25V and the junction temperature is 0°C.

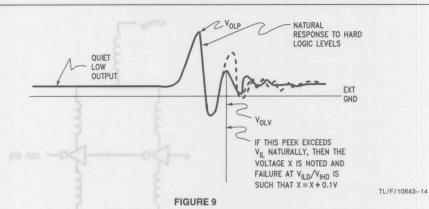
# HOW DO DYNAMIC THRESHOLD PROBLEMS MANIFEST THEMSELVES?

There are three main modes of failure during dynamic threshold testing. Firstly, the part can malfunction through a state change. Also possible are oscillations, glitches, AC delay changes, and slew rate degradation. One octal register tested recently was seen to exhibit metastable type characteristics. Failure criteria are as follows.

- On a LOW output the LOW level will not rise above a TTL threshold LOW, 0.8V, after the transition of the output.
- On a HIGH output the HIGH level will not drop below a CMOS threshold HIGH, 3.5V @ V<sub>DD</sub> = 5.0V, after the transition of the output.
- If the natural ringing, other than initial switching rail bounce, of the output violates the previous two criteria then the ringing amplitude will be noted. Failure is then defined as a 100 mV movement in the output toward the threshold from the peak ringing amplitude, (Figure 9).
- Gross failures will include functional state changes, oscillations, AC delay changes, and slew rates effects.

# HOW DO DYNAMIC THRESHOLD PROBLEMS AFFECT DIFFERENT FUNCTIONS?

All the products discussed thus far pass the FACT Quiet Series dynamic threshold limits of  $V_{IHD}=2.2V$  and  $V_{ILD}=0.8V$ , which are specified as being tested singularly. The case of the FCTQ534 represents one where much effort was required to observe the failure mode. There are classes of product that will display clock  $V_{IHD}$  failures readily. These would be products which toggle the outputs independent of data. The most common functions in the list would be counters and shift registers. If the 74XXX299 clock pin were tested, the initial clock edge would shift data inducing ground bounce. If the clock  $V_{IHD}$  is low enough, it will be that observed false clocks will continue until all outputs are in the same logic state as the serial data pin.



# WHAT DOES FACT QUIET SERIES DO TO ADDRESS DYNAMIC THRESHOLDS?

The Quiet Series product utilizes two technical innovations to accomplish its performance. First, by using a split ground bus configuration, input and output grounds are given a degree of isolation. Schematically this is shown in Figures 10a and b. The ground bus for inputs stages and outputs sections are separated on chip and only connected by the common inductance near the shoulder of the package and a mutual inductance between the leadframe fingers. Note, the V<sub>DD</sub> input and output V<sub>DD</sub> busses are electrically shorted on chip by the substrate resistance. The leadframe inductance forms a voltage divider such that the input only sees a percentage of the output ground noise. Secondly, a proprietary GTOTM technology, shown in Figure 10c, is used to shape the output edge. This then yields an output voltage waveform shown in Figure 10d. The soft turn on of the output attenuates the dv/dt, and therefore the di/dt presented to the ground inductance, yielding a reduction in the ground noise.

# HOW DOES NATIONAL COMPARE WITH OTHER VENDORS?

The characteristics of National Semiconductor's FACT Quiet Series ensure superior dynamic threshold performance in conventional corner pinned packaging. The split power rail technology used to isolate inputs and outputs addresses a noise issue which goes unresolved in multiple power pin ACL logic families, and most single pin families. The same split rail technology is used in the FACT FCT and FCTA logic lines. Referencing the FCT534 already discussed, Figure 11 shows one of the dramatic differences created by the Quiet Series technology.

# SUMMARY

With the new advanced CMOS technologies, the specifications and characteristics for dynamic thresholds need to be considered along with the other variables that impact the choice of a device type or family. This applications note has discussed the theories of test philosophy, failure criteria, and the root causes of dynamic thresholds. This information should provide the systems designer the tools to analyze any impact to design performance.





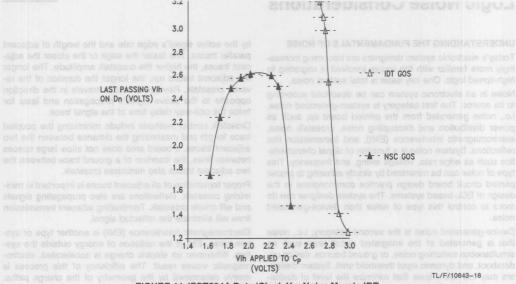


FIGURE 11. 'FCT534A Data/Clock V<sub>IH</sub> Noise Margin IDT
#5 (PDIP) vs NSC #2 (CDIP) 5.0V V<sub>DD</sub> @ Room

# **Design Innovations Address Advanced CMOS Logic Noise Considerations**

National Semiconductor Application Note 690 Michael L. Gilbert



## UNDERSTANDING THE FUNDAMENTALS OF NOISE

Today's electronic system designers are becoming increasingly more familiar with the issues involved in migrating to high-speed logic. One key issue is total system noise.

Noise in an electronic system can be described according to its source. The first category is system-generated noise, i.e., noise generated from the printed board up, such as power distribution and decoupling noise, crosstalk noise, electromagnetic interference (EMI), and transmission line reflections. System noise is a function of signal characteristics such as edge rate, voltage swing, and frequency. This type of noise can be minimized by strictly adhering to proper printed circuit board design practice commonplace in the design of ECL-based systems. The system designer can do more to control this type of noise than device-generated

Device-generated noise is the second category, i.e., noise that is generated at the integrated circuit level such as simultaneous switching noise, or ground bounce, device undershoot, and dynamic input threshold shift. System designers may use techniques that minimize the level of devicegenerated noise. Device-generated noise is more effectively minimized by the IC designer and manufacturer. In some asynchronous applications, such as the distribution of timing signals, use of inherently lower-noise ICs can be critical.

# **CONTROLLING SYSTEM-GENERATED NOISE IS CRITICAL**

The power distribution network is a key source of system noise. High-performance logic switches large amounts of current in a short amount of time and almost always requires multiple-plane printed circuit boards with separate power and ground planes instead of traces. Due to their high impedance, power and ground traces may generate too large of a power supply droop for low noise systems.

In addition, the logic's switching-current demand also requires bypass capacitors for each device, located as close to power or ground pin as possible. Usually a 0.1 µF ceramic chip capacitor provides adequate decoupling. Including power supply decoupling at every step of the system design is critical for a high-performance, low-noise system. Power supply noise is easily coupled and radiated throughout the system.

Crosstalk is another system noise. If not addressed during system design, it can create problems in high-performance systems. Crosstalk refers to the noise created when a signal on an "active" trace is coupled onto an adjacent parallel "quiet" signal trace.

Forward crosstalk manifests itself as a negative voltage spike on the adjacent quiet trace and results from mutual inductance effects. Its amplitude and duration are generally much less than reverse crosstalk. Reverse crosstalk is noise on the quiet trace resulting from a combination of capacitively-coupled and mutually-induced energy from the active signal trace. Its amplitude and duration are determined by the active signal's edge rate and the length of adjacent parallel traces. The faster the edge or the closer the adjacent traces, the higher the crosstalk amplitude. The longer the adjacent traces run, the longer the duration of the reverse crosstalk. Reverse crosstalk travels in the direction opposite to the active signal's propagation and lasts for twice the one-way delay time of the signal trace.

Crosstalk control methods include minimizing the coupled trace length and maximizing the distance between the two adjacent traces. If board area does not allow large spaces between lines, the insertion of a ground trace between the two adjacent traces also minimizes crosstalk.

Proper termination of all adjacent traces is important in minimizing crosstalk. Reflections are also propagating signals and will create crosstalk. Terminating adjacent transmission lines will eliminate the reflected signal.

Electromagnetic Interference (EMI) is another type of system noise. EMI is the radiation of energy outside the system. Whenever an electric charge is accelerated, electromagnetic waves result. The efficiency of this process is mainly determined by the geometry of the charge paths. The most significant charge paths in a system are the printed circuit board signal traces, power supplies, and I/O cables. The largest and most plentiful charge paths, they are also leading sources of EMI.

The EMI bandwidth is a function of the signal frequency, amplitude, edge rate, duty cycle, edge discontinuity, and ringing. These characteristics of high-performance logic, especially advanced CMOS logic, can cause signal traces and I/O cables to radiate more noise than ever before. The higher frequencies generated as a result of these characteristics will radiate more efficiently from signal lines because of their shorter wavelengths.

Addressing the characteristics of a signal that may create EMI is critical to reducing EMI, or achieving electromagnetic compatibility (EMC). Reliable solutions to EMC include proper shielding and grounding of all cables as well as proper termination of all signal traces. Adhering to other system design guidelines for power supply decoupling and crosstalk can also minimize EMI. Some of the output edge control techniques discussed later will also minimize EMI by directly effecting several key signal characteristics.

The last major form system noise is reflections on the transmission line and the resultant ringing. Ringing observed on signal traces has two sources: one is system-generated; the other, device-generated. The two are often confused. It is important to note that improperly terminated transmission lines will create ringing caused by reflections, i.e., systemgenerated noise.

Reflections are caused by mismatches in impedance from driver to transmission line or from transmission line to receiver/termination. The magnitude of these reflections is related to the length of the transmission line and the impedance along the line. Transmission line impedances and driver/receiver I/O impedances seldom match. Most often these impedances are orders of magnitude different. With the edge rates of today's advanced CMOS logic, transmission lines of approximately 20 centimeters (8 inches) or longer will most probably need some type of termination.

Choosing the right termination scheme is important. When designing with low-power advanced CMOS, do not select a termination that will dissipate several tens of milliamperes. Popular bipolar terminations such as a DC parallel termination (resistor to ground) or a Thevenin (voltage divider) termination (resistors to both rails) draw large amounts of DC current. Effective termination schemes that preserve low CMOS power consumption are a series resistor (for a single driver/receiver pair) or an AC parallel termination (resistor in series with a capacitor to ground) for distributed multiple loads.

Device-generated ringing is due to the parasitic LCR tank circuits in the IC and its load. The stimulus for this type of ringing is an overshoot or undershoot in the output signal. This ringing is minimized by slowing the output edge rate with higher loads or by improvements in IC circuitry.

# WHAT IS DEVICE-GENERATED NOISE?

Device-generated noise includes dynamic threshold shift, ground bounce, and output undershoot.

The first type of device-generated noise is dynamic threshold shift. System designers are very familiar with DC input threshold requirements, namely  $V_{\rm IH}$  (Input Voltage HIGH) and  $V_{\rm IL}$  (Input Voltage LOW). For TTL-based logic, these levels are typically 2.0V and 0.8V, respectively. For CMOS-based logic, these levels are typically 70% and 30% of  $V_{\rm DD}$ , respectively and are measured and guaranteed in a static (DC) mode only. Switching any part of the device-under-test is an invalid condition. In a real-life situation the IC is dynamic and so are the input thresholds.

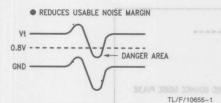


FIGURE 1. Dynamic Threshold

Dynamic input threshold shifts arise when one or several of the inputs are toggled, generating noise on the device's onchip power rails. The input threshold voltage is proportional to the power supply voltage. Any fluctuation of these rails, such as ground bounce and/or undershoot, will create fluctuations of the input threshold. Figure 1 illustrates a nega-

tive excursion on the internal ground of an IC. The input threshold tracks this excursion and crosses through the static LOW input level. This creates an unwanted change of state on the output when the threshold falls below the input level. In this case, an undershoot caused by bounce on the chip ground causes a normally valid input level to create an invalid output state.

Dynamic threshold shifts may create problems on synchronizing inputs should the device's output noise be great enough to cause the device's threshold voltage to shift across the input voltage level. On TTL-compatible inputs, dynamic threshold shifts could substantially reduce an already low noise margin.

In addition to causing erroneous changes in state, the output may begin to go into a high-frequency oscillation as input voltage levels approach the dynamic threshold. Regardless of whether the input in question is a synchronizing input, this high frequency oscillation will increase chip heating. Should this situation continue, device reliability could be effected.

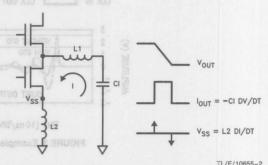


FIGURE 2. Ground Bounce Model

The second type of device-generated noise is ground bounce or simultaneous switching noise. Ground bounce or  $V_{OLP}$  (Voltage Output LOW, Peak) and undershoot or  $V_{OLV}$  (Voltage Output LOW, Valley) are names given to noise levels associated with the output of a logic device. While these two issues are not new to logic, they are of greater concern with advanced logic families. Since advanced CMOS outputs switch rail to rail at high speed and into heavy loads, performance and design concerns have risen in this area.

Similary,  $V_{DD}$  droop and overshoot are also device-generated noise issues. However, since both affect the logic HIGH level and since using CMOS outputs to drive TTL inputs provides much higher noise margin than the logic LOW level, this discussion focuses on low-level noise margin issues.

As the model in *Figure 2* illustrates, ground bounce is the voltage induced on the device ground inductance by current as it quickly discharges from a capacitive load, sinking into the output's N-channel transistor. The greater the amount and rate of discharge that is created by multiple simultaneously switching outputs, the greater the ground bounce level. Essentially there are more current sources sinking current into the same ground inductor.

Device undershoot or V<sub>OLV</sub> (Voltage Output LOW, Valley) is simply a function of the LCR tank circuit at the output. As edge rates increase, undershoot and subsequent ringing increase. Undershoot also decreases as the capacitive load

on the output increase and/or as the inductance of the output decreases. Therefore, advanced CMOS logic devices driving one or two other advanced CMOS logic devices will have more undershoot than an advanced CMOS device driving a heavily loaded bus. For this reason, in most systems undershoot levels are much less than those observed in test fixture environments. Also, improper bus termination may appear to worsen undershoot. In fact it is the energy of the reflected wave that increases the undershoot and not the device itself. Most undershoot levels in excess of 2.0V are the result of some mismatched impedance along the transmission line and can be eliminated with proper termination.

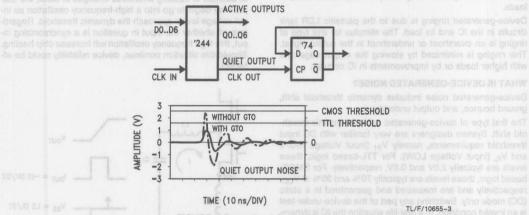


FIGURE 3. Example of Ground Bounce

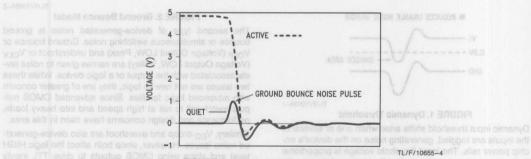
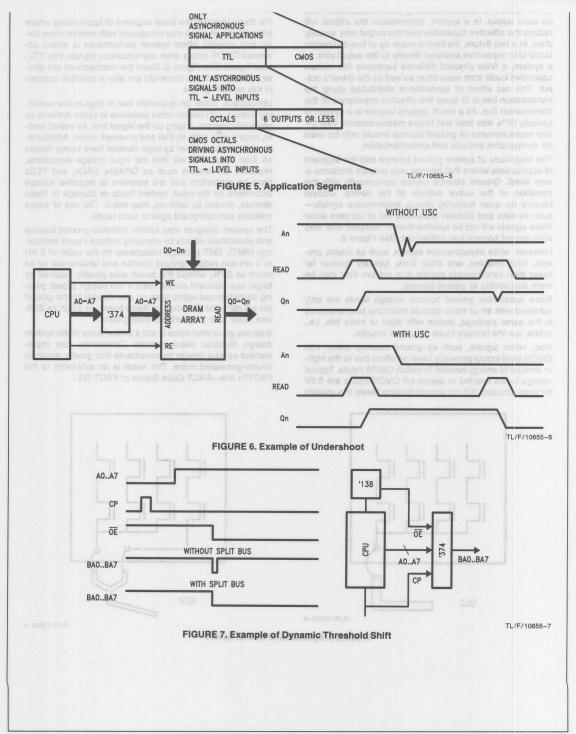


FIGURE 4. Location of Bounce Pulse





# WHERE CAN DEVICE-GENERATED NOISE AFFECT SYSTEM PERFORMANCE?

An integrated circuit ground inductor's di/dt is determined by the number of outputs switching and the capacitive load on each output. In a system, transmission line effects will reduce the effective capacitive load the output may actually drive. In a test fixture, the load is made up of low-dissipation factor chip capacitors soldered directly to the output pins. In a system, a finite physical distance separates the various capacitive loads from each other as well as the driver's output. The net effect of capacitance distributed along the transmission line is to lower the effective impedance of the transmission line. As a result, ground bounce in a system is typically 50% less than test fixture measurements. Test fixture measurements of ground bounce should only be used for comparative analysis and characterization.

The magnitude of system ground bounce and the segment of applications where that bounce may present problems is very small. Ground bounce occurs concurrently with the transition of the active outputs of the device. Ground bounce on quiet output(s) driving synchronous signals—such as data and address lines—are not of concern since these signals will not be synchronized or sampled until long after ground bounce has settled out. See *Figure 4*.

However, while asynchronous signals, such as resets, presets, latch enables, and clock lines, typically number far fewer than synchronous signals in a system they may be more susceptible to ground bounce.

Since substantial ground bounce voltage levels are only achieved with six or more outputs switching simultaneously in the same package, device with eight or more bits, i.e., octals, are the primary focus of ground bounce.

Also, noise signals, such as ground bounce, driven into CMOS-level inputs generally have no effect due to the higher amount of energy needed to switch CMOS inputs. Typical voltage levels needed to switch full CMOS inputs are 3.0V for approximately 2.0 ns; ground bounce levels in a system

or a test fixture do not reach this level. However, ground bounce on asynchronous signals into TTL-input levels may cause system errors. Typically TTL inputs need only 1.7V of noise of 2.0 ns to switch (e.g. FAST® and ALS).

For these reasons, the small segment of applications where ground bounce noise may compound with system noise levels and possibly affect system performance is where advanced CMOS octals drive asynchronous signals into TTL-level inputs. See *Figure 5*. Since the mechanisms are similar, shifts in dynamic threshold are also a possible concern in this small segment.

Undershoot, either on quiescent low or high-to-low switching outputs, can create noise problems in some systems by generating excess ringing on the signal line. As stated earlier, ringing also adds to EMI and crosstalk noise. Additionally, most devices driven by logic devices have clamp diodes on their inputs that will limit the input voltage excursions. However, as devices such as DRAMs, DACs, and PLDs have no protection and are sensitive to negative voltage excursions on the input, system faults or damage to these devices, caused by latch-up, may result. The use of series resistors can safeguard against such faults.

The system designer may further minimize ground bounce and undershoot effects by choosing surface mount technology (SMT). SMT package inductance on the order of 2 nH to 4 nH can reduce ground bounce and undershoot by as much as 25%, without the board area penalty incurred by larger non-standard pinout. Also, if the design allows, placing asynchronous signal lines on pins closest to the ground pin will minimize the noise on these lines—as much as 20% less noise than pins furthest from ground.

If device-generated noise is still a critical issue in the system design, National Semiconductor Corporation has implemented several design improvements that greatly minimize device-generated noise. The result is an extension to the FACTTM line—FACT Quiet Series or FACT QS.

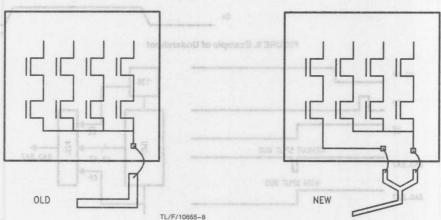


FIGURE 8. Split Ground Bus Structure

TL/F/10655-9

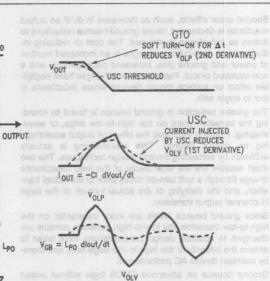


FIGURE 9. National Semiconductor's Proprietary Noise Control Circuitry

OUTPUT

TL/F/10655-10

# DESIGN INNOVATIONS RESOLVE DEVICE NOISE ISSUES

INPUT

FACT Quiet Series implements patented technological breakthroughs in device-generated noise suppression as well as several major performance improvements. Design improvements include a split ground bus and leadframe, a graduated output N-channel turn-on circuit, and an output undershoot correction circuit.

**USCTM** 

**GTOTM** 

UNDERSHOOT

UNDERSHOOT

FALLING EDGE LEVEL DETECTOR

SOFT TURN-ON TRANSISTORS

STAGES

INPUT/PREDRIVER

The first design improvement, a split ground bus and leadframe, addresses dynamic threshold shift. Since the cause of threshold shift is noise on the IC ground bus created by simultaneous output switching, separating the output and input ground buses virtually eliminates dynamic threshold shift.

FACT QS has separate on-chip ground buses for the input transistors and for the remainder of the internal gates, including the output transistors. FACT QS goes one step further to isolate output noise from the inputs by implementing a split leadframe for the ground pin. Figure 8 illustrates the change in the ground bus structure. Note that the split leadframe joins just prior to exiting the cavity. Standard pinout, package quality, and reliability are maintained using this technique.

Resulting from output noise, dynamic threshold shifts are worst-case under conditions of multiple simultaneously switching outputs. Values of dynamic thresholds on advanced CMOS without the split ground bus and leadframe range from 0.3V to 0.7V.

g is on the order of 2.0V to 3.0V Vot p in a test

The result of the split ground bus and leadframe is a dynamic threshold equivalent to the static threshold. For FACT ACTQ logic, typical dynamic threshold is 1.4V for a logic low. In this way, output switching noise becomes inconsequent to the input using split ground bussing. National Semiconductor's FACT QS, FACT FCT and FACT FCTA logic lines all incorporate split ground bus and leadframe improvements.

A second design improvement, a graduated output N-channel turn-on circuit (GTOTM), greatly reduces ground bounce. As Figure 2 illustrated, ground bounce is a function of the output waveshape, d²v/dt². Reducing package and chip inductance does have some effect in reducing ground bounce, but the reduction in ground bounce is not linear with inductance reduction. Package inductances may change by an order of magnitude, yet ground bounce is reduced only by as much as 25%.

Second order effects, such as increases in di/dt as output reactance is decreased, cause ground bounce reductions to flatten as inductance is reduced. The cost of reducing inductance on dual-in-line packages is an increased number of power and ground pins, increased package size, and a non-standard pinout. Package pinout changes have negligible effect on surface mount devices where inductance is low to begin with.

The greater reduction in ground bounce is found by rounding the transition point on the high-to-low edge, or wave-shaping. Figure 9 illustrates the effect of output waveshaping on ground bounce. This waveshaping is actually achieved by combining several design techniques. The two most notable are the slow decay of the load capacitance charge through a soft turn-on circuit prior to the actual transition, and the delaying of the actual turn-on of the large N-channel output transistor.

Since ground bounce levels are more substantial on the high-to-low transition, the low-to-high transition remains unchanged. In addition, design considerations were taken to ensure the integrity of the high-to-low edge rate, and thereby maintain device AC performance.

Ground bounce on advanced CMOS logic without output waveshaping is on the order of 2.0V to 3.0V  $V_{\rm OLP}$  in a test fixture environment. In the same environment, FACT QS, with the GTO circuitry, provides  $V_{\rm OLP}$  performance in the range of 1.0V to 1.3V. In a system, 30% to 50% lower  $V_{\rm OLP}s$  should result.

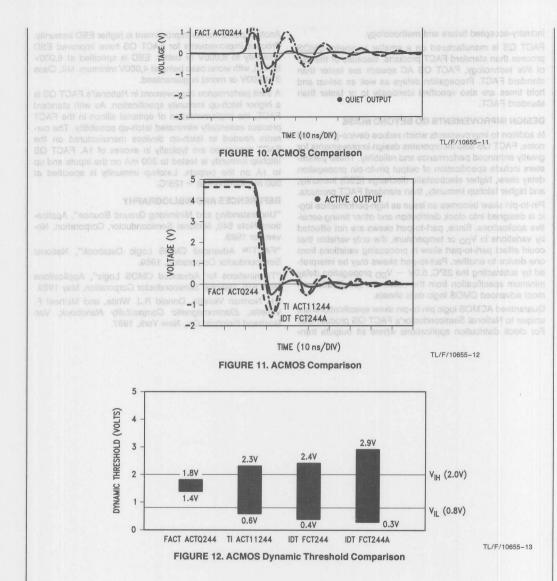
The third design improvement, undershoot corrector circuitry (USCTM), reduces output undershoot, both on the switching and quiescent (at ground) outputs. Undershoot is also a matter of di/dt. As output edge rates speed up and voltage swings increase, undershoot increases. Undershoot also increases as the number of simultaneously switching outputs increases. The result, V<sub>OLV</sub>, can be seen on both the switching edges as well as outputs quiescent at ground.

The undershoot correction circuit works by limiting negative di/dt excursions. The first part of this two-stage circuit senses a high-to-low edge. At a predetermined point on that edge, the undershoot corrector is turned on. The corrector simply activates a P-channel transistor which sources current into the output. This softens the di/dt that occurs when the load is depleted of charge. An internal RC timer controls the duration and decay of the correction.

Should the RC timer time out before undershoot is fully resolved, a differential amplifier, sensing that the output voltage is still below the input ground, keeps the current source turned on. This two-stage design is more reliable because of the time required for the current injector to turn on after the output goes negative.

Because USC operation is affected by package inductance, plastic DIP packages react differently than ceramic DIP packages. Similarly, surface mount devices have a different correction level. As ground bounce and undershoot decrease with decreasing inductance, the need for undershoot correction also decreases with decreasing inductance.





# OUTPUT CONTROL CIRCUITRY RESULTS IN LOWER NOISE

Figures 10 and 11 compare three major ACMOS product lines. These ACMOS manufacturers have different levels of noise suppression. All measurements were taken using an industry-accepted fixture and methodology.

FACT QS is manufactured on a smaller geometry CMOS process than standard FACT products. Because of the use of this technology, FACT QS AC speeds are faster than standard FACT. Propagation delays as well as set-up and hold times are also specified identically to or faster than standard FACT.

#### **DESIGN IMPROVEMENTS GO BEYOND NOISE**

In addition to improvements which reduce device-generated noise, FACT QS also incorporates design improvements for greatly enhanced performance and reliability. These parameters include specification of output pin-to-pin propagation delay skew, higher electrostatic discharge (ESD) immunity, and higher latchup immunity, than standard FACT products.

Pin-to-pin skew becomes an issue as high-performance logic is designed into clock distribution and other timing-sensitive applications. Since, part-to-part skews are not effected by variations in  $V_{\rm DD}$  or temperature, the only variable that could effect part-to-part skew is processing variations from one device to another. Part-to-part skews may be interpreted by subtracting the 25°C, 5.0V -  $V_{\rm DD}$  propagation delay minimum specification from the maximum specification on most advanced CMOS logic data sheets.

Guaranteed ACMOS logic pin-to-pin skew specifications are unique to National Semiconductor's FACT QS product line. For clock distribution applications where all outputs tran-

sition to the same state simultaneously, output skew is typically less than 500 ps, with worst case being 1.0 ns. For bus applications where outputs can transition to either state simultaneously, typical skew is less than 800 ps, with worst case being 1.0 ns.

Another performance improvement is higher ESD immunity. Process improvements for FACT QS have improved ESD immunity to 8,000V or better. ESD is specified at 6,000V typical, with worst case being at 4,000V minimum. MIL Class 3 (4,000V or more) is guaranteed.

A third performance improvement in National's FACT QS is a higher latch-up immunity specification. As with standard FACT, the implementation of epitaxial silicon in the FACT process essentially eliminated latch-up possibility. The currents needed to latch-up devices manufactured on the FACT processes are typically in excess of 1A. FACT QS latchup immunity is tested to 300 mA on the inputs and up to 1A on the outputs. Latchup immunity is specified at 300 mA minimum at  $\pm 125^{\circ}$ C.

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|         |  |

# 54AC/74AC00 • 54ACT/74ACT00 Quad 2-Input NAND Gate

#### **General Description**

The 'AC/'ACT00 contains four 2-input NAND gates.

#### **Features**

- Outputs source/sink 24 mA
- 'ACT00 has TTL-compatible inputs' → □ V
- Standard Military Drawing (SMD)
- 'AC00: 5962-87549
- 'ACT00: 5962-87699

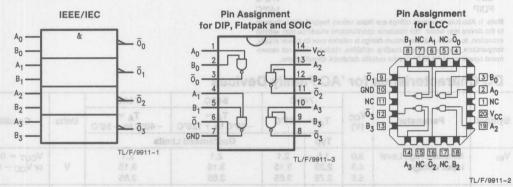
Ordering Code: See Section 8

# **Logic Symbol**

28 m/ /ms

# Connection Diagrams

DC V<sub>CC</sub> of Ground Current per Output Pin (Icc of IgNo)



| Your a Di   |     | 0.0                  |                      |     |                                      | V |
|---|-----|----------------------|----------------------|-----|--------------------------------------|---|
| Pin Nan   | nes | Description          |                      |     |                                      |   |
| $\frac{A_n, B_n}{\overline{O}_n}$                   | W   | Inputs<br>Outputs    |                      |     | Winimum High Level<br>Output Voltage |   |
| S1 5/8  |     |                      |                      | 5.5 |                                      |   |
| $V_{IIV} = V_{IIV}^*$ $V_{IOH} = -2$ $V_{IOH} = -2$ |     | 2.46<br>3.76<br>4.76 |                      |     |                                      |   |
| lour = 50 p   |     |                      |                      |     |                                      |   |
| JIA == NIA.   |     |                      |                      |     |                                      |   |
| lot 2   |     |                      | 88.0<br>88.0<br>88.0 |     |                                      |   |
| $V_1 = V_{CC}$ , $C$                                |     | ±1.0                 |                      |     |                                      |   |

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )         | -0.5V to $+7.0V$                |
|---|---------------------------------|
| DC Input Diode Current (I <sub>IK</sub> ) |                                 |
| $V_1 = -0.5V$                             | -20 mA                          |
| $V_I = V_{CC} + 0.5V$                     | + 20 mA                         |
| DC Input Voltage (V <sub>I</sub> )        | $-0.5V$ to $V_{CC} + 0.5V$      |
| DC Output Diode Current (IOK              | Features (                      |
| $V_O = -0.5V$                             | AS Mais source emp-20 mA        |
| $V_O = V_{CC} + 0.5V$                     | tagenoo-JVT and oo +20 mA       |
| DC Output Voltage (Vo)                    | $-0.5$ V to to $V_{CC} + 0.5$ V |
| DC Output Source                          | 'AC00: 5962-87549               |
| or Sink Current (IO)                      | ±50 mA                          |
| DC V <sub>CC</sub> or Ground Current      |                                 |
|   |                                 |

per Output Pin (ICC or IGND)

Storage Temperature (TSTG)

Junction Temperature (T<sub>J</sub>)

CDIP

PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

| Conditions   |                                   |
|--|-----------------------------------|
| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT   | 2.0V to 6.0V<br>4.5V to 5.5V      |
| Input Voltage (V <sub>I</sub> )  | 0V to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )   | OV to V <sub>CC</sub>             |
| Operating Temperature (T <sub>A</sub> ) 74AC/ACT 54AC/ACT  | -40°C to +85°C<br>-55°C to +125°C |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'AC Devices $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns                         |
| Minimum Input Edge Rate (ΔV/Δt)  |                                   |
| 'ACT Devices V <sub>IN</sub> from 0.8V to 2.0V V <sub>CC</sub> @ 4.5V, 5.5V  | 125 mV/ns                         |

### DC Characteristics for 'AC Family Devices

| Symbol  VIH  VIL  VOH |                                      | 384                    | 74                      | AC                   | 54AC                              | 74AC                            |       |   |  |
|-----------------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|---|--|
|                       | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |  |
|                       | STOUGHT                              |                        | Тур                     |                      | Guaranteed Lir                    | nits                            | _     | and the same of the   |  |
|                       | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | ٧     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>IL</sub>       | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | V se  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>       | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu A$   |  |
|                       |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | V     | $^{*} V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}} \\ -12 \text{ mA} \\ I_{\text{OH}} \qquad -24 \text{ mA} \\ -24 \text{ mA}$ |  |
| V <sub>OL</sub>       | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | ٧     | Ι <sub>ΟUT</sub> = 50 μΑ  |  |
|                       |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                 | 0.44<br>0.44<br>0.44            | V     | $^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ 12 mA $_{\text{IOL}}$ 24 mA $_{\text{24 mA}}$                                 |  |
| I <sub>IN</sub>       | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                              | ±1.0                            | μΑ    | $V_I = V_{CC}$ , GND  |  |

±50 mA

-65°C to +150°C

175°C

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

| Symbol       | Parameter 3                         | neter VCC (V) |       | + 25°C | -55°C to +125°C | -40°C to +85°C | Units | Conditions                               |  |
|--------------|-------------------------------------|---------------|-------|--------|-----------------|----------------|-------|--|--|
|              |                                     |               | Тур   | 30     | Guaranteed Li   | mits           |       |  |  |
| lold         | †Minimum Dynamic                    | 5.5           | KESWI | TEDM   | 50              | 75             | mA    | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD         | Output Current                      | 5.5           | 2.A   | 0.5    | -50             | -75            | mA    | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc<br>a.s.s | Maximum Quiescent<br>Supply Current | 5.5           | 9.0   | 4.0    | 0.8 80.08 8     | 40.0           | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

# DC Characteristics for 'ACT Family Devices

|                  | IA = -40°G                           |                        |                |              | 54ACT                             | 74ACT                           | neter             | Symbol Para   |
|------------------|--------------------------------------|------------------------|----------------|--------------|-----------------------------------|---------------------------------|-------------------|---|
| Symbol           | Parameter                            | V <sub>CC</sub><br>(V) |                |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units             | Conditions  |
| NPO              | 20 01                                |                        | Тур            | () F         | Guaranteed Li                     | mits                            | ing Date          | ansona Propaga  |
| V <sub>IH</sub>  | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5     | 2.0<br>2.0   | 0.7 2.0<br>2.0                    | 2.0<br>2.0                      | sie( <b>V</b> noi | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5     | 0.8          | 0.8<br>0.8                        | 0.8<br>0.8                      | V                 | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧                 | $I_{OUT} = -50 \mu\text{A}$   |
|                  | VO                                   | 4.5<br>5.5             | )V             | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | Pe<br>V Ce        | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧                 | I <sub>OUT</sub> = 50 μA  |
|                  |                                      | 4.5<br>5.5             |                | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | ٧                 | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     | 5.5                    |                | ±0.1         | ±1.0                              | ±1.0                            | μΑ                | $V_{I} = V_{CC}$ , GND  |
| ICCT             | Maximum<br>I <sub>CC</sub> /Input    |                        | 0.6            |              | 1.6                               | 1.5                             | mA                | $V_I = V_{CC} - 2.1V$   |
| I <sub>OLD</sub> | †Minimum Dynamic                     | 5.5                    |                |              | 50                                | 75                              | mA                | V <sub>OLD</sub> = 1.65V Max  |
| I <sub>OHD</sub> | Output Current                       | 5.5                    |                |              | -50                               | -75                             | mA                | V <sub>OHD</sub> = 3.85V Min  |
| lcc              | Maximum Quiescent<br>Supply Current  | 5.5                    |                | 4.0          | 80.0                              | 40.0                            | μΑ                | $V_{IN} = V_{CC}$ or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

# AC Electrical Characteristics: See Section 2 for waveforms OA 101 applications and OO

| Symbol           |                   | OAR               | 74AC       |  |            | 54AC |                         | 74AC       |                        |            |             |
|------------------|-------------------|-------------------|------------|--|------------|------|-------------------------|------------|------------------------|------------|-------------|
|                  | Parameter         | V <sub>CC</sub> * | 0.00       | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | to + | −55°C<br>125°C<br>50 pF | to +       | -40°C<br>85°C<br>50 pF | Units      | Fig.<br>No. |
| unit 1/32        |                   | - V Are 35        | Min        | Тур  | Max        | Min  | Max                     | Min        | Max                    | ulticher - |             |
| t <sub>PLH</sub> | Propagation Delay | 3.3<br>5.0        | 2.0        | 7.0<br>6.0                                       | 9.5<br>8.0 | 1.0  | 11.0<br>8.5             | 2.0<br>1.5 | 10.0<br>8.5            | ns         | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5 | 5.50.08<br>4.5                                   | 8.0<br>6.5 | 1.0  | 9.0<br>7.0              | 1.0        | 8.5<br>7.0             | ns         | 2-3,4       |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  | Parameter         |                   |  | 74ACT | v Devi | 54ACT  |     | 74ACT  |     | Chare | oa          |
|------------------|-------------------|-------------------|--|-------|--------|--|-----|--|-----|-------|-------------|
| Symbol           |                   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |        | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |     | Units | Fig.<br>No. |
|                  | 0                 | 0.38 + 01         | Min  | Тур   | Max    | Min  | Max | Min  | Max |       |             |
| t <sub>PLH</sub> | Propagation Delay | 5.0               | 1.5  | 5.5   | 9.0    | 1.0  | 9.5 | 1.0  | 9.5 | ns    | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay | 5.0               | 1.5  | 4.0   | 7.0    | 1.0  | 8.0 | 1.0  | 8.0 | ns    | 2-3,4       |

Voltage Range 5.0 is 5.0V ±0.5V

| Capacitanic           | C   |              | U.V  |       |        |                   |                                     |  |
|-----------------------|---|--------------|------|-------|--------|-------------------|-------------------------------------|--|
| Symbol                | ٧   | Parameter    | Тур  | Units | 94.4 C | onditio           | Minimum High Levisino               |  |
| C <sub>IN</sub>       | Input Capacitance Power Dissipation Capacitance |              | 4.5  | pF    | V      | CC = 5            | i.0V                                |  |
| Amas C <sub>PD</sub>  |   |              | 30.0 | pF8.€ | V      | <sub>CC</sub> = 5 | 5.0V                                |  |
|                       |   |              |      |       |        |                   |                                     |  |
|                       |   | 88,0<br>88,0 |      |       |        |                   |                                     |  |
|                       |   |              |      |       |        | 5.5               |                                     |  |
| $V_1 = V_{CO} - 2.1V$ |   | 1.6          |      |       |        |                   |                                     |  |
|                       |   |              |      |       |        |                   |                                     |  |
|                       |   |              |      |       |        |                   |                                     |  |
|                       |   |              |      | 0.4   |        |                   | Maximum Quiescent<br>Supply Current |  |



# 54AC/74AC02•54ACT/74ACT02 Quad 2-Input NOR Gate

#### **General Description**

The 'AC02/'ACT02 contains four, 2-input NOR gates.

The information on the ACT02 is Preliminary Information Only.

#### **Features**

- Outputs source/sink 24 mA
- 'ACT02 has TTL-compatible inputs 00 + 00 = 0V

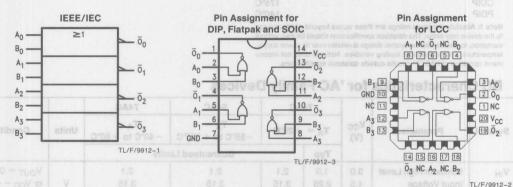
please contact the highenal Semiconductor Sales

Standard Military Drawing (SMD)

Ordering Code: See Section 8

#### **Logic Symbol**

#### **Connection Diagrams**



| Pin Names | Description | O.0 | O.

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| 011100, 210111241010 101 414111                       |   |
|---|---|
| Supply Voltage (V <sub>CC</sub> )                     | -0.5V to $+7.0V$  |
| DC Input Diode Current (I <sub>IK</sub> )             |   |
| $V_1 = -0.5V$   | -20 mA  |
| $V_1 = V_{CC} + 0.5V$                                 | + 20 mA   |
| DC Input Voltage (V <sub>I</sub> )                    | $-0.5$ V to $V_{CC} + 0.5$ V  |
| DC Output Diode Current (IOK)                         |   |
| $V_O = -0.5V$   | Am 02 - puls source/sink 2  |
| $V_O = V_{CC} + 0.5V_{Harmonical}$                    | ## 20 mA  |
| DC Output Voltage (Vo)                                |   |
| DC Output Source                                      |   |
| or Sink Current (I <sub>O</sub> )                     | ±50 mA  |
| DC V <sub>CC</sub> or Ground Current                  |   |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ± 50 mA   |
| Storage Temperature (TSTG)                            | -65°C to +150°C   |
|   | DC Input Diode Current ( $I_{IK}$ ) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ DC Input Voltage ( $V_I$ ) DC Output Diode Current ( $I_{OK}$ ) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage ( $V_O$ ) DC Output Voltage ( $V_O$ ) DC Output Source or Sink Current ( $I_O$ ) DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ ) |

PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Junction Temperature (T<sub>J</sub>)

CDIP

# Recommended Operating Conditions

V<sub>CC</sub> @ 4.5V, 5.5V

| Supply Voltage (V <sub>CC</sub> )               | Test Maddle Ser       |
|---|-----------------------|
| 'AC   | 2.0V to 6.0V          |
| 'ACT  | 4.5V to 5.5V          |
| Input Voltage (V <sub>I</sub> )                 | 0V to V <sub>CC</sub> |
| Output Voltage (V <sub>O</sub> )                | 0V to V <sub>CC</sub> |
| Operating Temperature (T <sub>A</sub> )         |                       |
| 74AC/ACT  | -40°C to +85°C        |
| 34AC/AC1  | 33 0 10 1 123 0       |
| Minimum Input Edge Rate (ΔV/Δt)                 |                       |
| 'AC Devices A SUCTOA and AS A                   |                       |
| 111   | Information Or        |
| V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V              | 125 mV/ns             |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |                       |
| 'ACT Devices                                    | Ordering              |
| V <sub>IN</sub> from 0.8V to 2.0V               |                       |

125 mV/ns

#### **DC Characteristics for 'AC Family Devices**

| SHED A          | TO KID                               | 386                    | 74                      | AC                   | 54AC                | 74AC                 |    | 82   |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|---------------------|----------------------|----|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) |                         |                      | Units               | Conditions           |    |  |
|                 |                                      |                        | Тур                     | Same ments           | Guaranteed Li       | mits                 |    |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85 | 2.1<br>3.15<br>3.85  | ٧  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65 | 0.9<br>1.35<br>1.65  | V  | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4   | 2.9<br>4.4<br>5.4    | V  | $I_{OUT} = -50 \mu\text{A}$  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7   | 2.46<br>3.76<br>4.76 | ٧  | $\label{eq:VIN} \begin{split} *V_{\text{IN}} &= V_{\text{IL}}  \text{or}  V_{\text{IH}} \\ &- 12  \text{mA} \\ I_{\text{OH}} &- 24  \text{mA} \\ &- 24  \text{mA} \end{split}$ |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1   | 0.1<br>0.1<br>0.1    | ٧  | Ι <sub>ΟUT</sub> = 50 μΑ   |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5   | 0.44<br>0.44<br>0.44 | ٧  | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                | ±1.0                 | μΑ | $V_{I} = V_{CC}$ , GND   |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

|                  | 7-62 0                              | 1.1 | -    |       |              | 1     | _  |  |
|------------------|-------------------------------------|-----|------|-------|--------------|-------|----|--|
|                  | 4d he = 10                          |     | Тур  | 10    | Guaranteed L | imits |    |  |
| I <sub>OLD</sub> | †Minimum Dynamic                    | 5.5 | AGDA | 71100 | 50           | 75    | mA | V <sub>OLD</sub> = 1.65V Max             |
| IOHD             | Output Current                      | 5.5 | 0,5  | 1.0   | -50          | -75   | mA | V <sub>OHD</sub> = 3.85V Min             |
| lcc              | Maximum Quiescent<br>Supply Current | 5.5 | 8.0  | 4.0   | 80.0         | 40.0  | μА | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### DC Characteristics for 'ACT Family Devices

|                 | 3/04=V                               |                        | IA = +25 G     |              | 54ACT                             | 74ACT                                |        | Symbol Pera  |
|-----------------|--------------------------------------|------------------------|----------------|--------------|-----------------------------------|--------------------------------------|--------|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) |                |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = V<br>-40°C to +85°C | Units  | Conditions   |
| A 0.0           |                                      |                        | Тур            |              | Guaranteed Li                     |                                      |        |  |
| VIH             | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5            | 2.0          | 2.0<br>2.0                        | 2.0                                  | V no   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5     | 0.8          | 0.8<br>0.8                        | 0.8<br>0.8                           | ٧      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                           | ٧      | $I_{OUT} = -50 \mu\text{A}$  |
|                 | V0.                                  | 4.5<br>5.5             | v I            | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                         | Payers | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                           | ٧      | $I_{OUT} = 50 \mu\text{A}$   |
|                 |                                      | 4.5<br>5.5             |                | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                         | V      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                | ±0.1         | ±1.0                              | ±1.0                                 | μА     | V <sub>I</sub> = V <sub>CC</sub> , GND   |
| Ісст            | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6            |              | 1.6                               | 1.5                                  | mA     | $V_I = V_{CC} - 2.1V$  |
| IOLD            | †Minimum Dynamic                     | 5.5                    |                |              | 50                                | 75                                   | mA     | V <sub>OLD</sub> = 1.65V Max   |
| IOHD            | Output Current                       | 5.5                    |                |              | -50                               | -75                                  | mA     | V <sub>OHD</sub> = 3.85V Min   |
| lcc             | Maximum Quiescent<br>Supply Current  | 5.5                    |                | 4.0          | 80.0                              | 40.0                                 | μА     | V <sub>IN</sub> = V <sub>CC</sub><br>or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# AC Electrical Characteristics: See Section 2 for waveforms 3 0.4 101 and a harmonic and 0.00

|                  |                   | DAI                   | 7  | 74AC       |            | 54AC  |            | 74AC   |            |       |             |
|------------------|-------------------|-----------------------|--|------------|------------|---|------------|--|------------|-------|-------------|
| Symbol Parameter | Parameter         | V <sub>CC</sub> * (V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |            | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |            | Units | Fig.<br>No. |
|                  |                   |                       | Min  | Тур        | Max        | Min   | Max        | Min  | Max        |       |             |
| t <sub>PLH</sub> | Propagation Delay | 3.3<br>5.0            | 1.5<br>1.5                                       | 5.0<br>4.0 | 7.5<br>6.0 | 1.0   | 9.0<br>7.0 | 1.0  | 8.0<br>6.5 | ns    | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay | 3.3<br>5.0            | 1.5<br>1.5                                       | 5.0<br>4.5 | 7.5<br>6.5 | 1.0   | 9.0<br>7.5 | 1.0  | 8.0<br>7.0 | ns    | 2-3,4       |

\*Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  |                   |                   |  | 74ACT | veQ y | 54.  | ACT | 74/  | ACT  | Chan  | 00    |
|------------------|-------------------|-------------------|--|-------|-------|--|-----|--|------|-------|-------|
| Symbol           | Parameter         | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |       | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.  |
|                  |                   | C8 + C9           | Min  | Тур   | Max   | Min  | Max | Min  | Max  |       |       |
| t <sub>PLH</sub> | Propagation Delay | 5.0               | 1.0  | 6.0   | 8.5   |  | dh  | 1.0  | 9.0  | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay | 5.0               | 1.0  | 6.5   | 9.5   | 0.5  | 2.1 | 1.0  | 10.0 | ns    | 2-3,4 |

\*Voltage Range 5.0 is 5.0V ±0.5V

| Symbol                       | V       | Parameter               | Тур  | Units | 0 | onditi | ions lotto vivoruo |  |
|------------------------------|---------|-------------------------|------|-------|---|--------|--------------------|--|
| CIN                          | Input C | Capacitance             | 4.5  | pF    | V | cc =   |                    |  |
| C <sub>PD</sub>              | Power   | Dissipation Capacitance | 30.0 | pF    | V | cc =   | 5.0V               |  |
| Am 48- nor                   |         | 4.76                    | 4,70 | 4.80  |   | 8.8    |                    |  |
|                              |         |                         |      |       |   |        |                    |  |
|                              |         |                         |      |       |   |        |                    |  |
|                              |         |                         |      |       |   |        |                    |  |
| $V_1 = V_{OC} - 2.1V$        |         |                         |      |       |   |        |                    |  |
| VOLD = 1.66V Max             |         |                         |      |       |   |        | TMinimum Dynamic   |  |
| V <sub>OHD</sub> = 3.86V Min |         |                         |      |       |   |        | Output Current     |  |
|                              |         |                         |      |       |   |        | Maximum Quissoent  |  |



# 54AC/74AC04 • 54ACT/74ACT04 Hex Inverter

#### **General Description**

The 'AC/'ACT04 contains six inverters.

The information for the ACT04 is preliminary OA information only.

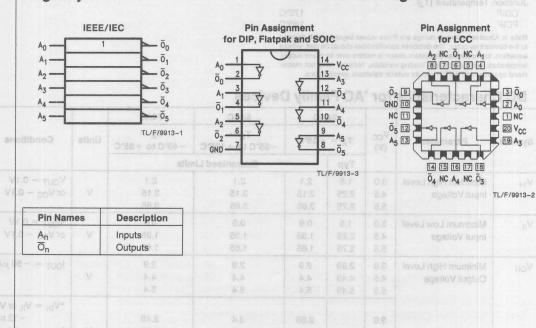
#### **Features**

- Outputs source/sink 24 mA
- 'ACT04 has TTL-compatible inputs
- Standard Military Drawing (SMD)
   'AC04: 5962–87609

Ordering Code: See Section 8

#### **Logic Symbol**

#### **Connection Diagrams**



#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

 $\begin{array}{lll} \text{Supply Voltage (V}_{CC}) & -0.5 \text{V to } +7.0 \text{V} \\ \text{DC Input Diode Current (I}_{IK}) & & & \\ V_I = -0.5 \text{V} & & -20 \text{ mA} \\ V_I = \text{V}_{CC} + 0.5 \text{V} & & +20 \text{ mA} \end{array}$ 

DC Input Voltage (V<sub>I</sub>) -0.5V to V<sub>CC</sub> + 0.5V DC Output Diode Current (I<sub>OK</sub>)

 $V_{O} = -0.5V$  -20 mA  $V_{O} = V_{CC} + 0.5V$  +20 mA DC Output Voltage ( $V_{O}$ ) -0.5V to to  $V_{CC} + 0.5V$ 

DC Output Source or Sink Current (I<sub>O</sub>)

DC V<sub>CC</sub> or Ground Current
per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±50 mA
Storage Temperature (T<sub>STG</sub>) -65°C to +150°C

Storage Temperature (T<sub>STG</sub>)
Junction Temperature (T<sub>J</sub>)

CDIP 175°C PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 'AC
 2.0V to 6.0V

 'ACT
 4.5V to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

 Output Voltage (V<sub>O</sub>)
 0V to V<sub>CC</sub>

Operating Temperature (T<sub>A</sub>)

74AC/ACT -40°C to +85°C -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> 4/100 Market V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices V<sub>IN</sub> from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

#### **DC Characteristics for 'AC Family Devices**

|                                | [ ]                                  | M                      | 74                      | AC                   | 54AC                              | 74AC                            |       | ]-4   |
|--------------------------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|---|
| Symbol                         | Parameter                            | V <sub>CC</sub><br>(V) |                         |                      | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |
|                                |                                      |                        | Тур                     | Legistimo            | Guaranteed Limits                 |                                 |       |   |
| V <sub>IH</sub><br>S=6168131.J | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |
| V <sub>IL</sub>                | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |
| V <sub>OH</sub>                | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu\text{A}$   |
|                                |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | ٧     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ $-24 \text{ mA}$ |
| V <sub>OL</sub>                | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | V     | $I_{OUT} = 50 \mu A$  |
|                                |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                 | 0.44<br>0.44<br>0.44            | V     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA                                  |
| I <sub>IN</sub>                | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                              | ±1.0                            | μА    | $V_{I} = V_{CC}$ , GND  |

±50 mA

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### 1

# DC Characteristics for 'AC Family Devices (Continued)

|                  | 74A.C                               |                     | 74                     | AC            | 54AC                              | 74AC                            |       |                              |  |
|------------------|-------------------------------------|---------------------|------------------------|---------------|-----------------------------------|---------------------------------|-------|------------------------------|--|
| Symbol Parameter | Parameter                           | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C |               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                   |  |
|                  |                                     | Тур                 | - 30                   | Guaranteed Li |                                   |                                 |       |                              |  |
| IOLD             | †Minimum Dynamic                    | 5.5                 | XSRI                   | 1996          | 50                                | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max |  |
| IOHD             | Output Current                      | 5.5                 | 0.11                   | 0.1           | -50                               | <b>-75</b>                      | mA    | V <sub>OHD</sub> = 3.85V Min |  |
| Icc<br>A,C-S     | Maximum Quiescent<br>Supply Current | 5.5                 | 10.0                   | 4.0           | 88 80.0                           | 40.0                            | μΑ    | $V_{IN} = V_{CC}$ or GND     |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

#### **DC Characteristics for 'ACT Family Devices**

|                  | D*00 - − 40°C                        |                        | 74                     | ACT          | 54ACT                             | 74ACT                           |           |  |  |
|------------------|--------------------------------------|------------------------|------------------------|--------------|-----------------------------------|---------------------------------|-----------|--|--|
| Symbol           | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions   |  |
|                  | n Max                                | in .                   | Тур                    | stille       | Guaranteed Li                     | mits                            |           |  |  |
| VIH              | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5             | 2.0          | 2.0 0.8<br>0.8 2.0 6.8            | 2.0                             | sieU no   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5             | 0.8          | 0.8<br>0.8                        | 0.8<br>0.8                      | V8.0 ± V0 | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧         | $I_{OUT} = -50 \mu\text{A}$  |  |
|                  | V                                    | 4.5<br>5.5             | oV<br>oV               | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    |           | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$                       |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001         | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧         | $I_{OUT} = 50 \mu A$   |  |
|                  |                                      | 4.5<br>5.5             |                        | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | V         | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     | 5.5                    | HI                     | ±0.1         | ±1.0                              | ±1.0                            | μА        | $V_I = V_{CC}$ , GND   |  |
| ГССТ             | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6                    |              | 1.6                               | 1.5                             | mA        | $V_I = V_{CC} - 2.1V$  |  |
| lold             | †Minimum Dynamic                     | 5.5                    |                        |              | 50                                | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub> | Output Current                       | 5.5                    |                        |              | -50                               | -75                             | mA        | V <sub>OHD</sub> = 3.85V Min   |  |
| lcc              | Maximum Quiescent<br>Supply Current  | 5.5                    |                        | 4.0          | 80.0                              | 40.0                            | μΑ        | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{CC}$  for 54ACT @ 25°C is identical to 74ACT @ 25°C.

# AC Electrical Characteristics: See Section 2 for waveforms 30 A 30 and an all all a section 2 for waveforms 30 A 30 and an all all a section 2 for waveforms 30 A 30 and an all all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and an all a section 2 for waveforms 30 A 30 and a section 3 A 30 and a 30 and a section 3 A 30 and a s

|                  |                   | DAI               | 74   | 74AC             |            | 54   | AC                      | 74   | AC                     |        |       |
|------------------|-------------------|-------------------|--|------------------|------------|------|-------------------------|------|------------------------|--------|-------|
| Symbol           | Parameter         | V <sub>CC</sub> * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |                  |            | to + | -55°C<br>125°C<br>50 pF | to + | -40°C<br>85°C<br>50 pF | Units  | Fig.  |
|                  |                   | 3                 | Min  | Тур              | Max        | Min  | Max                     | Min  | Max                    | ait to |       |
| <sup>t</sup> PLH | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5                                 | 4.5              | 9.0<br>7.0 | 1.0  | 11.0<br>8.5             | 1.0  | 10.0<br>7.5            | ns     | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay | 3.30.0<br>5.0     | 1.5<br>1.5                                 | 4.5 0 0 8<br>3.5 | 8.5<br>6.5 | 1.0  | 10.0<br>7.5             | 1.0  | 9.5<br>7.0             | ns     | 2-3,4 |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

#### AC Electrical Characteristics: See Section 2 for waveforms

|                       | Parameter<br>bns0 shirti |                   | 74ACT 54ACT |                                     |     | 74/  | ACT                     |  | 10 00 |       |             |
|-----------------------|--------------------------|-------------------|-------------|-------------------------------------|-----|------|-------------------------|--|-------|-------|-------------|
| Symbol                |                          | V <sub>CC</sub> * |             | A = +25°C<br>C <sub>L</sub> = 50 pF |     | to + | -55°C<br>125°C<br>50 pF | $T_A = -40^{\circ}C$<br>$to +85^{\circ}C$<br>$C_L = 50 pF$ |       | Units | Fig.<br>No. |
|                       |                          |                   | Min         | Тур                                 | Max | Min  | Max                     | Min  | Max   |       |             |
| t <sub>PLH</sub>      | Propagation Delay        | 5.0               | 1.0         | 6.0                                 | 8.5 | 0.0  | 2.1                     | 1.0  | 9.0   | ns    | 2-3,4       |
| t <sub>PHL</sub> VIIO | Propagation Delay        | 5.0               | 1.0         | 5.5 0.8                             | 8.0 | 0.6  | 8.1                     | 1.0  | 8.5   | ns    | 2-3,4       |

\*Voltage Range 5.0 is 5.0V  $\pm$  0.5V

| A. 03   - 1                                       |                               | A 3            | A A  | 3.5                | 233. 34             | . 31 N | Leve J doll-f muminité           |  |
|---|-------------------------------|----------------|------|--------------------|---------------------|--------|----------------------------------|--|
| Symbol  | V                             | Parameter      | Тур  | Units              | Co.                 | nditio |                                  |  |
| CIN/  | Inp                           | ut Capacitance | 4.5  | pF                 | Vo                  | C = 5. | ov                               |  |
| Am AS CPD HO!                                     | Power Dissipation Capacitance |                | 30.0 | pF <sub>aa</sub> , | V <sub>CC</sub> = 5 |        | ov                               |  |
| lour = 50 µA                                      | V                             | 0.1            | 1.0  | 1.0                | 100.0               | 4,5    | Maximum Low Level Output Voltage |  |
| $V_{HI}V = V_{HL} \text{ or } V_{HH}$ Am AS 24 mA |                               |                |      |                    |                     |        |                                  |  |
|   |                               |                |      |                    |                     |        |                                  |  |
|   |                               |                |      |                    |                     |        |                                  |  |
|   |                               |                |      |                    |                     |        |                                  |  |
|   |                               |                |      |                    |                     |        |                                  |  |
|   |                               |                |      |                    |                     |        |                                  |  |



# 54AC/74AC08 • 54ACT/74ACT08 Quad 2-Input AND Gate

#### **General Description**

The 'AC/'ACT08 contains four, 2-input AND gates.

The information for the ACT08 is preliminary information only.

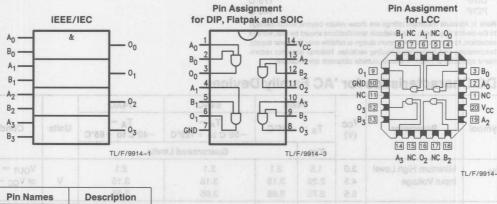
#### **Features**

- Outputs source/sink 24 mA
- 'ACT08 has TTL-compatible inputs
- Standard Military Drawing (SMD)

Ordering Code: See Section 8

#### **Logic Symbols**

#### **Connection Diagrams**



| Pin Nam   | nes | Description          |                   |  | 3.0<br>4.5<br>5.5 |                                    | TL/F/9914-2 |
|---|-----|----------------------|-------------------|--|-------------------|------------------------------------|-------------|
| A <sub>n</sub> , B <sub>n</sub><br>O <sub>n</sub>           |     | Inputs<br>Outputs    |                   |  |                   | Maximum Low Level<br>Input Voltage |             |
| tour =50  |     | 2.9<br>4.4<br>6.4    | 2.9<br>4,4<br>5.4 |  |                   |                                    |             |
| *VIN = VIL 07<br>- 12<br>- 10H 24<br>- 26                   | ٧   |                      | 2.4<br>3.7<br>4.7 |  |                   |                                    |             |
| lour = 50 µA  |     | 1.0<br>1.0<br>1.0    |                   |  |                   |                                    |             |
| 101 28 101 28 29 101 29 29 29 29 29 29 29 29 29 29 29 29 29 | ٧   | 0,44<br>0,44<br>0,44 |                   |  |                   |                                    |             |
| $V_1 = V_{CC}$ , GN   |     |                      |                   |  |                   |                                    |             |

| OTTICE/ DISTRIBUTORS FOR AVAILABILITY  | y and specifications.  | 'AC  | 2.0V to 6.0V  |
|--|--|--|---|
| Supply Voltage (V <sub>CC</sub> )  | -0.5V to $+7.0V$   | 'ACT   | 4.5V to 5.5V  |
| DC Input Diode Current ( $I_{IK}$ ) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ DC Input Voltage ( $V_I$ ) DC Output Diode Current ( $I_{OK}$ ) $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage ( $V_O$ ) DC Output Source | $\begin{array}{c} -20 \text{ mA} \\ +20 \text{ mA} \\ -0.5 \text{V to V}_{CC} + 0.5 \text{V} \\ -20 \text{ mA} \\ +20 \text{ mA} \\ -0.5 \text{V to to V}_{CC} + 0.5 \text{V} \end{array}$ | Input Voltage (V <sub>I</sub> ) Output Voltage (V <sub>O</sub> ) Operating Temperature (T <sub>A</sub> ) 74AC/ACT 54AC/ACT Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V | 0V to V <sub>CC</sub><br>0V to V <sub>CC</sub><br>-40°C to +85°C<br>-55°C to +125°C |
| or Sink Current (I <sub>O</sub> )  | ±50 mA   | Minimum Input Edge Rate (ΔV/Δt)  |   |
| DC V <sub>CC</sub> or Ground Current<br>per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )  | ±50 mA   | 'ACT Devices V <sub>IN</sub> from 0.8V to 2.0V   |   |
| Storage Temperature (T <sub>STG</sub> ) Junction Temperature (T <sub>J</sub> ) CDIP  | -65°C to +150°C  | V <sub>CC</sub> @ 4.5V, 5.5V   | 125 mV/ns   |

to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Note 1: Absolute maximum ratings are those values beyond which damage

# DC Characteristics for 'AC Family Devices

|                 | FORPLRE                              | .0                     | 74                      | AC                   | 54AC                             | 74AC                            |       |   |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|---|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |
|                 | B OH OF ON A                         |                        | Тур                     | N.IT                 | Guaranteed Lir                   | mits_weevalut                   |       |   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | ٧     | $I_{OUT} = -50 \mu\text{A}$   |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | V     | $\label{eq:VIN} \begin{split} * V_{\text{IN}} &= V_{\text{IL}}  \text{or}  V_{\text{IH}} \\ &- 12  \text{mA} \\ I_{\text{OH}} &- 24  \text{mA} \\ &- 24  \text{mA} \end{split}$ |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | ٧     | $I_{OUT} = 50 \mu A$  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                | 0.44<br>0.44<br>0.44            | ٧     | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}OL$ $^{24} \text{ mA}$ $^{24} \text{ mA}$  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μΑ    | $V_{I} = V_{CC}$ , GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| 7, |    |
|----|----|
| 74 | ч  |
|    | -1 |
|    |    |

| Cymbol | THE PARTY OF THE PARTY OF           | (V) | -55°C to + 125°C -40°C to +85°C |       | OIIII             | Conditions |    |  |
|--------|-------------------------------------|-----|---------------------------------|-------|-------------------|------------|----|--|
|        | 0L = 20 pF                          |     | Тур                             | 10    | Guaranteed L      | imits      |    |  |
| IOLD   | †Minimum Dynamic                    | 5.5 | 7.00                            | 11000 | 50                | 75         | mA | V <sub>OLD</sub> = 1.65V Max             |
| IOHD   | Output Current                      | 5.5 | 0.0                             | 0.1   | -50 <sub>aa</sub> | -75        | mA | V <sub>OHD</sub> = 3.85V Min             |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5 | 11.5                            | 4.0   | 7.0 0.08 8.5      | 40.0       | μА | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

# DC Characteristics for 'ACT Family Devices

|                  | 3.09=V                               |                     | 74A            | СТ           | 54ACT                             | 74ACT                           |                 |   |  |
|------------------|--------------------------------------|---------------------|----------------|--------------|-----------------------------------|---------------------------------|-----------------|---|--|
| Symbol           | Parameter                            | V <sub>CC</sub> (V) |                |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units           | Conditions  |  |
|                  | NO COL G                             | 7                   | Тур            | 145590       | Guaranteed Limits                 |                                 |                 | innegation (Dropens   |  |
| VIH              | Minimum High Level Input Voltage     | 4.5<br>5.5          | 1.5<br>1.5     | 2.0          | 2.0                               | 2.0<br>2.0                      | sle <b>V</b> nc | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5          | 1.5<br>1.5     | 0.8          | 0.8<br>0.8                        | 0.8<br>0.8                      | V               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧               | $I_{OUT} = -50 \mu\text{A}$   |  |
|                  | V                                    | 4.5<br>5.5          | 5V             | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | 9<br>80 V       | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5          | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧               | $I_{OUT} = 50 \mu A$  |  |
|                  |                                      | 4.5<br>5.5          |                | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | ٧               | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     | 5.5                 |                | ±0.1         | ±1.0                              | ±1.0                            | μΑ              | $V_{I} = V_{CC}$ , GND  |  |
| ICCT             | Maximum I <sub>CC</sub> /Input       | 5.5                 | 0.6            |              | 1.6                               | 1.5                             | mA              | $V_I = V_{CC} - 2.1V$   |  |
| lold             | †Minimum Dynamic                     | 5.5                 |                |              | 50                                | 75                              | mA              | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub> | Output Current                       | 5.5                 |                |              | -50                               | -75                             | mA              | V <sub>OHD</sub> = 3.85V Min  |  |
| lcc              | Maximum Quiescent<br>Supply Current  | 5.5                 |                | 4.0          | 80.0                              | 40.0                            | μΑ              | $V_{IN} = V_{CC}$ or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### AC Electrical Characteristics: See Section 2 for waveforms.

|                  | Parameter         | DAR               | 74AC 54AC  |            | AC         | 74   | AC                      |      |                         |       |        |
|------------------|-------------------|-------------------|--|------------|------------|------|-------------------------|------|-------------------------|-------|--------|
| Symbol           |                   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |            | to + | −55°C<br>125°C<br>50 pF | to + | -40°C<br>-85°C<br>50 pF | Units | Fig.   |
|                  |                   |                   | Min  | Тур        | Max        | Min  | Max                     | Min  | Max                     |       |        |
| tPLH             | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.5<br>5.5 | 9.5<br>7.5 | 1.0  | 12.5<br>9.0             | 1.0  | 10.0<br>8.5             | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.5 | 8.5<br>7.0 | 1.0  | 11.5<br>8.5             | 1.0  | 9.0<br>7.5              | ns    | 2-3, 4 |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

#### AC Electrical Characteristics: See Section 2 for waveforms.

|                  | Parameter         |                   | T <sub>A</sub> = +25°C T <sub>A</sub> = to |     |     | 54  | ACT  | 74/  | ACT  | stario | 100         |
|------------------|-------------------|-------------------|--|-----|-----|---|------|--|------|--------|-------------|
| Symbol           |                   | V <sub>CC</sub> * |  |     |     | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |      | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ |      | Units  | Fig.<br>No. |
|                  |                   | 169 + 03          | Min  | Тур | Max | Min   | Max  | Min  | Max  |        |             |
| t <sub>PLH</sub> | Propagation Delay | 5.0               | 1.0  | 6.5 | 9.0 |   | dis. | 1.0  | 10.0 | ns     | 2-3, 4      |
| tpHL             | Propagation Delay | 5.0               | 1.0  | 6.5 | 9.0 | 0.8   | 0.1  | 1.0  | 10.0 | ns     | 2-3, 4      |

Maximum Low Level 4.5

\*Voltage Range 5.0 is 5.0V ±0.5V

| Symbol                                      | V                                | Parameter      | Тур        | Units | Sa C                   | onditio | Output Voltee                     |  |
|---|----------------------------------|----------------|------------|-------|------------------------|---------|-----------------------------------|--|
| CIN   | Inpu                             | ıt Capacitance | 4.5        | pF    | V                      | CC = 5  | .0V                               |  |
| C <sub>PD</sub>                             | Power Dissipation<br>Capacitance |                | 20.0       | pF.8  | V <sub>CC</sub> = 5.0V |         | .0V                               |  |
|   |                                  |                | f.0<br>f.0 | 1.0   |                        |         | Massimum Low Level Cutput Voltage |  |
|   |                                  |                |            |       |                        |         |                                   |  |
|   |                                  |                |            |       |                        |         | Maximum input<br>Leakage Current  |  |
|   |                                  |                |            |       |                        |         | Maximum<br>loc/Input              |  |
|   |                                  |                |            |       |                        |         |                                   |  |
| NOHD = 3.85V Min                            |                                  |                |            |       |                        |         |                                   |  |
| V <sub>IN</sub> = V <sub>OD</sub><br>or GND |                                  |                |            | 4.0   |                        |         |                                   |  |



# 54AC/74AC10 • 54ACT/74ACT10 Triple 3-Input NAND Gate

#### **General Description**

The 'AC/'ACT10 contains three, 3-input NAND gates.

The information for the ACT10 is Preliminary Information only.

#### **Features**

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)

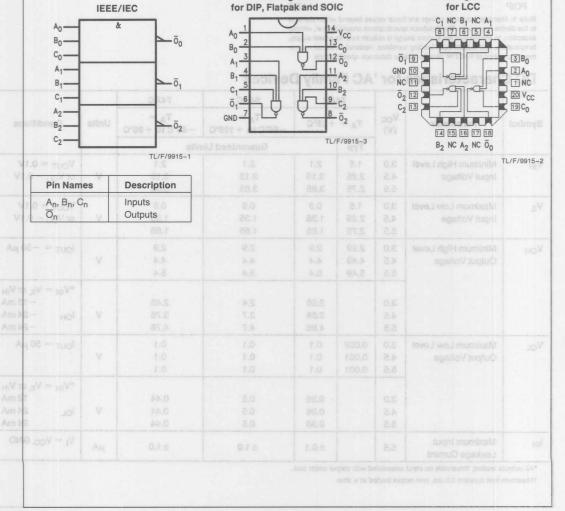
   'AC10: 5962-87610

Absolute Maximum Ratings (Note 1)

Pin Assignment

Ordering Code: See Section 8
Logic Symbol

#### **Connection Diagrams**



Pin Assignment

| Supply Voltage (V <sub>CC</sub> )                     | -0.5V to +7.0V                  | 'ACT   | 4.5V to 5.5V          |
|---|---------------------------------|--|-----------------------|
| DC Input Diode Current (IIK)                          |                                 | Input Voltage (V <sub>I</sub> )                    | OV to V <sub>CC</sub> |
| $V_1 = -0.5V$   | -20 mA                          | Output Voltage (Vo)                                | 0V to V <sub>CC</sub> |
| $V_I = V_{CC} + 0.5V$                                 | + 20 mA                         | Operating Temperature (T <sub>A</sub> )            | 11 0 01011110 00      |
| DC Input Voltage (V <sub>I</sub> )                    | $-0.5V$ to $V_{CC} + 0.5V$      | 74AC/ACT   | -40°C to +85°C        |
| DC Output Diode Current (IOK)                         | Features                        | 54AC/ACT   | -55°C to +125°C       |
| $V_{O} = -0.5V$<br>$V_{O} = V_{CC} + 0.5V$ (OM2) g    | AS 2998 SOURCE 60 -20 mA        | Minimum Input Edge Rate (ΔV/Δ 'AC Devices          | The 'AC/'ACT10 of     |
| DC Output Voltage (V <sub>O</sub> )                   | $-0.5$ V to to $V_{CC} + 0.5$ V | V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> |                       |
| DC Output Source                                      |                                 | V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V                 | 125 mV/ns             |
| or Sink Current (IO)                                  | ± 50 mA                         | Minimum Input Edge Rate (ΔV/Δ                      | t) a main a mark      |
| DC V <sub>CC</sub> or Ground Current                  |                                 | 'ACT Devices                                       |                       |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                          |  | Logic Symb            |
| Storage Temperature (T <sub>STG</sub> )               | -65°C to +150°C                 | V <sub>CC</sub> @ 4.5V, 5.5V                       | 125 mV/ns             |
| Junction Temperature (T <sub>J</sub> )                |                                 |  |                       |
| CDIP meminglesA nin                                   | 175°C                           |  |                       |

0108 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

PDIP

### **DC Characteristics for 'AC Family Devices**

|                  |  | 0                      | 74                      | AC                   | 54AC                              | 74AC                            | inportation and | Gy-man-yO   |  |
|------------------|--|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-----------------|---|--|
| Symbol Parameter |  | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units           | Conditions  |  |
|                  | B <sub>2</sub> NO A <sub>2</sub> NO G <sub>Q</sub> |                        | Тур                     | 18                   | Guaranteed Lin                    | mits                            |                 | - C   |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage                | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | V               | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage                 | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | V               | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage               | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | V               | I <sub>OUT</sub> = -50 μA   |  |
|                  |  | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | ٧               | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>II</sub><br>-12 m/<br>I <sub>OH</sub> -24 m/<br>-24 m/ |  |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage                | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | ٧               | I <sub>OUT</sub> = 50 μA  |  |
|                  |  | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                 | 0.44<br>0.44<br>0.44            | ٧               | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>II</sub><br>12 mA<br>I <sub>OL</sub> 24 mA<br>24 mA    |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current                   | 5.5                    |                         | ±0.1                 | ±1.0                              | ±1.0                            | μΑ              | V <sub>I</sub> = V <sub>CC</sub> , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### 4

#### DC Characteristics for 'AC Family Devices (Continued) Included Inc

|        | ZAAC                                |                        | 74               | AC      | 54AC                             | 74AC                            |       |  |
|--------|-------------------------------------|------------------------|------------------|---------|----------------------------------|---------------------------------|-------|--|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C  | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                               |
|        | Rg 08 - 40                          |                        | Тур              | = 10    | Guaranteed Li                    | mits                            |       |  |
| IOLD   | †Minimum Dynamic                    | 5.5                    | xeM              | \$110.5 | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max             |
| IOHD   | Output Current                      | 5.5                    | 11.0             | 0.7     | -50                              | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min             |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | 10.0             | 4.0     | 88 80.0                          | 40.0                            | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{|N}$  and  $I_{|CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{|CC}$ .  $I_{|CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

# DC Characteristics for 'ACT Family Devices

|   | A = -40°C                            |                     | 74.            | ACT          | 54ACT                             | 74ACT                           |             |  |  |
|---|--------------------------------------|---------------------|----------------|--------------|-----------------------------------|---------------------------------|-------------|--|--|
| Symbol                                  | Parameter = 15                       | V <sub>CC</sub> (V) |                | + 25°C       | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units       | Conditions   |  |
| X 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 |                                      | 91                  | Тур            | 1215/0       | Guaranteed Li                     | mits                            |             |  |  |
| V <sub>IH</sub>                         | Minimum High Level<br>Input Voltage  | 4.5<br>5.5          | 1.5<br>1.5     | 2.0          | 2.0<br>2.0 3.3                    | 2.0<br>2.0                      | vsleV no    | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>                         | Maximum Low Level Input Voltage      | 4.5<br>5.5          | 1.5<br>1.5     | 0.8<br>0.8   | 0.8<br>0.8                        | 0.8<br>0.8                      | ٧           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>                         | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧           | $I_{OUT} = -50 \mu\text{A}$  |  |
|   | V                                    | 4.5<br>5.5          | 9V             | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | Pot<br>VOay | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$                       |  |
| V <sub>OL</sub>                         | Maximum Low Level Output Voltage     | 4.5<br>5.5          | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧           | $I_{OUT} = 50 \mu A$   |  |
|   |                                      | 4.5<br>5.5          |                | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | V           | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub>                         | Maximum Input<br>Leakage Current     | 5.5                 |                | ±0.1         | ±1.0                              | ± 1.0                           | μΑ          | $V_I = V_{CC}$ , GND   |  |
| ICCT                                    | Maximum I <sub>CC</sub> /Input       | 5.5                 | 0.6            |              | 1.6                               | 1.5                             | mA          | $V_I = V_{CC} - 2.1V$  |  |
| lold                                    | †Minimum Dynamic                     | 5.5                 |                |              | 50                                | 75                              | mA          | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub>                        | Output Current                       | 5.5                 |                |              | -50                               | -75                             | mA          | V <sub>OHD</sub> = 3.85V Min   |  |
| lcc                                     | Maximum Quiescent<br>Supply Current  | 5.5                 |                | 4.0          | 80.0                              | 40.0                            | μΑ          | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### 

|                  |                   | DAI                   | 7          | 74AC   |            | 54   | AC                      | 74   | 1AC                       |         |             |
|------------------|-------------------|-----------------------|------------|--|------------|------|-------------------------|------|---------------------------|---------|-------------|
| Symbol           | Parameter         | V <sub>CC</sub> * (V) |            | C <sub>L</sub> = +25°C<br>C <sub>L</sub> = 50 pF | -55°C      | to + | -55°C<br>125°C<br>50 pF | to - | −40°C<br>-85°C<br>- 50 pF | Units   | Fig.<br>No. |
| vetil V/88       | t may Am          | 7479                  | Min        | Тур  | Max        | Min  | Max                     | Min  | Max                       | ioil 57 | L many      |
| t <sub>PLH</sub> | Propagation Delay | 3.3<br>5.0            | 1.5<br>1.5 | 6.0<br>4.5                                       | 9.5<br>7.0 | 1.0  | 11.0<br>8.5             | 1.0  | 10.5                      | ns ns   | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay | 3.3<br>5.0            | 1.5<br>1.5 | 5.5 0.08<br>4.0                                  | 8.5<br>6.0 | 1.0  | 10.0<br>7.0             | 1.0  | 10.0<br>6.5               | ns      | 2-3,4       |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |                   | 11.5              |     | 74ACT                  | / Devi | 54   | ACT                     | 74/  | ACT                    | Chara |       |
|------------------|-------------------|-------------------|-----|------------------------|--------|------|-------------------------|------|------------------------|-------|-------|
| Symbol           | Parameter and     | V <sub>CC</sub> * |     | C <sub>L</sub> = +25°C | 6      | to + | -55°C<br>125°C<br>50 pF | to + | -40°C<br>85°C<br>50 pF | Units | Fig.  |
|                  |                   |                   | Min | Тур                    | Max    | Min  | Max                     | Min  | Max                    |       |       |
| t <sub>PLH</sub> | Propagation Delay | 5.0               | 1.0 | 6.5                    | 9.0    | ne   | 31                      | 1.0  | 10.0                   | ns    | 2-3,4 |
| tpHL VI.O        | Propagation Delay | 5.0               | 1.0 | 6.5                    | 9.0    | 0.8  | 8.8                     | 1.0  | 9.5                    | ns    | 2-3,4 |

\*Voltage Range 5.0 is 5.0V  $\pm 0.5 \text{V}$ 

| A 60                         |      |                            |      |       |       |            |                                     |  |
|------------------------------|------|----------------------------|------|-------|-------|------------|-------------------------------------|--|
| Symbol                       | V P  | Parameter                  | Тур  | Units | Co    | nditio     | ns dipiri muminiM                   |  |
| CIN                          | Inpu | t Capacitance              | 4.5  | pF    | Vo    | C = 5.     |                                     |  |
| Am ASCPD<br>Am AS —          |      | er Dissipation<br>acitance | 25.0 | pF    | Vo    | C = 5.     | OV                                  |  |
| lour = 50 µA                 |      |                            |      |       | 100.0 | 4.6<br>3.5 | Maximum Low Level<br>Output Voltage |  |
|                              |      |                            |      |       |       |            |                                     |  |
|                              |      |                            |      |       |       |            |                                     |  |
|                              |      |                            |      |       |       |            |                                     |  |
| V <sub>OLD</sub> = 1.65V Max |      |                            |      |       |       |            |                                     |  |
|                              |      |                            |      |       |       |            |                                     |  |
|                              |      |                            |      |       |       |            |                                     |  |



# 54AC/74AC11 Triple 3-Input AND Gate

#### **General Description**

The 'AC11 contains three 3-input AND gates.

#### **Features**

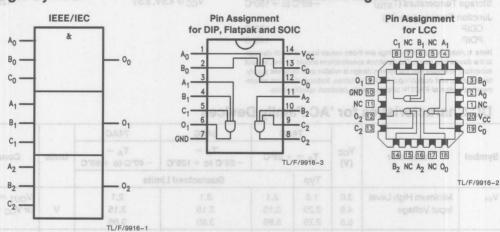
- Outputs source/sink 24 mA
- Standard Military Drawing (SMD) Standard Military Drawing (SMD) Standard Military Drawing (SMD) Standard Military Drawing (SMD)

Ordering Code: See Section 8

**Logic Symbol** 

VI = Vcc. G

#### **Connection Diagrams**



| Pin Names  | Description |
|--|-------------|
| A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> | Inputs      |
| On   | Outputs     |

4

#### **Absolute Maximum Rating (Note 1)**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V<sub>CC</sub>) DC Input Diode Current (I<sub>IK</sub>)  $V_1 = -0.5V$ -20 mA

 $V_I = V_{CC} + 0.5V$ +20 mA -0.5V to  $V_{CC} + 0.5V$ DC Input Voltage (V<sub>I</sub>)

-0.5V to +7.0V

±50 mA

DC Output Diode Current (IOK)

 $V_0 = -0.5V$  $V_{O} = V_{CC} + 0.5V$  (CME) grid

DC Output Voltage (VO) -0.5V to to V<sub>CC</sub> + 0.5V

DC Output Source or Sink Current (IO)

DC V<sub>CC</sub> or Ground Current per Output Pin (ICC or IGND)  $\pm 50 \, \text{mA}$ Storage Temperature (TSTG) -65°C to +150°C

Junction Temperature (T<sub>J</sub>)

175°C PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### **Recommended Operating** Conditions

Supply Voltage (VCC) 'AC

2.0V to 6.0V 'ACT 4.5V to 5.5V OV to Vcc

Input Voltage (V<sub>I</sub>) Output Voltage (Vo) Operating Temperature (TA)

-40°C to +85°C

-55°C to +125°C

OV to Vcc

54AC/ACT Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

74AC/ACT

VIN from 30% to 70% of VCC

125 mV/ns V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices VIN from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

#### **DC Characteristics for 'AC Family Devices**

|                  |                                      | 19                  | 74                      | AC                   | 54AC                             | 74AC                            |       |   |
|------------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|---|
| Symbol Parameter |                                      | V <sub>CC</sub> (V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |
|                  |                                      |                     | Тур                     |                      | Guaranteed Lin                   | mits                            |       |   |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | v a   | $I_{OUT} = -50 \mu\text{A}$   |
|                  |                                      | 3.0<br>4.5<br>5.5   |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | ٧     | $\label{eq:VIN} \begin{split} * V_{\text{IN}} &= V_{\text{IL}}  \text{or}  V_{\text{IH}} \\ &- 12  \text{mA} \\ I_{\text{OH}} &- 24  \text{mA} \\ &- 24  \text{mA} \end{split}$ |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | ٧     | $I_{OUT} = 50 \mu A$  |
|                  |                                      | 3.0<br>4.5<br>5.5   |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                | 0.44<br>0.44<br>0.44            | ٧     | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}OL$ $^{24} \text{ mA}$ $^{24} \text{ mA}$  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     | 5.5                 |                         | ±0.1                 | ±1.0                             | ±1.0                            | μΑ    | $V_I = V_{CC}$ , GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued)

|        |                                     |                        | 74               | IAC    | 54AC                              | 74AC                            | e armer<br>De eliman |  |
|--------|-------------------------------------|------------------------|------------------|--------|-----------------------------------|---------------------------------|----------------------|--|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                | Conditions                               |
|        |                                     |                        | Тур              |        | Guaranteed Li                     | mits                            | 1111                 | MATINAAC                                 |
| lold   | †Minimum Dynamic                    | 5.5                    |                  | uqni   | 50                                | 75                              | mA                   | V <sub>OLD</sub> = 1.65V Max             |
| IOHD   | Output Current                      | 5.5                    |                  |        | -50                               | -75                             | mA                   | V <sub>OHD</sub> = 3.85V Min             |
| Icc b  | Maximum Quiescent<br>Supply Current | 5.5                    | sierosis         | 4.0    | OA' ent 80.08 me 'AC              | 40.0                            | μА                   | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. The property of the standard outputs loaded; thresholds on input associated with output under test. The property of the standard outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. and the respective limit @ 5.5V V<sub>CC</sub> and the respective limit @ 5.5V V<sub>CC</sub> and the respective limit @ 5.5V V<sub>CC</sub>.

#### AC Characteristics: See Section 2 for waveforms

|                  |                   |                   |            | 74AC                  |            | 54         | AC                      | 74         | AC                     |       |             |
|------------------|-------------------|-------------------|------------|-----------------------|------------|------------|-------------------------|------------|------------------------|-------|-------------|
| Symbol           | Parameter         | V <sub>CC</sub> * |            | C <sub>L</sub> = +25° |            | to +       | −55°C<br>125°C<br>50 pF | to +       | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                  |                   | en ann neg        | Min        | Тур                   | Max        | Min        | Max                     | Min        | Max                    | Sym   | ilgo.       |
| t <sub>PLH</sub> | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5 | 5.5<br>4.0            | 9.5<br>8.0 | 1.0        | 11.0<br>8.5             | 1.0<br>1.0 | 10.0<br>8.5            | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5 | 5.5<br>4.0            | 8.5<br>7.0 | 1.0<br>1.0 | 10.5<br>8.0             | 1.0<br>1.0 | 9.5<br>7.5             | ns    | 2-3, 4      |

<sup>\*</sup>Voltage Range 3.3 is 3.3V ±0.3V

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 20.0 | pF    | V <sub>CC</sub> = 5.0V |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time. graph of evidence and a time graph of evidence and the decidence of the decidence

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V



#### 54AC/74AC14

# **Hex Inverter with Schmitt Trigger Input**

#### **General Description**

The 'AC14 contains six inverter gates each with a Schmitt trigger input. The 'AC14 contains six logic inverters which accept standard CMOS input signals and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 'AC14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

Syenitol

Symbol

#### **Features**

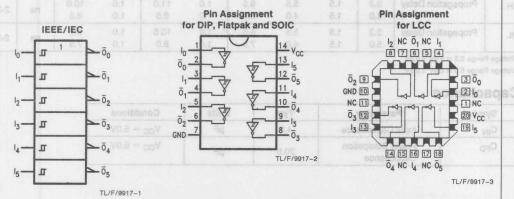
- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)

   'AC14: 5962-87624

#### Ordering Code: See Section 8

#### Logic Symbol

#### **Connection Diagrams**



#### **Function Table**

| Input | Output |  |
|-------|--------|--|
| Α     | ō      |  |
| L     | Н      |  |
| Н     | L      |  |

| Pin Names | Description |
|-----------|-------------|
| In        | Inputs      |
| Ōn        | Outputs     |

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for available       |            |                           |
|---|------------|---------------------------|
| Supply Voltage (V <sub>CC</sub> )       | 40°C to ±1 | 0.5V to +7.0V             |
| DC Input Diode Current (IIK)            |            |                           |
| $V_1 = -0.5V$                           |            | -20 mA                    |
| $V_I = V_{CC} + 0.5V$                   |            | + 20 mA                   |
| DC Input Voltage (V <sub>I</sub> )      | -0.5V      | to $V_{CC} + 0.5V$        |
| DC Output Diode Current (IOK)           |            |                           |
| $V_0 = -0.5V$                           |            | -20 mA                    |
| $V_O = V_{CC} + 0.5V$                   |            | + 20 mA                   |
| DC Output Voltage (V <sub>O</sub> )     | -0.5V to   | to V <sub>CC</sub> + 0.5V |
| DC Output Source                        |            | 50                        |
| or Sink Current (I <sub>O</sub> )       |            | ±50 mA                    |
| DC V <sub>CC</sub> or Ground Current    |            |                           |
| per Output Pin (ICC or IGND)            |            | ± 50 mA                   |
| Storage Temperature (T <sub>STG</sub> ) | -65        | 5°C to +150°C             |
| Junction Temperature (T <sub>J</sub> )  |            |                           |
| CDIP                                    |            | 175°C                     |
|   |            |                           |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

PDIP

#### Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

| AC   |                   | 2.0V to 6.0V<br>4.5V to 5.5V      |
|--|-------------------|-----------------------------------|
| Input Voltage (V <sub>I</sub> )                                  |                   | 0V to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )                                 |                   | 0V to V <sub>CC</sub>             |
| Operating Temperature<br>74AC/ACT<br>54AC/ACT                    | (T <sub>A</sub> ) | −40°C to +85°C<br>−55°C to +125°C |
| Minimum Input Edge R 'AC Devices V <sub>IN</sub> from 30% to 70° |                   | 'cc                               |
| V <sub>CC</sub> @ 3.3V, 4.5V, 5.                                 |                   | plane 125 mV/ns                   |
| Minimum Input Edge R   | late (Δ           | V/Δt) menuO luqtuO                |
| V <sub>IN</sub> from 0.8V to 2.0<br>V <sub>CC</sub> @ 4.5V, 5.5V | V<br>8.8          | money (Igg 125 mV/ns              |
|  |                   |                                   |

Note: I<sub>IIN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than

### DC Characteristics for 'AC Family Devices

| .04                      | to +85°C Unit                        |                        |                         | AC                   | 54AC                             | 74AC                            | retens            | 169                         | Symbol   |
|--------------------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------------------|-----------------------------|--|
| Symbol                   | Parameter MA                         | V <sub>CC</sub><br>(V) |                         |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units             | Conditions                  |  |
| 2-3,4                    |                                      |                        | Тур                     | 0.1                  | Guaranteed Li                    | mits                            | ellon Del         | Рторав                      | HJ9  |
| V <sub>OH</sub><br>2-3,4 | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | ello <b>y</b> Del | I <sub>OUT</sub> =          | -50 μΑ   |
|                          |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | V                 | *V <sub>IN</sub> =          | V <sub>IL</sub> or V <sub>IH</sub><br>-12 mA<br>-24 mA<br>-24 mA |
| V <sub>OL</sub>          | Maximum Low Level Output Voltage     | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | N V               | I <sub>OUT</sub> =          | 50 μΑ  |
|                          |                                      |                        |                         | (9)                  | 0.00                             | sonsfoage                       | 0                 | *VIN =                      | V <sub>IL</sub> or V <sub>IH</sub>                               |
|                          |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                | 0.44<br>0.44<br>0.44            | V                 | loL                         | 12 mA<br>24 mA<br>24 mA  |
| I <sub>IN</sub>          | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μА                | $V_{I} = V_{0}$             | CC, GND  |
| V <sub>t+</sub>          | Maximum Positive<br>Threshold        | 3.0<br>4.5<br>5.5      |                         | 2.2<br>3.2<br>3.9    | 2.2<br>3.2<br>3.9                | 2.2<br>3.2<br>3.9               | V                 | T <sub>A</sub> = Worst Case |  |
| V <sub>t</sub> -         | Minimum Negative<br>Threshold        | 3.0<br>4.5<br>5.5      |                         | 0.5<br>0.9<br>1.1    | 0.5<br>0.9<br>1.1                | 0.5<br>0.9<br>1.1               | ٧                 | $T_A = V$                   | Vorst Case   |

140°C

†Maximum test duration 2.0 ms, one output loaded at a time.

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

#### DC Characteristics for 'AC Family Devices (Continued) The Property of the Prop

|                     |                                     |                     | 74AC                       |                   | 54AC                                | 74AC                            | ge ess   | If Military/Aurost                       |  |
|---------------------|-------------------------------------|---------------------|----------------------------|-------------------|-------------------------------------|---------------------------------|----------|--|--|
| Symbol              | Parameter  Maximum Hysteresis       | V <sub>CC</sub> (V) | T <sub>A</sub> =           | + 25°C            | T <sub>A</sub> = -55°C to + 125°C   | T <sub>A</sub> = -40°C to +85°C | Units    | Conditions                               |  |
|                     |                                     |                     | Тур                        | put Voltag        | Guaranteed Li                       | mits                            | rent (ha | DC Input Diede Cu                        |  |
| V <sub>h(max)</sub> |                                     | 3.0<br>4.5<br>5.5   | 5×1 denegme                | 1.2<br>1.4<br>1.6 | 1.2 05 +<br>1.4<br>1.6              | 1.2<br>1.4<br>1.6               | V        | T <sub>A</sub> = Worst Case              |  |
| V <sub>h(min)</sub> | Minimum Hysteresis                  | 3.0<br>4.5<br>5.5   | iut Edge<br>es<br>10% to 7 | 0.3<br>0.4<br>0.5 | 0.3 02 -<br>0.4 02 +<br>0.5.0 + 00\ | 0.3<br>0.4<br>0.5               | v v (6V) | TA = Worst Case                          |  |
| IOLD                | †Minimum Dynamic                    | 5.5                 | V, 4.5V,                   | 8,8 Ø 50V         | 50                                  | 75                              | mA       | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD                | Output Current                      | 5.5                 | agod Jui                   | Nemum Inc.        | -50                                 | -75                             | mA       | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc<br>anv/m        | Maximum Quiescent<br>Supply Current | 5.5                 | 1,8V to 2<br>V, S.6V       | 4.0               | 80.0                                | 40.0                            | μА       | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### AC Electrical Characteristics: See Section 2 for waveforms

| Symbol           |                   |  | N. July    | 74AC   | 5   | 4AC          | 74   | AC           | 2.00  |             |
|------------------|-------------------|--|------------|--|---|--------------|--|--------------|-------|-------------|
|                  | Parameter         | Contract of the contract of th |            | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |              | $T_A = -40^{\circ}C$<br>$to +85^{\circ}C$<br>$C_L = 50 pF$ |              | Units | Fig.<br>No. |
|                  | Units Cond        | 28 + 01 3 01   | Min        | Тур Мах  | Min   | Max          | Min  | Max          | 19    | Symbo       |
| t <sub>PLH</sub> | Propagation Delay | 3.3<br>5.0   | 1.5<br>1.5 | 9.5 13.5<br>7.0 10.0                             | 1.0   | 16.0<br>12.0 | 1.5<br>1.5   | 15.0<br>11.0 | ns    | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay | 3.3<br>5.0   | 1.5<br>1.5 | 7.5 11.5<br>6.0 8.5                              | 1.0   | 14.0         | 1.5<br>1.5   | 13.0<br>9.5  | ns    | 2-3,4       |

<sup>\*</sup>Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

| Symbol          | Parameter         | Тур  | Units | Conditions             |
|-----------------|-------------------|------|-------|------------------------|
| CIN             | Input Capacitance | 4.5  | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub> | Power Dissipation | 05.0 | 0.1   | V <sub>CC</sub> = 5.0V |
|                 | Capacitance       | 25.0 | pF    |                        |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.



# 54AC/74AC20 Dual 4-Input NAND Gate

#### **General Description**

The 'AC20 contains four 4-input NAND gates.

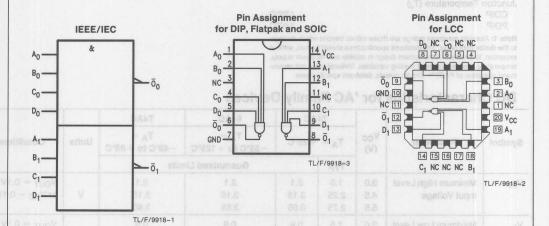
#### **Features**

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)

Ordering Code: See Section 8

**Logic Symbol** 

#### **Connection Diagrams**



| Pin Names                     | Description    |
|-------------------------------|----------------|
| $A_m$ , $B_n$ , $C_n$ , $D_n$ | Inputs Outputs |

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0VSupply Voltage (V<sub>CC</sub>)

DC Input Diode Current (IIK)  $V_1 = -0.5V$ 

-20 mA +20 mA

 $V_I = V_{CC} + 0.5V$ DC Input Voltage (VI)

-0.5V to  $V_{CC} + 0.5V$ 

DC Output Diode Current (IOK)

-20 mA  $V_0 = -0.5V$  $V_O = V_{CC} + 0.5V$  (CM2) galaxied visibility basis + 20 mA -0.5V to to V<sub>CC</sub> + 0.5V DC Output Voltage (VO)

DC Output Source

or Sink Current (In) ±50 mA

DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±50 mA Storage Temperature (TSTG) -65°C to +150°C

Junction Temperature (T<sub>J</sub>)

CDIP memogisaA ni9 PDIP

175°C 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### **Recommended Operating** Conditions

Supply Voltage (VCC) 'AC

2.0V to 6.0V 4.5V to 5.5V

Input Voltage (V<sub>I</sub>) Output Voltage (Vo)

'ACT

OV to VCC OV to Vcc

Operating Temperature (TA)

74AC/ACT 54AC/ACT

-40°C to +85°C -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

VIN from 30% to 70% of VCC

Vcc @ 3.3V, 4.5V, 5.5V

125 mV/ns

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

VIN from 0.8V to 2.0V VCC @ 4.5V, 5.5V

125 mV/ns

#### **DC Characteristics for 'AC Family Devices**

| E ™ Vec         |                                      | 0                      | 74                                | AC                   | 54AC                              | 74AC                                   |        |   |  |
|-----------------|--------------------------------------|------------------------|-----------------------------------|----------------------|-----------------------------------|--|--------|---|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) |                                   |                      | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C        | Units  | Conditions  |  |
|                 | C, NC NC NC NC R                     |                        | Тур                               | LIT.                 | Guaranteed Li                     | mits                                   |        | B comme   |  |
| V <sub>IH</sub> | Minimum High Level   3.0   1.5   2.1 |                        | 2.1 2.1<br>3.15 3.15<br>3.85 3.85 |                      | ٧                                 | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$ |        |   |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75               | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65                    | V      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49              | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4                      | emay n | $I_{OUT} = -50 \mu A$   |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                                   | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76                   | V      | $^*$ V $_{\rm IN}=$ V $_{\rm IL}$ or V $_{\rm IH}$ $-$ 12 mA $_{\rm OH}$ $-$ 24 mA $_{\rm C}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001           | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1                      | V      | $I_{OUT} = 50 \mu A$  |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                                   | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                 | 0.44<br>0.44<br>0.44                   | V      | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA                              |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                                   | ±0.1                 | ±1.0                              | ±1.0                                   | μΑ     | $V_I = V_{CC}$ , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued)

|                  | Parameter                           |                        | 74AC<br>T <sub>A</sub> = +25°C |     | 54AC                             | 74AC                            | Units | olone 2 back                             |
|------------------|-------------------------------------|------------------------|--------------------------------|-----|----------------------------------|---------------------------------|-------|--|
| Symbol           |                                     | V <sub>CC</sub><br>(V) |                                |     | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C |       | Conditions                               |
|                  |                                     |                        | Тур                            |     | Guaranteed Li                    | mits                            | 180   | DAACITAA                                 |
| I <sub>OLD</sub> | †Minimum Dynamic                    | 5.5                    |                                |     | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max             |
| I <sub>OHD</sub> | Output Current                      | 5.5                    |                                |     | -50                              | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min             |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5                    | eink 24                        | 4.0 | 80.0                             | 40.0                            | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note : $I_{\rm IN}$  and  $I_{\rm CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\rm CC}$ .

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  | Parameter memogles A | marpi         | mano i di noi 74AC |                   | 54AC       |     | 74   | AC O | c Sym   | Logi |  |  |             |
|------------------|----------------------|---------------|--------------------|-------------------|------------|-----|--|------|---|------|--|--|-------------|
| Symbol           |                      | mamagianA (V) | mamnglas A 119     | V <sub>CC</sub> * |            |     | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |      | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ |      | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ |  | Fig.<br>No. |
|                  |                      |               | 0                  | Min               | Тур        | Max | Min  | Max  | Min   | Max  | THE STREET   |  |             |
| t <sub>PLH</sub> | Propagation Delay    | 3.3<br>5.0    | 2.0<br>1.5         | 6.0<br>5.0        | 8.5<br>7.0 | 1.0 | 11.0<br>8.5                                | 1.5  | 10.0  | ns   | 2-3,4  |  |             |
| t <sub>PHL</sub> | Propagation Delay    | 3.3<br>5.0    | 1.5                | 5.0<br>4.0        | 7.0<br>6.0 | 1.0 | 10.5<br>7.0                                | 1.0  | 9.0<br>7.0  | ns   | 2-3,4  |  |             |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

| Symbol          | Parameter                        | Тур  | Units | Conditions<br>V <sub>CC</sub> = 5.0V |  |
|-----------------|----------------------------------|------|-------|--------------------------------------|--|
| CIN             | Input Capacitance                | 4.5  | pF    |                                      |  |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40.0 | pF    | V <sub>CC</sub> = 5.0V               |  |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.



# 54AC/74AC32 ● 54ACT/74ACT32 Quad 2-Input OR Gate

#### **General Description**

The 'AC/'ACT32 contains four, 2-input OR gates.

The information for the ACT32 is Preliminary information only.

#### **Features**

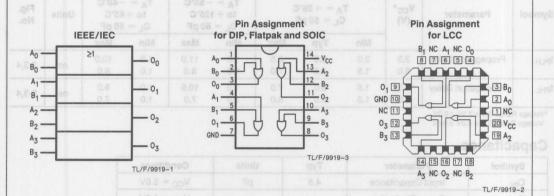
- Outputs source/sink 24 mA
- 'ACT32 has TTL-compatible inputs
- Standard Military Drawing (SMD) — 'AC32: 5962-87614

Ordering Code: See Section 8

#### **Logic Symbol**

#### **Connection Diagrams**

AC Electrical Characteristics: see Section 2 for waveforms



| Pin Names                       | Description |  |  |
|---------------------------------|-------------|--|--|
| A <sub>n</sub> , B <sub>n</sub> | Inputs      |  |  |
| On                              | Outputs     |  |  |

125 mV/ns

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales

| oility and specifications.        |
|-----------------------------------|
| -0.5V to $+7.0$ V                 |
| aranteed Limits                   |
| -20 mA                            |
| + 20 mA                           |
| $-0.5$ V to $V_{CC} + 0.5$ V      |
| 0.04 0.00                         |
| -20 mA                            |
| + 20 mA                           |
| $-0.5$ V to to $V_{CC}$ + $0.5$ V |
|                                   |
| ± 50 mA                           |
|                                   |
| ±50 mA                            |
| -65°C to +150°C                   |
|                                   |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

CDIP PDIP

#### Absolute Maximum Rating (Note 1) Recommended Operating Conditions

V<sub>CC</sub> @ 4.5V, 5.5V

|      | 6,770,077                                    |         |   |
|------|--|---------|---|
|      | Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT   |         | 2.0V to 6.0V<br>4.5V to 5.5V  |
|      | Input Voltage (V <sub>I</sub> )              |         | 0V to V <sub>CC</sub>   |
|      | Output Voltage (V <sub>O</sub> )             |         | olement OV to VCC   |
|      | Operating Temperatur<br>74AC/ACT<br>54AC/ACT | 3.5     | -40°C to +85°C  |
|      | V <sub>IN</sub> from 30% to 70               | )% of \ | V/Δt) Memo Video Memo |
| ivel | 'ACT Devices                                 |         | OC Characteristics  |

### **DC Characteristics for 'AC Family Devices**

| Symbol Am AS —       | - = tuoi V                          | 4.4                 | 74                      | AC                    | 54AC                              | 84.4 74AC lev                   | Units                     | Conditions   |
|----------------------|-------------------------------------|---------------------|-------------------------|-----------------------|-----------------------------------|---------------------------------|---------------------------|--|
|                      | Parameter                           | V <sub>CC</sub> (V) | T <sub>A</sub> =        | + 25°C                | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C |                           |  |
|                      | HO! V                               |                     | Тур                     | Typ Guaranteed Limits |                                   |                                 |                           |  |
| V <sub>IH</sub>      | Minimum High Level<br>Input Voltage | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85   | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | ollege<br>ollege          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| VIL AS<br>Am AS      | Maximum Low Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65   | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | ٧                         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| Ves -                | Minimum High Level Output Voltage   | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4     | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | negut<br>Ovent            | $I_{OUT} = -50 \mu\text{A}$  |
| xeM Vča.<br>niM Vča. | = aloV Am                           | 3.0<br>4.5<br>5.5   |                         | 2.56<br>3.86<br>4.86  | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | t<br>m Dynar<br>ber Vit   | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>- 12 mA<br>I <sub>OH</sub> - 24 mA<br>- 24 mA |
| VoL                  | Maximum Low Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1     | 0.1<br>0.1<br>0.1                 | 0.1 3 0.1<br>0.1<br>0.1 0.1     | inemul<br>V<br>o abiodesi | $I_{OUT} = 50 \mu A$   |
|                      |                                     | 3.0<br>4.5<br>5.5   |                         | 0.36<br>0.36<br>0.36  | 0.5<br>0.5<br>0.5                 | 0.44<br>0.44<br>0.44            | v ai oraș                 | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA                                       |
| I <sub>IN</sub>      | Maximum Input<br>Leakage Current    | 5.5                 |                         | ±0.1                  | ±1.0                              | ±1.0                            | μΑ                        | $V_I = V_{CC}$ , GND   |

175°C

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued)

|               |                                     |                     | 74AC<br>T <sub>A</sub> = +25°C |             | 54AC                              | 74AC                            | aki edi            | toatroo seesto                           |  |
|---------------|-------------------------------------|---------------------|--------------------------------|-------------|-----------------------------------|---------------------------------|--------------------|--|--|
| Symbol Paramo | Parameter                           | V <sub>CC</sub> (V) |                                |             | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units              | Conditions                               |  |
| Do V of VO    |                                     |                     | Тур                            | gestoV aug  | Guaranteed Li                     | rent (IIId)                     | DC Input Diode Cur |  |  |
| lold          | †Minimum Dynamic                    | 5.5                 | (oV) eg                        | stput Valle | 50                                | 75                              | mA                 | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD          | Output Current                      | 5.5                 | mperatu                        | T gaitere   | -50                               | od V8.0=75                      | mA (               | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc as r      | Maximum Quiescent<br>Supply Current | 5.5                 | anh2 tu                        | 4.0         | 80.0                              | 40.0                            | μΑ                 | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{\text{IN}}$  and  $I_{\text{CC}}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\text{CC}}$ .

ICC for 54AC @ 25°C is identical to 74AC @ 25°C.

| GILLAND              |                                      |                     | 74.            | ACT          | 54AC  | GT + .01                          | 74ACT  | (are I) or                    |   |  |
|----------------------|--------------------------------------|---------------------|----------------|--------------|---|-----------------------------------|--|-------------------------------|---|--|
| Symbol               | Parameter                            | V <sub>CC</sub> (V) |                |              | + 25°C T <sub>A</sub> =<br>-55°C to + 125°C |                                   | T <sub>A</sub> = -40°C to +85°C                    | Units                         | Conditions  |  |
|                      |                                      |                     | Тур            |              | Guarar                                      | teed Li                           | mits dealer could be                               | na egnérar rou<br>routemb out | Note 1: Absolute maxim  |  |
| V <sub>IH</sub>      | Minimum High Level<br>Input Voltage  | 4.5<br>5.5          | 1.5<br>1.5     | 2.0<br>2.0   | 2.0<br>2.0                                  | power au<br>es not rec<br>stions: | 2.0<br>2.0   | or instead with               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub>      | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5          | 1.5<br>1.5     | 0.8<br>0.8   | 0.8<br>0.8                                  | unliy                             | 0.8<br>0.8   | olieV19                       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>      | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49   | 4.4 0<br>5.4 | 4.4<br>5.4                                  | AG                                | 4.4<br>5.4   | V                             | $I_{OUT} = -50 \mu\text{A}$   |  |
| enolti               | P.C. Units Corn                      | 4.5<br>5.5          | - sorc         | 3.86<br>4.86 | 3.70<br>4.70                                |                                   | 3.76<br>4.76                                       | V                             | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub>      | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5          | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                                  | 3.15                              | 85.5 0.1 <sub>3.8</sub><br>85.6 0.1 <sub>3.8</sub> | Vaga                          | I <sub>OUT</sub> = 50 μA  |  |
| V1.0<br>V1.0         | V or Vac                             | 4.5<br>5.5          |                | 0.36<br>0.36 | 0.50<br>0.50                                |                                   | 0.44<br>0.44                                       | Low Level<br>ageV             | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN4</sub> 03- | Maximum Input<br>Leakage Current     | 5.5                 |                | ±0.1         | ± 1.0                                       | 2.9                               | 88.5 ± 1.08  | μΑ                            | V <sub>I</sub> = V <sub>CC</sub> , GND  |  |
| Ісст                 | Maximum<br>I <sub>CC</sub> /Input    | 5.5                 | 0.6            |              | 1.6   | 5.4                               | @A,8 1.5 8   | mA                            | $V_I = V_{CC} - 2.1V$   |  |
| I <sub>OLD</sub>     | †Minimum Dynamic                     | 5.5                 |                |              | 50  | 2.55                              | 750.8  | mA                            | V <sub>OLD</sub> = 1.65V Max  |  |
| IOHD                 | Output Current                       | 5.5                 |                |              | -50   | 38.8                              | -75  | mA                            | V <sub>OHD</sub> = 3.85V Min  |  |
| ICC AH OR            | Maximum Quiescent<br>Supply Current  | 5.5                 |                | 4.0          | 80.0  | 1:0                               | soc.o 40.0.e                                       | μΑ                            | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  |                   |                   |  | 74AC       |            | 54   | AC          | 74   | AC          | met!  |        |
|------------------|-------------------|-------------------|--|------------|------------|--|-------------|--|-------------|-------|--------|
| Symbol           | Parameter         | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |             | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ |             | Units | Fig.   |
|                  |                   | 00                | aola   | Min        | Тур        | Max  | Min         | Max  | Min         | Max   | T-01   |
| t <sub>PLH</sub> | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.5 | 9.0<br>7.5 | 1.0<br>1.0   | 12.0<br>9.0 | 1.5<br>1.0   | 10.0<br>8.5 | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.0 | 8.5<br>7.0 | 1.0  | 11.5<br>8.5 | 1.0  | 9.0<br>7.5  | ns    | 2-3, 4 |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  | Parameter         | reni eldit               | 74ACT  T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF |     |     | 54/   | ACT | 74/  | ACT  | tel Juchi i | med and     |
|------------------|-------------------|--------------------------|--|-----|-----|---|-----|--|------|-------------|-------------|
| Symbol           |                   | V <sub>CC</sub> *<br>(V) |  |     |     | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units       | Fig.<br>No. |
|                  |                   |                          | Min  | Тур | Max | Min   | Max | Min  | Max  |             |             |
| t <sub>PLH</sub> | Propagation Delay | 5.0                      | 1.0  | 6.5 | 9.0 |   | 81  | 1.0  | 10.0 | ns          | 2-3,        |
| t <sub>PHL</sub> | Propagation Delay | 5.0                      | 1.0  | 6.5 | 9.0 |   |     | 1.0  | 10.0 | ns          | 2-3,        |

\*Voltage Range 5.0 is 5.0V  $\pm 0.3$ V

#### Capacitance

| Symbol          | Parameter                        | <b>Тур</b> | Units | Conditions      |
|-----------------|----------------------------------|------------|-------|-----------------|
| CIN             | Input Capacitance                | 4.5        | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 20.0       | pF 0  | $V_{CC} = 5.0V$ |



# 54AC/74AC74 • 54ACT/74ACT74 **Dual D-Type Positive Edge-Triggered Flip-Flop**

#### **General Description**

The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, Q) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

LOW input to SD (Set) sets Q to HIGH level LOW input to CD (Clear) sets Q to LOW level Clear and Set are independent of clock Simultaneous LOW on  $\overline{C}_D$  and  $\overline{S}_D$  makes both Q and  $\overline{Q}$ 

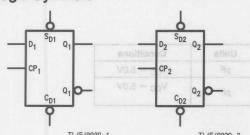
AC Electrical Characteristics: See Section 2 for wave

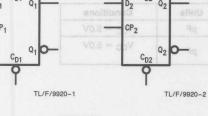
#### **Features**

- Output source/sink 24 mA
- 'ACT74 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC74: 5962-88520
  - 'ACT74: 5962-87525

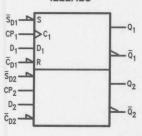
Ordering Code: See Section 8

#### **Logic Symbols**





#### IEEE/IEC

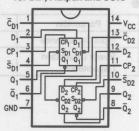


TI /F/9920-3

| Pin Names                                  | Description         |
|--|---------------------|
| D <sub>1</sub> , D <sub>2</sub>            | Data Inputs         |
| CP <sub>1</sub> , CP <sub>2</sub>          | Clock Pulse Inputs  |
| $\overline{C}_{D1}, \overline{C}_{D2}$     | Direct Clear Inputs |
| S <sub>D1</sub> , S <sub>D2</sub>          | Direct Set Inputs   |
| $Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$ | Outputs             |

#### **Connection Diagrams**

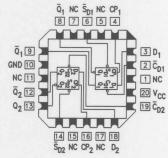
**Pin Assignment** for DIP, Flatpak and SOIC



TL/F/9920-4

locmy2

#### Pin Assignment for LCC

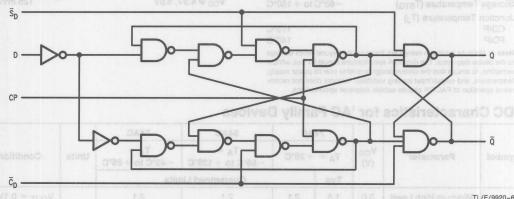


TL/F/9920-5

|         | Inp              | uts |   | Out            | puts             | ondine:         |
|---------|------------------|-----|---|----------------|------------------|-----------------|
| SD      | CD               | CP  | D | Q              | Q                | AC Veltas       |
| /8.E or | /E-H             | X   | Х | Н              | L                | 'AGT            |
| O'Hot   | VO L             | X   | X | L              | HV)              | put Voltage     |
| io\Los  | VO L             | X   | X | Н              | (oH) =           | utput Voltag    |
| Н       | Н                | _   | Н | (ATH en        | np4rate          | perating Te     |
| H-      | 40 <b>H</b> 3.to | _   | L | L              | Н                | 74AC/ACT        |
| H       | of H of          | L   | X | Q <sub>0</sub> | $\overline{Q}_0$ | <b>SHAQ/AGT</b> |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- = LOW-to-HIGH Clock Transition
- $Q_0(\overline{Q}_0)$  = Previous  $Q(\overline{Q})$  before LOW-to-HIGH Transition of Clock

# **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Absolute Maximum Rating (Note 1)**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

 $\begin{array}{lll} \text{Supply Voltage (V}_{CC}) & -0.5 \text{V to } +7.0 \text{V} \\ \text{DC Input Diode Current (I}_{IK}) & & & \\ V_I = -0.5 \text{V} & & -20 \text{ mA} \\ V_I = \text{V}_{CC} + 0.5 \text{V} & & +20 \text{ mA} \end{array}$ 

DC Input Voltage (V<sub>I</sub>)

CDIP

PDIP

DC Output Diode Current ( $I_{OK}$ )  $V_O = -0.5V$  -20 mA  $V_O = V_{CC} + 0.5V$  +20 mA DC Output Voltage ( $V_O$ ) -0.5V to to  $V_{CC} + 0.5V$ 

-0.5V to  $V_{CC} + 0.5$ V

175°C

140°C

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}$ C to  $+150^{\circ}$ C Junction Temperature ( $T_{J}$ )

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating

74AC/ACT  $-40^{\circ}$ C to  $+85^{\circ}$ C  $-55^{\circ}$ C to  $+125^{\circ}$ C Minimum Input Edge Rate ( $\Delta$ V/ $\Delta$ t)

'AC Devices
V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>
V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices

 $\rm V_{IN}$  from 0.8V to 2.0V  $\rm V_{CC}$  @ 4.5V, 5.5V 125 mV/ns

| - 10            | a franchis                           |                        | 74                      | AC                   | 54AC                             | 74AC                            |                     |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|---------------------|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units               | Conditions   |
|                 |                                      |                        | Тур                     | -                    | Guaranteed Li                    | mits                            |                     |  |
| ViH             | Minimum High Level                   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | ib el <b>V</b> tari | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | V                   | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V                   | $I_{OUT} = -50 \mu\text{A}$  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | ٧                   | $\label{eq:VIN} \begin{split} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &- 12 \text{ mA} \\ I_{\text{OH}} &- 24 \text{ mA} \\ &- 24 \text{ mA} \end{split}$ |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V                   | Ι <sub>ΟυΤ</sub> = 50 μΑ   |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                | 0.44<br>0.44<br>0.44            | V                   | $^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA<br>IOL  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μА                  | $V_I = V_{CC}$ , GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued) and Date of Board DA

|              | 74AC                                |                        | OA7                    | 4AC    | 54AC                              | 74AC                            |       |  |
|--------------|-------------------------------------|------------------------|------------------------|--------|-----------------------------------|---------------------------------|-------|--|
| Symbol       | Parameter Agoa = 30                 | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |        | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                               |
|              |                                     |                        | Тур                    | 70     | Guaranteed Li                     | mits                            |       |  |
| IOLD         | †Minimum Dynamic                    | 5.5                    | RIV                    | 01100  | 50                                | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max             |
| IOHD         | Output Current                      | 5.5                    |                        | 20     | -50                               | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min             |
| Icc<br>4,8-8 | Maximum Quiescent<br>Supply Current | 5.5                    | 13                     | 0.14.0 | 0.08 12.0                         | 40.0                            | μΑ    | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

|                  | 2.5 10.6 ns                         |                        | 744                    | CT           | 10.0                             | 54ACT        | 3.5                             | 74ACT        | . Ō 10               | THILL From Sen  |  |
|------------------|-------------------------------------|------------------------|------------------------|--------------|----------------------------------|--------------|---------------------------------|--------------|----------------------|---|--|
| Symbol           | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = -55°C to +125°C |              | T <sub>A</sub> = -40°C to +85°C |              | Units                | Conditions  |  |
|                  |                                     |                        | Тур                    |              | 187-0                            | Guaranteed L | imits                           | areastur     | a Clina              | discionO OA   |  |
| VIH              | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5             | 2.0          | 500                              | 2.0          | 24.83                           | 2.0          | ٧                    | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5             | 0.8          | 25°C                             |              | Vec*                            | 0.8          | em.V <sub>is</sub> q | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>  | Minimum High Level Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4   |                                  | 4.4<br>5.4   |                                 | 4.4<br>5.4   | ٧                    | $I_{OUT} = -50 \mu\text{A}$   |  |
|                  | 4.5<br>2.0 ns                       | 4.5<br>5.5             | 6.0<br>4.0             | 3.86<br>4.86 | 4.0<br>3.0                       | 3.70<br>4.70 | 8.8                             | 3.76<br>4.76 | Pine, Hill           | $V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage | 4.5<br>5.5             | 0.001<br>0.001         | 0.1<br>0.1   | 6.6                              | 0.1          | 5.0<br>8.3                      | 0.1          | V no                 | I <sub>OUT</sub> = 50 μA  |  |
|                  | 0.0<br>0<br>0                       | 4.5<br>5.5             | 5.6<br>0.5<br>0.5      | 0.36<br>0.36 | 4.5<br>0<br>0                    | 0.50<br>0.50 | 3.3<br>6.0                      | 0.44         | any yns              | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current    | 5.5                    |                        | ±0.1         |                                  | ±1.0         |                                 | ±1.0         | μА                   | V <sub>I</sub> = V <sub>CC</sub> , GND  |  |
| ICCT             | Maximum<br>I <sub>CC</sub> /Input   | 5.5                    | 0.6                    |              |                                  | 1.6          |                                 | 1.5          | mA                   | $V_I = V_{CC} - 2.1V$   |  |
| I <sub>OLD</sub> | †Minimum Dynamic                    | 5.5                    |                        |              | 14.1                             | 50           |                                 | 75           | mA                   | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub> | Output Current                      | 5.5                    |                        | 4            |                                  | -50          |                                 | -75          | mA                   | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5                    |                        | 4.0          |                                  | 80.0         |                                 | 40.0         | μА                   | $V_{IN} = V_{CC}$ or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                  |   | TAAC                     |            | 74AC                  |              | 54  | AC           | 74   | AC           |       |        |
|------------------|---|--------------------------|------------|-----------------------|--------------|---|--------------|--|--------------|-------|--------|
| Symbol           | Parameter   | V <sub>CC</sub> *<br>(V) |            | C <sub>L</sub> = +25° |              | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |              | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 \text{ pF}$ |              | Units | Fig.   |
| webs Mag         |   | 207                      | Min        | Тур                   | Max          | Min   | Max          | Min  | Max          | .0.40 |        |
| f <sub>max</sub> | Maximum Clock<br>Frequency  | 3.3<br>5.0               | 100<br>140 | 125<br>160            |              | 70<br>95  | d.           | 95<br>125  | themu0 tu    | MHz   | alto   |
| t <sub>PLH</sub> | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 3.3<br>5.0               | 3.5<br>2.5 | 8.0<br>6.0            | 12.0<br>9.0  | 1.0   | 13.0<br>9.5  | 2.5  | 13.0<br>10.0 | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 3.3<br>5.0               | 4.0        | 10.5                  | 12.0<br>9.5  | 1.0<br>1.0  | 14.0<br>10.5 | 3.5<br>2.5   | 13.5<br>10.5 | ns    | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$                                     | 3.3<br>5.0               | 4.5<br>3.5 | 8.0<br>6.0            | 13.5<br>10.0 | 1.0   | 17.5<br>12.0 | 4.0<br>3.0   | 16.0<br>10.5 | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$                                     | 3.3<br>5.0               | 3.5<br>2.5 | 8.0<br>6.0            | 14.0<br>10.0 | 1.0<br>1.0  | 13.5<br>10.0 | 3.5<br>2.5   | 14.5<br>10.5 | ns    | 2-3, 4 |

\*Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V

#### AC Operating Requirements: See Section 2 for Waveforms

| V1.0 -           | apV to  | 0,0  | 74AC 54AC                |              | l a        | 74AC  | Imput V    |  |             |             |      |
|------------------|---|------|--------------------------|--------------|------------|---|------------|--|-------------|-------------|------|
| Symbol           | Parameter   | 8.0  | V <sub>CC</sub> *<br>(V) | 7.70         |            | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |            | $T_A = -40^{\circ}C$<br>$to +85^{\circ}C$<br>$C_L = 50 pF$ | Units       | Fig.<br>No. |      |
| -50 p.A          | - 1001 V  | 6.4  |                          | Тур          |            | Gua   | ranteed    | Mini   | mum opstioV | JudhiO      | HO   |
| t <sub>s</sub>   | Set-up Time, HIGH or<br>D <sub>n</sub> to CP <sub>n</sub>           | LOW  | 3.3<br>5.0               | 1.5<br>1.0   | 4.0        | 38.6  | 5.0<br>4.0 | 8.   | 4.5<br>3.0  | ns          | 2-7  |
| th As of         | Hold Time, HIGH or L  | OW   | 3.3<br>5.0               | -2.0<br>-1.5 | 0.5<br>0.5 | 0B,A  | 0.5        | 8.   | 0.5         | ns          | 2-7  |
| t <sub>w</sub>   | $CP_n$ or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$<br>Pulse Width | 0.1  | 3.3<br>5.0               | 3.0<br>2.5   | 5.5<br>4.5 | 1.0   | 8.0<br>5.5 | 8,   | 7.0<br>5.0  | ns          | 2-3  |
| t <sub>rec</sub> | Recovery Time  Con or Son to CP                                     | 0.44 | 3.3<br>5.0               | -2.5<br>-2.0 | 0          | 0.36  | 0.5<br>0.5 | 18   | 0           | ns          | 2-3, |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

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# AC Electrical Characteristics: See Section 2 for Waveforms

|                  | Parameter  |                       |     | 74ACT  |      | 54  | ACT   | 74. | ACT                    | mes s   | THE T       |
|------------------|--|-----------------------|-----|--|------|-----|---|-----|------------------------|---------|-------------|
| Symbol           |  | V <sub>CC</sub> * (V) |     | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |      |     | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |     | -40°C<br>85°C<br>50 pF | Units   | Fig.<br>No. |
|                  |  |                       | Min | Тур  | Max  | Min | Max   | Min | Max                    | S be    | ous:        |
| f <sub>max</sub> | Maximum Clock<br>Frequency   | 5.0                   | 145 | 210  | 7    | 85  | 4   | 125 | ghose                  | MHz     | maD         |
| t <sub>PLH</sub> | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $\overline{Q}_n$ or $\overline{Q}_n$ | 5.0                   | 3.0 | 5.5  | 9.5  | 1.0 | 11.5  | 2.5 | 10.5                   | ns also | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $\overline{Q}_n$ or $\overline{Q}_n$ | 5.0                   | 3.0 | 6.0  | 10.0 | 1.0 | 12.5  | 3.0 | 11.5                   | ns      | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay CP <sub>n</sub> to Q <sub>n</sub> or Q n   | 5.0                   | 4.0 | 7.5  | 11.0 | 1.0 | 14.0  | 4.0 | 13.0.                  | ns      | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$  | 5.0                   | 3.5 | 6.0  | 10.0 | 1.0 | 12.0  | 3.0 | 11.5                   | ns      | 2-3, 4      |

\*Voltage Range 5.0 is 5.0V ±0.5V

# AC Operating Requirements: See Section 2 for Waveforms

|                  |  |                   | 74                                | ACT | 54ACT  | 74ACT  | Antikono contra | min sk      |  |
|------------------|--|-------------------|-----------------------------------|-----|--|--|-----------------|-------------|--|
| Symbol           | Parameter  | V <sub>CC</sub> * | T <sub>A</sub> = C <sub>L</sub> = |     | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40$ °C<br>to $+85$ °C<br>$C_L = 50$ pF | Units           | Fig.<br>No. |  |
| 20               | VICE DIE PROPERTY DE SO  |                   | Тур                               |     | Guaranteed Min   | imum   |                 | anne gA     |  |
| ts               | Set-up Time, HIGH or LOW<br>D <sub>n</sub> to CP <sub>n</sub>                | 5.0               | 1.0                               | 3.0 | 4.0  | 3.5  | ns              | 2-7         |  |
| th               | Hold Time, HIGH or LOW   | 5.0               | -0.5                              | 1.0 | 1.0  | 1.0  | ns              | 2-7         |  |
| t <sub>w</sub>   | CP <sub>n</sub> or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$<br>Pulse Width | 5.0               | 3.0                               | 5.0 | 7.0  | 6.0  | ns              | 2-3         |  |
| t <sub>rec</sub> | Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP               | 5.0               | -2.5                              | 0   | 0.5  | 0  | ns o            | 2-3, 7      |  |

\*Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 35.0 | pF    | V <sub>CC</sub> = 5.0V |



# 54AC/74AC86

# Quad 2-Input Exclusive-OR Gate

#### **General Description**

The 'AC86 contains four, 2-input exclusive-OR gates.

#### **Features**

- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
   "AC86: 5962-89550

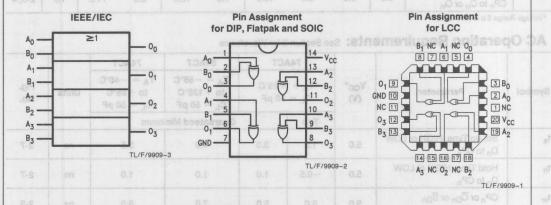
AC Electrical Characteristics: see Section 2 for Waveforms

Sympol

Ordering Code: See Section 8

**Logic Symbol** 

#### **Connection Diagrams**



|       | Pin Names  | Description   |
|-------|--|---------------|
| 2-3,7 | A <sub>0</sub> -A <sub>3</sub><br>B <sub>0</sub> -B <sub>3</sub> | Inputs Inputs |
| 343   | 00-03  | Outputs       |

 Symbol
 Parameter
 Typ
 Units
 Cenditions

 CHV
 Input Capacitance
 4.5
 pF
 Voc = 5.0V

 CPD
 Power Dissipation
 35.0
 pF
 Voc = 5.0V

 Capacitance
 35.0
 pF
 Voc = 5.0V

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0VSupply Voltage (V<sub>CC</sub>) DC Input Diode Current (IIK)  $V_1 = 0.5V$ -20 mA  $V_1 = V_{CC} + 0.5V$ +20 mA DC Input Voltage (V<sub>I</sub>) -0.5V to V<sub>CC</sub> +0.5V

DC Output Diode Current (IOK)  $V_0 = -0.5V$ 

 $V_O = V_{CC} + 0.5V$ +20 mA -0.5V to V<sub>CC</sub> +0.5V DC Output Voltage (Vo) ±50 mA

DC Output Source or Sink Current (IO) DC V<sub>CC</sub> or Ground Current

Per Output Pin (ICC or IGND) ±50 mA -65°C to +150°C

Storage Temperature (T<sub>STG</sub>) Junction Temperature (T<sub>J</sub>)

CDIP 175°C PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>) 'AC 2.0V to 6.0V 'ACT 4.5V to 5.5V Input Voltage (V<sub>I</sub>) OV to VCC Output Voltage (Vo) turni mumica OV to VCC Operating Temperature (TA) -40°C to +85°C 74AC/ACT -55°C to +125°C 54AC/ACT

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

VIN from 30% to 70% of VCC

125 mV/ns V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices VIN from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V

# DC Characteristics for 'AC Family Devices

|                 | xshi               | niaŭ j                 | 74/                   | AC                   | 54AC                                      | 74AC                            |           |  |  |
|-----------------|--------------------|------------------------|-----------------------|----------------------|---|---------------------------------|-----------|--|--|
| Symbol          | Parameter          | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |                      | T <sub>A</sub> = 0.00<br>-55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions   |  |
|                 |                    | 3.T                    | Тур                   | 1.0                  | Guaranteed L                              | imits 0.8 V8                    | ation Del | реун Ргоред  |  |
| VIH             | Minimum High Level | 3.0                    | 1.5                   | 2.1                  | 2.1                                       | 2.1                             | IRdanO o  | V <sub>OUT</sub> = 0.1V  |  |
|                 | Input Voltage      | 4.5                    | 2.25                  | 3.15                 | 3.15                                      | 3.15                            | VER       | or V <sub>CC</sub> - 0.1V  |  |
|                 |                    | 5.5                    | 2.75                  | 3.85                 | 3.85                                      | 3.85                            | 1.0± V0.8 | Voltage Range 5.6V   |  |
| VIL             | Maximum Low Level  | 3.0                    | 1.5                   | 0.9                  | 0.9                                       | 0.9                             | . 9       | V <sub>OUT</sub> = 0.1V  |  |
|                 | Input Voltage      | 4.5                    | 2.25                  | 1.35                 | 1.35                                      | 1.35                            | V         | or V <sub>CC</sub> - 0.1V  |  |
|                 |                    | 5.5                    | 2.75                  | 1.65                 | 1.65                                      | 1.65                            | gel       | Symbol   |  |
| V <sub>OH</sub> | Minimum High Level | 3.0                    | 2.99                  | 2.9                  | 2.9                                       | 2.9                             | nagaO lu  | $I_{OUT} = -50 \mu A$  |  |
|                 | Output Voltage     | 4.5                    | 4.49                  | 4.4                  | Pq4.4 88                                  | echal 4.4 O notes               | V         | Cpp Por  |  |
|                 |                    | 5.5                    | 5.49                  | 5.4                  | 5.4                                       | 5.4                             |           |  |  |
|                 |                    | 3.0<br>4.5<br>5.5      |                       | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                         | 2.46<br>3.76<br>4.76            | ٧         | $^{*V_{\text{IN}}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $-12 \text{ mA}$ $I_{\text{OH}} -24 \text{ mA}$ $-24 \text{ mA}$ |  |
| VOL             | Maximum Low Level  | 3.0                    | 0.002                 | 0.1                  | 0.1                                       | 0.1                             |           | $I_{OUT} = 50 \mu A$   |  |
|                 | Output Voltage     | 4.5                    | 0.001                 | 0.1                  | 0.1                                       | 0.1                             | V         |  |  |
|                 |                    | 5.5                    | 0.001                 | 0.1                  | 0.1                                       | 0.1                             |           |  |  |
|                 |                    | 3.0                    |                       | 0.36                 | 0.50                                      | 0.44                            |           | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA  |  |
|                 |                    | 4.5                    |                       | 0.36                 | 0.50                                      | 0.44                            | V         | I <sub>OL</sub> 24 mA  |  |
|                 |                    | 5.5                    |                       | 0.36                 | 0.50                                      | 0.44                            |           | 24 mA  |  |

-20 mA

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 20 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued) The Republic of the Continued of the

| Symbol                | VO.S Parameter                      | V <sub>CC</sub> (V) | 74               | AC                 | 54AC                               | 74AC                            | equ eon   | N Military/Aerosp  |
|-----------------------|-------------------------------------|---------------------|------------------|--------------------|------------------------------------|---------------------------------|-----------|--|
|                       |                                     |                     | T <sub>A</sub> = | = 25°C             | T <sub>A</sub> = -55°C to + 125°C  | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions   |
| paV of                |                                     |                     | Тур              | usileV tu          | Guaranteed L                       | imits                           | (all) the | DC Input Diade Cut   |
| I <sub>IN</sub> oV of | Maximum Input<br>Leakage Current    | 5.5                 | oV) egs          | ±0.1               | Am 05-<br>+ 20 1 <b>0.1</b> ± 1.00 | ±1.0                            | μА        | $V_{I} = V_{CC}$ , GND                                       |
| loz as r              | Maximum TRI-STATE®                  |                     | T                | AAGAAC<br>AAGAAG   | 8 Am 60                            | (20                             | )) inem.  | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{O} = V_{CC}$ , GND |
| I <sub>OLD</sub>      | †Minimum Dynamic                    | 5.5                 | DEN EGG<br>SBS   | muumini<br>NC Devi | 50                                 | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max                                 |
| IOHD                  | Output Current                      | 5.5                 | of aP08          | mora No            | -50.0+50                           | of V8.0-75                      | mA        | V <sub>OHD</sub> = 3.85V Min                                 |
| Icc                   | Maximum Quiescent<br>Supply Current | 5.5                 | bil italia       | 4.0                | Am Cast<br>80                      | 40 mem                          | μА        | V <sub>IN</sub> = V <sub>CC</sub> or GND                     |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Parameter

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                  |  | V <sub>CC</sub> * (V) |  | 74AC       |             |   | 54AC         |  | AC          | t to ansurar to | soliquome   |
|------------------|--|-----------------------|--|------------|-------------|---|--------------|--|-------------|-----------------|-------------|
| Symbol           | Parameter                              |                       | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |            |             | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |              | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |             | Units           | Fig.<br>No. |
|                  |  |                       | Min  | Тур        | Max         | Min   | Max          | Min  | Max         | 1               |             |
| t <sub>PHL</sub> | Propagation Delay<br>Inputs to Outputs | 3.3<br>5.0            | 2.0  | 6.0<br>4.5 | 11.5<br>8.5 | 1.0   | 14.0<br>10.0 | 1.5  | 12.5<br>9.5 | ns ns           | 2-3,        |
| t <sub>PLH</sub> | Propagation Delay<br>Inputs to Outputs | 3.3<br>5.0            | 2.0  | 6.5<br>4.5 | 11.5<br>8.5 | 1.0   | 14.0<br>10.0 | 1.5<br>1.0   | 12.5<br>9.0 | ns              | 2-3, 4      |

\*Voltage Range 3.3V is 3.3V  $\pm 0.3$ V Voltage Range 5.0V is 5.0V  $\pm 0.5$ V

#### Capacitance

Symbol

|                 |      |             |                  |     |     | 200               |      |     |  |
|-----------------|------|-------------|------------------|-----|-----|-------------------|------|-----|--|
| CIN             | Inpu | ut Capacita | ince             | 4.5 | pF  | V <sub>CC</sub> = | 5.0V |     |  |
| C <sub>PD</sub> | Pov  | ver Dissipa | tion Capacitance | 35  | pF  | V <sub>CC</sub> = | 5.0V | 4.5 |  |
|                 |      |             | 4.8              |     | 5.4 | A.6               | 5.49 |     |  |
|                 | V"   |             |                  |     |     |                   |      |     |  |
| -12 mA          |      |             |                  |     |     |                   |      |     |  |
|                 |      |             |                  |     |     |                   |      |     |  |
| Am +S-          |      |             |                  |     | 4.7 |                   |      |     |  |
|                 |      |             |                  |     |     | 7.0               |      |     |  |
|                 |      |             |                  |     |     |                   |      |     |  |
|                 |      |             |                  |     |     |                   |      |     |  |
|                 | V*   |             |                  |     |     |                   |      |     |  |
|                 |      |             | 0.44             |     |     |                   |      |     |  |
|                 |      |             |                  |     |     |                   |      |     |  |

Units

Conditions

Тур

<sup>†</sup>Maximum test duration 20 ms, one output loaded at a time.



# 54AC/74AC109 • 54ACT/74ACT109 Dual JK Positive Edge-Triggered Flip-Flop

#### **General Description**

The 'AC/'ACT109 consists of two high-speed completely independent transition clocked  $J\overline{K}$  flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The  $J\overline{K}$  design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and  $\overline{K}$  inputs together.

Asynchronous Inputs:

LOW input to  $\overline{S}_D$  (Set) sets Q to HIGH level LOW input to  $\overline{C}_D$  (Clear) sets Q to LOW level

Clear and Set are independent of clock

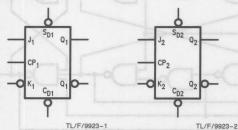
Simultaneous LOW on  $\overline{\mathbb{C}}_D$  and  $\overline{\mathbb{S}}_D$  makes both Q and  $\overline{\mathbb{Q}}$ 

#### **Features**

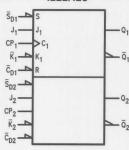
- Outputs source/sink 24 mA
- 'ACT109 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC109: 5962-89551
  - 'ACT109: 5962-88534

#### Ordering Code: See Section 8

# **Logic Symbols**



#### IEEE/IEC

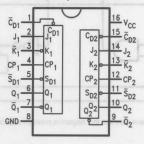


TL/F/9923-7

| Pin Names  | Description  |
|--|--|
| $J_1, J_2, \overline{K}_1, \overline{K}_2$ $CP_1, CP_2$ $\overline{C}_{D1}, \overline{C}_{D2}$ $\overline{S}_{D1}, \overline{S}_{D2}$ $Q_1, Q_2, \overline{Q}_1, \overline{Q}_2$ | Data Inputs Clock Pulse Inputs Direct Clear Inputs Direct Set Inputs Outputs |

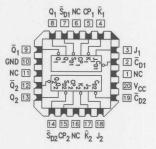
#### **Connection Diagrams**

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9923-3

# Pin Assignment for LCC



TL/F/9923-4

#### Truth Table (each half)

|                  |                  | Inputs      |          | Outp  | outs           |                  |
|------------------|------------------|-------------|----------|-------|----------------|------------------|
| $\overline{s}_D$ | $\overline{c}_D$ | СР          | J        | K     | Q              | Q                |
| L                | Н                | X           | X        | X     | Н              | وعلوا            |
| Н                | L                | X           | X        | X     | E              | Н                |
| L                | L                | X           | X        | X     | H              | H                |
| Н                | Н                | _           | L        | L     | F. B.          | Н                |
| Н                | Н                | 5           | Н        | L     | Tog            | gle              |
| Н                | Н                | 5           | L        | Н     | Q <sub>0</sub> | $\overline{Q}_0$ |
| Н                | H #              | note To Ins | brittest | His : | F SFH Se       | BSRL             |
| ыны              | ritoHeesi        | sm 🗷 bn     | X        | X     | Q <sub>0</sub> | $\overline{Q}_0$ |

H = HIGH Voltage Level

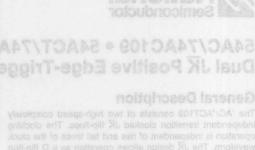
L = LOW Voltage Level

\_\_ = LOW-to-HIGH Transition

X = Immaterial

 $Q_0(\overline{Q}_0) = \text{Previous } Q_0(\overline{Q}_0) \text{ before LOW-to-HIGH Transition of Clock}$ 

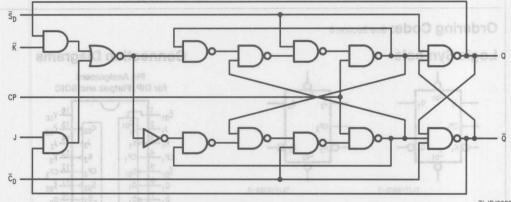
#### Logic Diagram (one half shown)



operation is independent of rise and tall times of the plock waveform. The JR design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and R incuts together.

Asynchronous inputs:

LOW input to Co (Clear) sets Q to LOW level



TL/F/9923-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Fin Assignment

for LCC

of Set MC CP K

on Se

| Pin Names |
|-----------|
|           |

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ ) -0.5V to +7.0VDC Input Diode Current ( $I_{IK}$ )  $V_I = -0.5V$  -20 mA  $V_I = V_{CC} + 0.5V$  +20 mA

DC Input Voltage ( $V_I$ ) -0.5V to  $V_{CC} + 0.5V$ DC Output Diode Current ( $I_{OK}$ )

 $V_{O} = -0.5V$  -20 mA  $V_{O} = V_{CC} + 0.5V$  +20 mADC Output Voltage ( $V_{O}$ ) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Source or Sink Current (I<sub>O</sub>)

or Sink Current (I<sub>O</sub>) ± 50 mA

DC V<sub>CC</sub> or Ground Current
per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ± 50 mA

Storage Temperature (T<sub>STG</sub>)
Junction Temperature (T<sub>J</sub>)

CDIP PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>)
'AC
'ACT

Input Voltage (Vi)

2.0V to 6.0V 4.5V to 5.5V 0V to V<sub>CC</sub>

Output Voltage (V<sub>O</sub>)
Operating Temperature (T<sub>A</sub>)
74AC/ACT

-40°C to +85°C -55°C to +125°C

54AC/ACT
Minimum Input Edge Rate (ΔV/Δt)
'AC Devices

 $V_{\rm IN}$  from 30% to 70% of  $V_{\rm CC}$   $V_{\rm CC}$  @ 3.3V, 4.5V, 5.5V

125 mV/ns

Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

**DC Characteristics for 'AC Family Devices** 

-65°C to +150°C

175°C

140°C

|                 |                                  | -                   | 74               | AC     | la h     | 54AC             |            | 74AC                    | ins      | e i ripiH   |                                       |
|-----------------|----------------------------------|---------------------|------------------|--------|----------|------------------|------------|-------------------------|----------|-------------|---------------------------------------|
| Symbol          | Parameter                        | V <sub>CC</sub> (V) | T <sub>A</sub> = | + 25°C | -58      | T <sub>A</sub> = |            | -40°C to +85            | °C       | Units       | Conditions                            |
|                 |                                  | 76                  | € Тур            |        |          | Guaran           | teed Li    | mits 8.6                |          |             |                                       |
| VIH             | Minimum High Level               | 3.0                 | 1.5              | 2.1    | 4.70     | 2.1              | 4.86       | 2.1                     |          |             | V <sub>OUT</sub> = 0.1V               |
| Au              | Input Voltage                    | 4.5                 | 2.25             | 3.15   | F.0 -    | 3.15             |            | 100.0 3.15              | leve     | V           | or V <sub>CC</sub> - 0.1V             |
|                 |                                  | 5.5                 | 2.75             | 3.85   | 1.0      | 3.85             | 1.0        | 100.0 3.85.8            |          | oitage      | V SugtuO                              |
| VILIV 10        | Maximum Low Level                | 3.0                 | 1.5              | 0.9    |          | 0.9              |            | 0.9                     |          |             | $V_{OUT} = 0.1V$                      |
|                 | Input Voltage                    | 4.5                 | 0 2.25           | 1.35   | 0.50     | 1.35             |            | 1.35                    |          | V           | or V <sub>CC</sub> - 0.1V             |
| 24 mA           | 701 A                            | 5.5                 | 0 2.75           | 1.65   | 03.0     | 1.65             | 0.38       | 1.65                    |          |             |                                       |
| VOH             | Minimum High Level               | 3.0                 | 2.99             | 2.9    |          | 2.9              |            | 2.9                     |          | Jugal a     | $I_{OUT} = -50 \mu\text{A}$           |
|                 | Output Voltage                   | 4.5                 | 4.49             | 4.4    | 0.T±     | 4.4              |            | 4.4                     |          | theVnO      |                                       |
| 2.1V            | V <sub>I</sub> = V <sub>GG</sub> | 5.5                 | 5.49             | 5.4    |          | 5.4              |            | 5.4                     |          | -           |                                       |
|                 |                                  | - 6,                |                  |        | 8.1      |                  |            | 8.0 8.6                 |          | - 1         | *VIN = VIL or VIH                     |
|                 |                                  | 3.0                 |                  | 2.56   | ris Di   | 2.4              |            | 2.46                    | 70       | m Dynan     | -10 mA                                |
|                 |                                  | 4.5                 |                  | 3.86   | PACE .   | 3.7              |            | 3.76                    | Q15      | ٧           | I <sub>OH</sub> -24 mA                |
| .85V Min        | E = qHoV   Am                    | 5.5                 |                  | 4.86   | - 50     | 4.7              |            | 4.76                    |          | 3110110     | -24 mA                                |
| VOL             | Maximum Low Level                | 3.0                 | 0.002            | 0.1    | 0.09     | 0.1              | 4.0        | 0.1                     | ine      | n Quieso    | $I_{OUT} = 50 \mu\text{A}$            |
|                 | Output Voltage                   | 4.5                 | 0.001            | 0.1    | 1.00     | 0.1              |            | 0.1                     |          | V           |                                       |
|                 |                                  | 5.5                 | 0.001            | 0.1    |          | 0.1              | sebnu fire | 0.1 as a                | Bigris ) | io ablorias |                                       |
|                 |                                  |                     |                  | 5 LIX. | 100      | 1000             |            | mil is its babbol fuglu | 0-90     | n 2.0 ms, r | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ |
|                 |                                  | 3.0                 |                  | 0.36   |          | 0.5              |            | 0.44                    | ouns     | bl at Ofes  | 12 mA                                 |
|                 |                                  | 4.5                 |                  | 0.36   |          | 0.5              |            | 0.44                    |          | V           | I <sub>OL</sub> 24 mA                 |
|                 |                                  | 5.5                 |                  | 0.36   | The same | 0.5              |            | 0.44                    |          |             | 24 mA                                 |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current | 5.5                 |                  | ±0.1   |          | ±1.0             |            | ±1.0                    |          | μΑ          | $V_I = V_{CC}$ , GND                  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol  | Parameter                           | Parameter (V) T <sub>A</sub> = +25°C -55°C to +125°C -40°C to +85 |         | -40°C to +85°C | Units      | Conditions         |    |  |
|---------|-------------------------------------|---|---------|----------------|------------|--------------------|----|--|
|         | V0                                  |   | Тур     | Input Voltage  | sell) men  | DC Input Diode Cur |    |  |
| IOLD    | †Minimum Dynamic                    | 5.5   | (oV) et | Output Volta   | 50         | 75                 | mA | V <sub>OLD</sub> = 1.65V Max             |
| IOHD    | Output Current                      | 5.5   | uizioam | Operating Te   | -50 0 + 50 | / of V8.0-75       | mA | V <sub>OHD</sub> = 3.85V Min             |
| Icc ast | Maximum Quiescent<br>Supply Current | 5.5   | egbE 10 | 4.0            | 80.0       | 40.0               | μА | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

|                       |                                     |                        | 74.              | ACT          | 3.41                     | 54ACT                      |                                    | 74ACT                           | (a,T) (m)      | Junction Temperatu   |
|-----------------------|-------------------------------------|------------------------|------------------|--------------|--------------------------|----------------------------|------------------------------------|---------------------------------|----------------|--|
| Symbol                | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | -55°                     | T <sub>A</sub> =<br>C to + | 125°C                              | T <sub>A</sub> = -40°C to +85°C | Units          | Conditions   |
|                       |                                     |                        | Тур              |              | (                        | Guaran                     | teed Li                            | mits                            | odstab erf     | to the device may occur.   |
| V <sub>IH</sub>       | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   |                          | 2.0                        | power sur<br>as not red<br>stions, | 2.0<br>2.0                      | V              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>       | Maximum Low Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | esoi                     | 0.8                        | ylim                               | 0.8<br>0.8                      | V              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub>       | Minimum High Level Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | AT                       | 4.4<br>5.4                 | 0//                                | 4.4<br>5.4                      | V              | $I_{OUT} = -50 \mu\text{A}$  |
| VIO                   | N THOU                              | 4.5<br>5.5             | -40°C            | 3.86<br>4.86 | STC 10 -<br>Guara<br>2.1 | 3.70<br>4.70               | 2.1                                | 3.76<br>4.76                    | V<br>me I doil | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| V <sub>OL</sub> /1.0  | Maximum Low Level<br>Output Voltage | 4.5<br>5.5             | 0.001            | 0.1<br>0.1   | 3.15                     | 0.1<br>0.1                 | 3.15<br>3.85                       | 4.5 1.0 2.26<br>5.5 1.0 2.75    | Veg            | $I_{OUT} = 50 \mu A$   |
|                       | = TUOV<br>00V 10 V                  | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.9<br>1.35<br>1.65      | 0.50<br>0.50               | 0.9<br>1.35<br>1.65                | 3.8 0.44<br>3 0.44              | ved wed        | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub> a CB- | Maximum Input<br>Leakage Current    | 5.5                    | F                | ±0.1         | 2.6<br>4.4               | ±1.0                       | 2.9<br>4.4                         | 68.5<br>84.4 ± 1.0              | μА             | $V_{I} = V_{CC}$ , GND   |
| ICCT                  | Maximum<br>I <sub>CC</sub> /Input   | 5.5                    | 0.6              |              | 8.8                      | 1.6                        | 5.4                                | 1.5                             | mA             | $V_I = V_{CC} - 2.1V$  |
| I <sub>OLD</sub>      | †Minimum Dynamic                    | 5.5                    |                  |              | 2.4                      | 50                         | 2.56                               | 75                              | mA             | V <sub>OLD</sub> = 1.65V Max   |
| IOHD                  | Output Current                      | 5.5                    |                  |              | 7.6                      | -50                        | 88.6                               | -75                             | mA             | V <sub>OHD</sub> = 3.85V Min   |
| Icc Au o              | Maximum Quiescent<br>Supply Current | 5.5                    |                  | 4.0          | 1.0                      | 80.0                       | 1.0                                | 40.0                            | μΑ             | $V_{IN} = V_{CC}$ or GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

# AC Electrical Characteristics: See Section 2 for waveforms

|                  | PARCT   | 1                 | SAAC   | 74AC        |              | 54         | AC                      | 74         | AC                      |       |             |
|------------------|---|-------------------|--|-------------|--------------|------------|-------------------------|------------|-------------------------|-------|-------------|
| Symbol           | Parameter   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             |              | to +       | −55°C<br>125°C<br>50 pF | to H       | -40°C<br>-85°C<br>50 pF | Units | Fig.<br>No. |
|                  | xaM niM   | KsM               | Min  | Тур         | Max          | Min        | Max                     | Min        | Max                     |       |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency  | 3.3<br>5.0        | 125<br>150                                       | 150<br>175  | 210          | 65<br>95   | 0.8                     | 100<br>125 | mum Clock<br>annoy      | MHz   | NEO!        |
| t <sub>PLH</sub> | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$                                     | 3.3<br>5.0        | 4.0<br>2.5                                       | 8.0<br>6.0  | 13.5<br>10.0 | 1.0<br>1.0 | 17.5<br>12.0            | 3.5<br>2.0 | 16.0<br>10.5            | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $CP_n$ to $Q_n$ or $\overline{Q}_n$                                     | 3.3<br>5.0        | 3.0<br>2.0                                       | 8.0<br>6.0  | 14.0<br>10.0 | 1.0        | 13.5<br>10.0            | 3.0<br>1.5 | 14.5<br>10.5            | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 3.3<br>5.0        | 3.0<br>2.5                                       | 8.0<br>6.0  | 12.0<br>9.0  | 1.0        | 13.0<br>9.5             | E Marin    | 13.0<br>10.0            | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 3.3<br>5.0        | 3.0<br>2.0                                       | 10.0<br>7.5 | 12.0<br>9.5  | 1.0<br>1.0 | 14.0<br>10.5            | 3.0<br>2.0 | 13.5<br>10.5            | ns    | 2-3, 4      |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

|                  |       | 0°05- = AT 3                                       | PAR I             | 744  | C          | 54AC   | 74AC   |       |      |
|------------------|-------|--|-------------------|--|------------|--|--|-------|------|
| Symbol           | Unite | Parameter  | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|                  | -     |  | C 303 ISI 18439   | Тур  | 1          | Guaranteed M   | inimum   | Calum |      |
| ts               |       | Time, HIGH or LOW $\overline{K}_n$ to $CP_n$       | 3.3<br>5.0        | 3.5<br>2.0                                       | 6.5<br>4.5 | 8.0<br>5.5   | 7.5<br>5.0   | ns    | 2-7  |
| th               |       | Time, HIGH or LOW                                  | 3.3<br>5.0        | -1.5<br>-0.5                                     | 0 0.5      | 0<br>0.5   | 0 90 or n  | ns    | 2-7  |
| tw               |       | Width S <sub>Dn</sub>                              | 3.3<br>5.0        | 2.0  | 4.0<br>3.5 | 8.0<br>5.5   | 4.5<br>3.5   | ns    | 2-3  |
| t <sub>rec</sub> | 1     | very Time<br>or S <sub>Dn</sub> to CP <sub>n</sub> | 3.3<br>5.0        | -2.5<br>-1.5                                     | 0          | 0.5<br>0.5   | 0 0 00   | ns    | 2-3, |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

# 

|                  |   |  |                   | BAAR   | 74ACT |      | 54A  | СТ    | 74  | ACT                       |       |             |
|------------------|---|--|-------------------|--|-------|------|--|-------|-----|---------------------------|-------|-------------|
| Symbol           | Units                                       | Parameter of   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | T <sub>A</sub> = -<br>to + 1<br>C <sub>L</sub> = | 125°C |     | -40°C<br>+85°C<br>= 50 pF | Units | Fig.<br>No. |
|                  |   | xsiii niii   | Mass              | Min  | Тур   | Max  | Min  | Max   | Min | Max                       |       |             |
| f <sub>max</sub> | 04484                                       | imum Clock<br>juency   | 5.0               | 145  | 210   |      | 85   |       | 125 |                           | MHz   | finan       |
| tpLH             | C 20 10 10 10 10 10 10 10 10 10 10 10 10 10 | agation Delay<br>to Q <sub>n</sub> or Q <sub>n</sub>               | 5.0               | 4.0  | 7.0   | 11.0 | 1.0  | 14.0  | 3.5 | 13.0                      | ns    | 2-3, 4      |
| t <sub>PHL</sub> |   | agation Delay<br>to Q <sub>n</sub> or Q <sub>n</sub>               | 5.0               | 3.0  | 6.0   | 10.0 | 1.0  | 12.0  | 2.5 | 11.5                      | ns    | 2-3, 4      |
| t <sub>PLH</sub> | X5.00                                       | eagation Delay or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 5.0               | 2.5  | 5.5   | 9.5  | 1.0  | 11.5  | 2.0 | 10.5                      | ns    | 2-3, 4      |
| <sup>t</sup> PHL |   | eagation Delay or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 5.0               | 2.5  | 6.0   | 10.0 | 1.0  | 12.5  | 2.0 | 11.5                      | ns    | 2-3, 4      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# AC Operating Requirements: See Section 2 for waveforms

|                  |           | 744.0  | SAAC              | 74A  | СТ  | 54ACT  | 74ACT                        |       |             |
|------------------|-----------|--|-------------------|--|-----|--|------------------------------|-------|-------------|
| Symbol           | stinU     | Parameter A  | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |     | $T_A = -55^{\circ}$<br>to + 125°C<br>$C_L = 50 \text{ pl}$ | to +85°C                     | Units | Fig.<br>No. |
|                  |           | 7g 88 = 30   | 4 00 = £          | Тур  | _   | Guarantee  | d Minimum                    |       |             |
| ts               |           | Time, HIGH or LOW  | 5.0               | 0.5  | 2.0 | 2.5  | VO.J 10   2.5   Smill        | ns    | 2-7         |
| t <sub>h</sub>   |           | Time, HIGH or LOW  | 5.0               | 0 0  | 2.0 | 2.0  | 2.0                          | blons | 2-7         |
| tw               | A 121021C | Width<br>or $\overline{\mathbb{C}}_{Dn}$ or $\overline{\mathbb{S}}_{Dn}$ | 5.0               | 3.0  | 5.0 | 7.0  | 6.0 <sub>Mbh</sub>           | ns    | 2-3         |
| t <sub>rec</sub> | 1         | very Time<br>or $\overline{S}_{Dn}$ to $CP_n$                            | 5.0               | -2.5   | 0   | 0.5  | Son<br>ery Time <sup>0</sup> | ns    | 2-3, 7      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

# Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 35.0 | pF    | V <sub>CC</sub> = 5.0V |



# 54AC/74AC125 • 54ACT/74ACT125 Quad Buffer with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT125 contains four independent non-inverting buffers with TRI-STATE outputs.

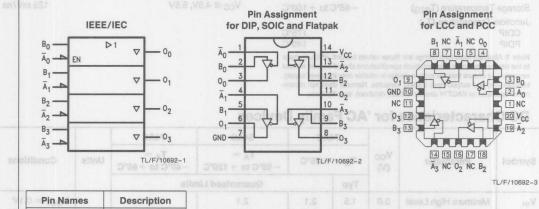
#### **Features**

- Outputs source/sink 24 mA
- 'ACT125 has TTL-compatible outputs

Ordering Code: See Section 8

#### **Logic Symbol**

# Connection Diagrams



| Pin Names                | Description |
|--------------------------|-------------|
| $\overline{A}_n$ , $B_n$ | Inputs      |
| On                       | Outputs     |

#### **Function Table**

| Inpu    | ts | Output |
|---------|----|--------|
| An      | On |        |
| V =beV* | L  | L      |
| L       | Н  | 2H8 -  |
| HHO     | X  | Z      |
|         | 1  | 4.75   |

- H = HIGH Voltage Level
  L = LOW Voltage Level
  Z = HIGH Impedance
  X = Immaterial
  - 6.5 2.7

    6.5 4.60 4.7

    Maximum Low Level 3.0 0.002 0.1 0.1

    Output Voltage 4.6 0.001 0.1

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Vcc) -0.5V to +7.0VDC Input Diode Current (IK)

 $V_1 = -0.5V$ 

 $V_I = V_{CC} + 0.5V$ +20 mA DC Input Voltage (Vi) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Diode Current (IOK)

 $V_0 = -0.5V$ -20 mA  $V_O = V_{CC} + 0.5V$ - 20 mA

-0.5V to  $V_{CC} + 0.5V$ DC Output Voltage (VO)

DC Output Source

or Sink Current (IO) ±50 mA

DC V<sub>CC</sub> or Ground Current per Output Pin (ICC or IGND)

±50 mA -65°C to +150°C Storage Temperature (TSTG)

Junction Temperature (T<sub>J</sub>) CDIP

175°C PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### **Recommended Operating Conditions**

Supply Voltage (Vcc)

2.0V to 6.0V 'AC 'ACT 4.5V to 5.5V Input Voltage (VI) OV to Vcc

Output Voltage (VO)

-20 mA

Operating Temperature (TA) 74AC/ACT -40°C to +85°C 54AC/ACT -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices VIN from 30% to 70% of VCC

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

OV to Vcc

|                 |                                      |                     | 74                      | 1AC                  | 54AC                             | 74AC                            |       | School A  |  |
|-----------------|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|---|--|
| Symbol          | Parameter                            | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |  |
|                 |                                      |                     | Тур                     |                      | Guaranteed Lin                   |                                 |       |   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | V V   | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V sh  | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 |                                      | 3.0<br>4.5<br>5.5   | H                       | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | H     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ $-24 \text{ mA}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V     | I <sub>OUT</sub> = 50 μA  |  |
|                 |                                      | 3.0<br>4.5<br>5.5   |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | ٧     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA                                  |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                 |                         | ±0.1                 | ±1.0                             | ±1.0                            | μΑ    | $V_I = V_{CC}$ , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

### 4

# DC Characteristics for 'AC Family Devices (Continued)

|               | ZIAC                                |                        | DAN7             | 4AC    | 54AC                             | 74AC                            |       |  |  |
|---------------|-------------------------------------|------------------------|------------------|--------|----------------------------------|---------------------------------|-------|--|--|
| Symbol        | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |  |
|               | Ct. = 50 pF                         | 7                      | Тур              |        | Guaranteed Li                    |                                 |       |  |  |
| loz<br>2-3, 4 | Maximum TRI-STATE<br>Current        | 5.5                    | M.               | ±0.5   | 0.9 ±10.0 0                      | ±5.0                            | μΑ    | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , $V_{GND}$<br>$V_{O}$ = $V_{CC}$ , GND |  |
| IOLD          | †Minimum Dynamic                    | 5.5                    |                  |        | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD          | Output Current                      | 5.5                    |                  |        | -50                              | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc           | Maximum Quiescent<br>Supply Current | 5.5                    |                  | 8.0    | 160.0                            | 80.0                            | μA    | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

|                   |  |                        | 74               | ACT          | 54ACT                            | 74ACT                           | 0 + VE 8   | el 8.0 epns Plande V.*  |  |
|-------------------|--|------------------------|------------------|--------------|----------------------------------|---------------------------------|--|---|--|
| Symbol            | Parameter                                  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units  | Conditions  |  |
|                   |  |                        | Тур              | T TO         | Guaranteed Li                    | NA RECO                         | EL ESPACION AND AND AND AND AND AND AND AND AND AN |   |  |
| VIH               | Minimum High Level Input Voltage           | 4.5<br>5.5             | 1.5<br>1.5       | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> M | Maximum Low Level Input Voltage            | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8                              | 0.8                             | ٧  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>   | Minimum High Level<br>Output Voltage       | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | Noise  | $I_{OUT} = -50 \mu\text{A}$   |  |
| 2-3, 4            | 1.0 10.0 ns                                | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | dien De  | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$              |  |
| V <sub>OL</sub> S | Maximum Low Level Output Voltage           | 4.5<br>5.5             | 0.001<br>0.001   | 0.1          | 0.00.1                           | 0.1                             | eldeni<br>V  | $I_{OUT} = 50 \mu A$  |  |
| 2-5<br>2-6        | 1.0 10.5 ns<br>1.0 10.5 ns                 | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | oldssld<br>Ois <b>V</b> ole                        | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{1}OL$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ |  |
| I <sub>IN</sub>   | Maximum Input Leakage Current              | 5.5                    |                  | ±0.1         | ±1.0                             | ±1.0                            | μΑ   | $V_I = V_{CC}$ , GND  |  |
| loz               | Maximum TRI-STATE<br>Current               | 5.5                    |                  | ±0.5         | ± 10.0                           | ±5.0                            | μΑ   | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| ICCT              | Maximum I <sub>CC</sub> /Input             | 5.5                    | 0.6              |              | 1.6                              | 1.5                             | mA   | $V_{I} = V_{CC} - 2.1V$ ‡   |  |
| lold              | †Minimum Dynamic                           | 5.5                    |                  | 37.55        | 50                               | 75                              | mA   | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub>  | Output Current                             | 5.5                    |                  | Rg           | -50                              | 9911 <del>- 75</del> 150 100    | mA   | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc               | Maximum Quiescent VO 8 = 50 Supply Current | 5.5                    |                  | 8.0          | 160.0                            | 80.0                            | μΑ   | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

 $<sup>\</sup>dagger$ Maximum test duration 2.0 ms, one output loaded at a time.

<sup>‡</sup>May be measured per the JEDEC Alternate Method.

Note:  $I_{\mbox{\footnotesize CC}}$  for 54ACT @ 25°C is identical to 74ACT @ 25°C.

# 

|                  |                                     | THAC              |  | 74AC       |             | 044 54  | AC                              | 74/  | AC          |            |             |
|------------------|-------------------------------------|-------------------|--|------------|-------------|---|---------------------------------|--|-------------|------------|-------------|
| Symbol           | Parameter                           | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |             | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |                                 | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ |             | Units      | Fig.<br>No. |
|                  |                                     |                   | Min  | Тур        | Max         | Min   | Max                             | Min  | Max         | mius 1.4   | -           |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 1.0<br>1.0                                       | 6.5        | 9.0<br>7.0  | ±0.±  | 5.5                             | 1.0  | 10.0<br>7.5 | ns         | 2-3, 4      |
| tpHL V88.        | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 1.0  | 6.5<br>5.0 | 9.0<br>7.0  |   | 5.6                             |  | 10.0        | ns         | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time                  | 3.3<br>5.0        | 1.0  | 6.0<br>5.0 | 10.5<br>7.0 | 0.8   | 6.5                             | 1.0  | 11.0        | ns         | 2-5         |
| t <sub>PZL</sub> | Output Enable Time                  | 3.3<br>5.0        | 1.0<br>1.0                                       | 7.5<br>5.5 | 10.0        | output unde   | ruw belaicote<br>s ta bahadi fi | 1.0  | 11.0        | ns         | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 1.0  | 7.5<br>6.5 | 10.0<br>9.0 | d laups to n  | to be less line<br>74AC @ 26°C  | 1.0<br>1.0   | 10.5<br>9.5 | ns and loo | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 1.0  | 7.5<br>6.5 | 10.5        | T Fam   | 01 'AC                          | 1.0  | 11.5<br>9.5 | ns         | 2-6         |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

# AC Electrical Characteristics: See Section 2 for Waveforms

|                  |                                     | 497               | not I bear                                       | Kernoner Ek |      | A STATE OF   |       |  |      |               |        |
|------------------|-------------------------------------|-------------------|--|-------------|------|--|-------|--|------|---------------|--------|
| Vr.o             | = TUOV                              | 0.5               |  | 74ACT       | 100  | 5  | 54ACT |  | CT   | -<br>suminité | Part I |
| Symbol           | 1 4 5 CM 1 1 3 M                    | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |       | $T_A = -40^{\circ}C$<br>$to +85^{\circ}C$<br>$C_L = 50 pF$ |      | Units         | Fig.   |
|                  | 100.00                              | 2.6               | Min  | Тур         | Max  | Min  | Max   | Min  | Max  | or respect    | - 17   |
| tpLH             | Propagation Delay<br>Data to Output | 5.0               | 1.0  | 6.5         | 9.0  | 5,49   | 5,5   | 1.0  | 10.0 | ns            | 2-3, 4 |
| Am AS —          | Propagation Delay<br>Data to Output | 5.0               | 1.0  | 0.07.0      | 9.0  |  | 4.5   | 1.0  | 10.0 | ns            | 2-3, 4 |
| t <sub>PZH</sub> | Output Enable Time                  | 5.0               | 1.0  | 6.0         | 8,5  | 100.0  | 4.6   | 1.0  | 9.5  | ns            | 2-5    |
| t <sub>PZL</sub> | Output Enable Time                  | 5.0               | 1.0  | 7.0         | 9.5  | 100.0  | 5.5   | 1.0  | 10.5 | ns            | 2-6    |
| t <sub>PHZ</sub> | Output Disable Time                 | 5.0               | 1.0  | 7.0         | 9.5  |  |       | 1.0  | 10.5 | ns            | 2-5    |
| t <sub>PLZ</sub> | Output Disable Time                 | 5.0               | 1.0  | 7.5         | 10.0 |  | 4.5   | 1.0  | 10.5 | ns            | 2-6    |

\*Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| \$1/ | Symbol                 | Parameter                        | AC/ACT | Units  | Conditions             | and   |
|------|------------------------|----------------------------------|--------|--------|------------------------|-------|
| 88   | I Vea.t = GJOV         | Am 85                            | Тур    | Office | Conditions             | nic   |
| 100  | Vacin = GHOV           | A Input Capacitance              | 4.5    | pF     | $V_{\rm CC} = 5.0V$    |       |
|      | C <sub>PD</sub> V = MV | Power Dissipation<br>Capacitance | 45.0   | 0.8 pF | V <sub>CC</sub> = 5.0V | ineio |



# 54AC/74AC138 • 54ACT/74ACT138 1-of-8 Decoder/Demultiplexer

# **General Description**

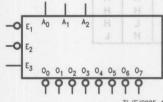
The 'AC/'ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/'ACT138 devices or a 1-of-32 decoder using four 'AC/'ACT138 devices and one inverter.

#### **Features**

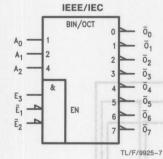
- Demultiplexing capability
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT138 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC138: 5962-87622
  - 'ACT138: 5962-87554

#### Ordering Code: See Section 8

#### **Logic Symbol**



TL/F/9925-1

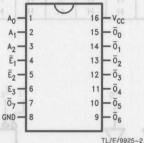


#### **Pin Names** Description $A_0 - A_2$ Address Inputs

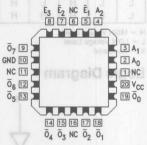
 $\overline{E}_1 - \overline{E}_2$ Enable Inputs Enable Input E<sub>3</sub>  $\overline{O}_0 - \overline{O}_7$ Outputs

#### **Connection Diagrams**

**Pin Assignment** for DIP, Flatpak and SOIC



Pin Assignment for LCC



TI /F/9925-3

#### **Functional Description**

The 'AC/'ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>) and, when enabled, provides eight mutually exclusive active-LOW outputs ( $\overline{O}_0-\overline{O}_7$ ). The 'AC/'ACT138 features three Enable inputs, two active-LOW ( $\overline{E}_1$ ,  $\overline{E}_2$ ) and one active-HIGH (E<sub>3</sub>). All outputs will be HIGH unless  $\overline{E}_1$  and  $\overline{E}_2$  are LOW and E<sub>3</sub> is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines)

decoder with just four 'AC/'ACT138 devices and one inverter (see *Figure 1*). The 'AC/'ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

#### **Truth Table**

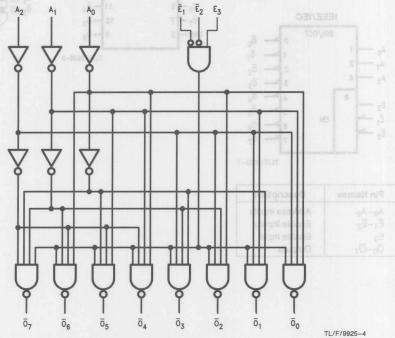
|                |                | colinp         | uts            | s for es       |                | ugni el        |                | <b>16</b>      | Out            | puts           | for hig        | belips y       | ilsebi |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--------|
| Ē <sub>1</sub> | E <sub>2</sub> | E <sub>3</sub> | A <sub>0</sub> | A <sub>1</sub> | A <sub>2</sub> | Ō <sub>0</sub> | Ō <sub>1</sub> | Ō <sub>2</sub> | Ō <sub>3</sub> | O <sub>4</sub> | O <sub>5</sub> | O <sub>6</sub> | 07     |
| Н              | X              | X              | X              | X              | X              | Has Has        | H              | Har            | H              | 2 Hee          | H              | теңес          | veH8   |
| X              | Н              | X              | X              | X              | X              | at Hone        | on He          | H              | Н              | H              | Н              | Hon            | H      |
| X              | X              | L              | X              | X              | X              | a :Hari        | AH-            | Н              | Н              | Н              | Н              | Н              | Н      |
|                |                |                |                | 7554           | 8-5868         | (T138)         | DA"            |                |                |                |                |                |        |
| L              | L              | Н              | L              | L              | L              | L              | Н              | Н              | Н              | Н              | Н              | Н              | Н      |
| L              | L              | Н              | Н              | L              | L              | Н              | L              | Н              | Н              | Н              | Н              | Н              | H      |
| L              | L              | Н              | L              | Н              | L              | Н              | Н              | L              | Н              | Н              | H              | H              | H      |
| L              | L              | Н              | Н              | Н              | L              | Н              | H              | Н              | L              | Н              | Н              | Н              | Н      |
|                |                |                | sms.           | Maria.         | o man          | BOSE           | 22000          |                |                |                |                |                |        |
| L              | Jhen           | Н              | 4019           | L              | Н              | Н              | Н              | Н              | Н              | L              | Н              | Н              | Н      |
| L              | L              | H              | Н              | L              | Н              | H              | Н              | Н              | Н              | Н              | L              | Н              | Н      |
| L              | L              | Н              | L              | Н              | Н              | Н              | Н              | Н              | Н              | Н              | Н              | L              | Н      |
| L              | E.             | H              | Н              | Н              | Н              | Н              | Н              | H              | Н              | Н              | Н              | Н              | L      |

H = HIGH Voltage Level

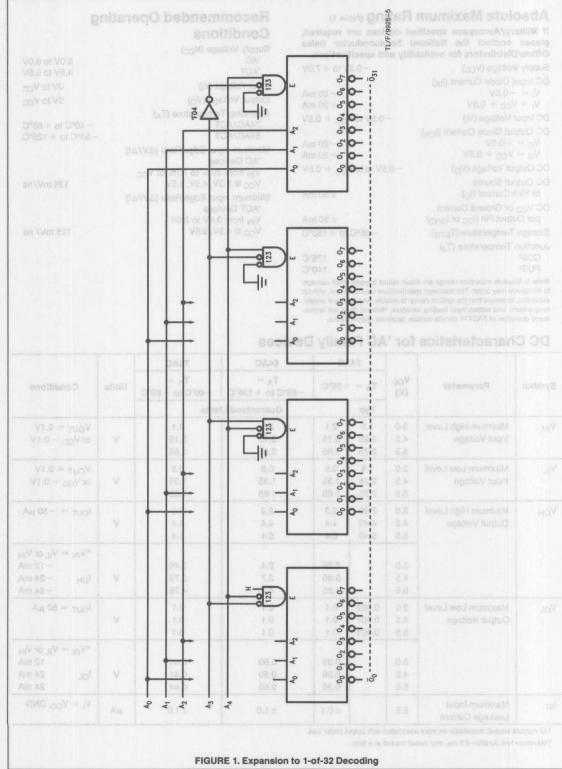
L = LOW Voltage Level

X = Immaterial

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



4-59

# Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )         | -0.5V to $+7.0V$             |
|---|------------------------------|
| DC Input Diode Current (I <sub>IK</sub> ) |                              |
| $V_1 = -0.5V$                             | -20 mA                       |
| $V_I = V_{CC} + 0.5V$                     | + 20 mA                      |
| DC Input Voltage (V <sub>I</sub> )        | $-0.5$ V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK)             |                              |
| $V_{O} = -0.5V$                           | -20 mA                       |
| $V_O = V_{CC} + 0.5V$                     | + 20 mA                      |

DC Output Voltage ( $V_O$ ) -0.5V to to  $V_{CC}+0.5V$  DC Output Source or Sink Current ( $I_O$ )  $\pm$  50 mA

DC  $V_{CC}$  or Ground Current per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}$ C to  $+150^{\circ}$ C Junction Temperature ( $T_{JJ}$ )

CDIP 175°C PDIP 140°C Note 1: Absolute maximum ratings are those values beyond which damage

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

# Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT   | 2.0V to 6.0V<br>4.5V to 5.5V      |
|--|-----------------------------------|
| Input Voltage (V <sub>I</sub> )  | 0V to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )   | 0V to V <sub>CC</sub>             |
| Operating Temperature (T <sub>A</sub> )<br>74AC/ACT<br>54AC/ACT  | -40°C to +85°C<br>-55°C to +125°C |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'AC Devices $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @ 3.3V, 4.5V, 5.5V | 125 mV/ns                         |
| Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices   |                                   |

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ ns

|                 |                                      |                                 | 74                      | AC                   |                                  | 54AC                 | 74AC                            |       |   |  |
|-----------------|--------------------------------------|---------------------------------|-------------------------|----------------------|----------------------------------|----------------------|---------------------------------|-------|---|--|
| Symbol          | Parameter                            | Vcc<br>(V)<br>3.0<br>4.5<br>5.5 | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C |                      | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |  |
|                 |                                      |                                 | Тур                     |                      |                                  | Guaranteed Li        | mits                            |       |   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  |                                 | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | Lat                              | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5               | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 26                               | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5               | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 3                                | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4               | ٧     | $I_{OUT} = -50 \mu A$   |  |
|                 |                                      | 3.0<br>4.5<br>5.5               | Ŷ                       | 2.56<br>3.86<br>4.86 |                                  | 2.4<br>3.7<br>4.7    | 2.46<br>3.76<br>4.76            | ٧     | $V_{\rm IN} = V_{\rm IL} \text{ or } V_{\rm IH}$ $-12 \text{ mA}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5               | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    |                                  | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1               | ٧     | $I_{OUT} = 50 \mu A$  |  |
|                 |                                      | 3.0<br>4.5<br>5.5               | 3.5.5.3                 | 0.36<br>0.36<br>0.36 |                                  | 0.50<br>0.50<br>0.50 | 0.44<br>0.44<br>0.44            | ٧     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA                                    |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                             |                         | ±0.1                 | C1 (S04)                         | ±1.0                 | ±1.0                            | μΑ    | $V_{I} = V_{CC}$ , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## 4

# DC Characteristics for 'AC Family Devices (Continued)

|        | TAAC                                |                        | 74               | AC     | 54AC                             | 74AC                            |       |  |
|--------|-------------------------------------|------------------------|------------------|--------|----------------------------------|---------------------------------|-------|--|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                               |
|        | Re 08 = 10                          | T                      | Тур              | 302    | Guaranteed Lir                   |                                 |       |  |
| lold   | †Minimum Dynamic                    | 5.5                    | ADDAY<br>ALGORA  | 6100   | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max             |
| IOHD   | Output Current                      | 5.5                    | 12.0             | 1.0    | -50                              | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min             |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | 15.0             | 8.0    | 160.0                            | 80.0                            | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

|                  | .5 14.0                             |                        | 74A                    | CT           | 54ACT             | 74ACT                                  | relation        | ipelL Propagati   |
|------------------|-------------------------------------|------------------------|------------------------|--------------|-------------------|--|-----------------|---|
| Symbol           | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |              | -55°C to + 125°C  | T <sub>A</sub> = 0.8<br>-40°C to +85°C | Units           | Conditions  |
|                  |                                     |                        | Тур                    |              | Guaranteed Li     | mits                                   | V2.0± V0        | Voltage Range 5.0 is 5.   |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5             | 2.0          | 2.0               | 2.0                                    | sn <sub>V</sub> | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5             | 0.8          | 0.8               | 0.8                                    | ٧               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                  |
| V <sub>OH</sub>  | Minimum High Level Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4   | 4.4<br>5.4        | 4.4<br>5.4                             | ٧               | $I_{OUT} = -50 \mu\text{A}$   |
| 2-3, 4           | en a.fr a.                          | 4.5<br>5.5             | 12.5                   | 3.86<br>4.86 | 3.70 0.7<br>4.70  | 3.76 d<br>4.76                         | on Delay        | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage    | 4.5<br>5.5             | 0.001<br>0.001         | 0.1          | 0.1<br>0.1        | 0.1                                    | V               | I <sub>OUT</sub> = 50 μA  |
|                  | 12.5 ns                             |                        | 13.5                   | 1.0          | 8.0 11.8          | 5,0 2.5                                | , Ō :           | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>                   |
| 2-8, 4           | .0 12.5 ns                          | 4.5<br>5.5             | 12.5                   | 0.36<br>0.36 | 0.50<br>8.11 0.50 | 0.44<br>0.2 0.44                       | valeV no        | I <sub>OL</sub> 24 mA   |
| 2-3, 4           | Maximum Input<br>Leakage Current    | 5.5                    | 14.0                   | ±0.1         | 0.S1 ± 1.0 0.8    | a.s ±1.0 <sub>0.3</sub>                | μΑ              | $V_{I} = V_{CC}$ , GND  |
| Ісст             | Maximum<br>I <sub>CC</sub> /Input   | 5.5                    | 0.6                    | 1.0          | a.or 1.6 a.o      | 0.9 1.5 0.8                            | mA              | $V_I = V_{CC} - 2.1V$   |
| IOLD             | †Minimum Dynamic                    | 5.5                    |                        |              | 50                | 75                                     | mA              | V <sub>OLD</sub> = 1.65V Max  |
| I <sub>OHD</sub> | Output Current                      | 5.5                    |                        |              | -50               | -75                                    | mA              | V <sub>OHD</sub> = 3.85V Min  |
| lcc              | Maximum Quiescent<br>Supply Current | 5.5                    | 0                      | 8.0          | 160.0             | 80.0                                   | μΑ              | V <sub>IN</sub> = V <sub>CC</sub> or GND                                |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time. Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

|                  |  | (4)        |            | or – an hu  |                    | C <sub>L</sub> = | 50 pF        | C <sub>L</sub> = | 50 pF        |                  | NO.    |
|------------------|--|------------|------------|-------------|--------------------|------------------|--------------|------------------|--------------|------------------|--------|
|                  |  |            | Min        | Тур         | Max                | Min              | Max          | Min              | Max          |                  |        |
| t <sub>PLH</sub> | Propagation Delay $A_n$ to $\overline{O}_n$                                | 3.3<br>5.0 | 1.5<br>1.5 | 8.5<br>6.5  | 13.0<br>9.5        | 1.0<br>1.0       | 16.0<br>12.0 | 1.5<br>1.5       | 15.0<br>10.5 | ns               | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay An to On   | 3.3<br>5.0 | 1.5<br>1.5 | 8.0<br>6.0  | 12.5<br>9.0        | 1.0<br>1.0       | 15.0<br>11.5 | 1.5<br>1.5       | 14.0<br>10.5 | nbasM<br>ns      | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$ | 3.3<br>5.0 | 1.5<br>1.5 | 11.0<br>8.0 | 15.0 <sup>11</sup> | 1.0              | 16.5<br>13.0 | 1.5<br>1.5       | 16.0<br>12.0 | ns               | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$ | 3.3<br>5.0 | 1.5<br>1.5 | 9.5<br>7.0  | 13.5<br>9.5        | 1.0<br>1.0       | 15.5<br>12.0 | 1.5<br>1.5       | 15.0<br>10.5 | DA- <b>ns</b> et | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay E <sub>3</sub> to O <sub>n</sub>                         | 3.3<br>5.0 | 1.5<br>1.5 | 11.0<br>8.0 | 15.5               | 1.0              | 17.0<br>13.5 | 1.5<br>1.5       | 16.5<br>12.5 | ns               | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay E <sub>3</sub> to O <sub>n</sub>                         | 3.3<br>5.0 | 1.5<br>1.5 | 8.5<br>6.0  | 13.0<br>8.0        | 1.0              | 15.0<br>11.0 | 1.5<br>1.0       | 14.0<br>9.5  | ns               | 2-3, 4 |

Guaranteed Limits

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                      | D0 v 10  | - 0               |     | 74ACT                  | 54   | ACT  | 74   | ACT  | S PERGENT | 4.7    |
|----------------------|--|-------------------|-----|------------------------|--|------|--|------|-----------|--------|
| Symbol               | Parameter  | V <sub>CC</sub> * |     | C <sub>L</sub> = +25°C | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units     | Fig.   |
|                      |  |                   | Min | Тур Мах                | Min  | Max  | Min  | Max  | Output    |        |
| tpLH                 | Propagation Delay A <sub>n</sub> to $\overline{O}_n$                       | 5.0               | 1.5 | 7.0 07.8 10.5          | 1.0  | 12.5 | 1.5  | 11.5 | ns        | 2-3, 4 |
| t <sub>PHL</sub>     | Propagation Delay  | 5.0               | 1.5 | 6.5                    | 1.0  | 12.5 | 1.5  | 11.5 | ns        | 2-3, 4 |
| t <sub>PLH</sub>     | Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$ | 5.0               | 2.5 | 8.0 11.5               | 1.0  | 13.5 | 2.0  | 12.5 | ns        | 2-3, 4 |
| t <sub>PHL</sub>     | Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$ | 5.0               | 2.0 | 7.5 08.0 11.5          | 1.0  | 12.5 | 2.0  | 12.5 | ns        | 2-3, 4 |
| t <sub>PLH3/10</sub> | Propagation Delay E <sub>3</sub> to On                                     | 5.0               | 2.5 | 8.0 12.0               | 1.0  | 14.0 | 2.0  | 13.0 | ns        | 2-3, 4 |
| t <sub>PHL</sub>     | Propagation Delay<br>E <sub>3</sub> to On                                  | 5.0               | 2.0 | 6.5 8.1 10.5           | 1.0  | 12.0 | 1.5  | 11.5 | ns        | 2-3, 4 |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 60.0 | pF    | V <sub>CC</sub> = 5.0V |

<sup>\*</sup>Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V



# 54AC/74AC139 • 54ACT/74ACT139 Dual 1-of-4 Decoder/Demultiplexer

#### **General Description**

The 'AC/'ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'AC/'ACT139 can be used as a function generator providing all four minterms of two variables.

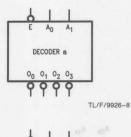
#### **Features**

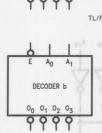
- Multifunction capability
- Two completely independent 1-of-4 decoders
- Active LOW mutually exclusive outputs
- Outputs source/sink 24 mA
- 'ACT139 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - —'AC139: 5962-87623
  - 'ACT139: 5962-87553

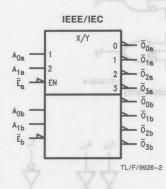
Ordering Code: See Section 8

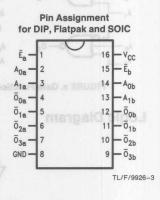
**Logic Symbols** 

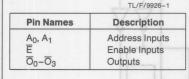
#### **Connection Diagrams**

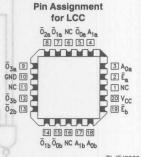












TL/F/9926-4

#### **Functional Description**

The 'AC/'ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A<sub>0</sub>-A<sub>1</sub>) and provides four mutually exclusive active-LOW outputs  $(\overline{O}_0 - \overline{O}_3)$ . Each decoder has an active-LOW enable  $(\overline{E})$ . When E is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'AC/'ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

# Truth Table

|      | Inputs         |                | HUDURO         | Outputs        |                |                |  |  |  |  |
|------|----------------|----------------|----------------|----------------|----------------|----------------|--|--|--|--|
| Ē    | A <sub>0</sub> | A <sub>1</sub> | Ō <sub>0</sub> | Ō <sub>1</sub> | Ō <sub>2</sub> | O <sub>3</sub> |  |  |  |  |
| н    | X              | X              | · H            | NH-            | OH N           | э Н            |  |  |  |  |
| L    | L              | L              | No Const       | Н              | Н              | Н              |  |  |  |  |
| nu ( | HO             | DOLO           | HA             | L              | ALI            | Н              |  |  |  |  |
| L    | L              | Н              | Н              | Н              | L              | Н              |  |  |  |  |
| L    | Н              | H              | Н.             | Ho s           | H              | 2              |  |  |  |  |

- H = HIGH Voltage Level
- L = LOW Voltage Level
  X = Immaterial
- X = Immaterial each scoepling two inputs and providing four mutually-ex-

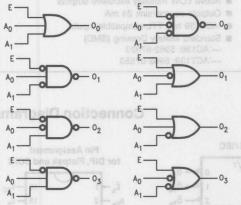
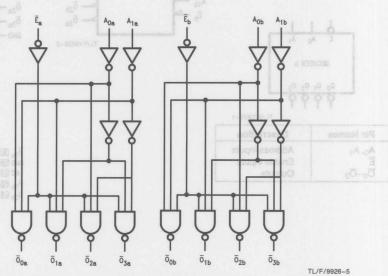


FIGURE a. Gate Functions (Each Half)

# TL/F/9926-6

# **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

0.5V to +7.0V Supply Voltage (VCC) DC Input Diode Current (IIK)  $V_1 = -0.5V$ -20 mA  $V_I = V_{CC} + 0.5V$ +20 mA -0.5V to  $V_{CC} + 0.5$ V DC Input Voltage (V<sub>I</sub>) DC Output Diode Current (IOK)  $V_0 = -0.5V$ -20 mA

 $V_0 = V_{CC} + 0.5V$ +20 mA DC Output Voltage (Vo) -0.5V to to  $V_{CC} + 0.5$ V DC Output Source

DC V<sub>CC</sub> or Ground Current per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) Storage Temperature (TSTG)

or Sink Current (IO)

Junction Temperature (T,I) CDIP PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating **Conditions**

Supply Voltage (V<sub>CC</sub>) 2.0V to 6.0V 'AC 4.5V to 5.5V 'ACT OV to Vcc Input Voltage (VI) 0V to V<sub>CC</sub> Output Voltage (VO) Operating Temperature (TA)

-40°C to +85°C 74AC/ACT -55°C to +125°C 54AC/ACT

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

VIN from 30% to 70% of VCC Vcc. @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

VIN from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

#### **DC Characteristics for 'AC Family Devices**

| VI                    |                    | - 8             | 74               | AC     | 8.0          | 54AC             | 8.0   | 1.5          | 74AC                       |         | LI woul m  | umixsivi           |                                    |
|-----------------------|--------------------|-----------------|------------------|--------|--------------|------------------|-------|--------------|----------------------------|---------|------------|--------------------|------------------------------------|
| Symbol                | Parameter          | V <sub>CC</sub> | T <sub>A</sub> = | + 25°C | - 5          | T <sub>A</sub> = |       |              | T <sub>A</sub> =<br>C to + | 85°C    | Units      | Con                | ditions                            |
|                       |                    |                 | Тур              |        | Guaranteed L |                  | imits |              |                            | egatio) |            |                    |                                    |
| V <sub>IHI</sub> V to | Minimum High Level | 3.0             | 1.5              | 2.1    |              | 2.1              |       |              | 2.1                        |         |            | V <sub>OUT</sub> = | 0.1V                               |
| -24 mA                | Input Voltage      | 4.5             | 2.25             | 3.15   | 3.70         | 3.15             |       |              | 3.15                       |         | V          | or V <sub>CC</sub> |                                    |
| Am 18-                |                    | 5.5             | 2.75             | 3.85   | 4,70         | 3.85             |       |              | 3.85                       |         |            |                    |                                    |
| VIL Aq                | Maximum Low Level  | 3.0             | 0 1.5            | 0.9    | 0.1          | 0.9              | 1.0   | 100.0        | 0.9                        | leve    | J woJ n    | Vout =             | 0.1V JoV                           |
|                       | Input Voltage      | 4.5             | 2.25             | 1.35   | 1.0          | 1.35             |       | 100.0        | 1.35                       |         | a Vilo     | or Vcc             | - 0.1V                             |
| uiV to                |                    | 5.5             | 2.75             | 1.65   |              | 1.65             |       |              | 1.65                       |         |            |                    |                                    |
| VoH                   | Minimum High Level | 3.0             | 2.99             | 2.9    | 08.0         | 2.9              | 0.36  |              | 2.9                        |         |            | I <sub>OUT</sub> = | -50 μΑ                             |
| Am AS                 | Output Voltage     | 4.5             | 4.49             | 4.4    | 0.80         | 4.4              |       |              | 4.4                        |         | V          |                    |                                    |
|                       |                    | 5.5             | 5.49             | 5.4    |              | 5.4              |       |              | 5.4                        |         | tuned or   | Maximus            |                                    |
| GND                   |                    | U.              | 7                |        | が出           |                  | TAZ   | 1            | G,G                        |         | Current    | *VIN =             | VIL or VIH                         |
| WER -                 |                    | 3.0             |                  | 2.56   | -            | 2.4              |       |              | 2.46                       |         |            | umicsM             | -12 mA                             |
| 9.1.05                |                    | 4.5             |                  | 3.86   | 1.6          | 3.7              |       | 8.0          | 3.76                       |         | V          | Іон                | -24 mA                             |
|                       |                    | 5.5             |                  | 4.86   | 000          | 4.7              |       |              | 4.76                       |         |            | 99.4.33            | -24 mA                             |
| V <sub>OL</sub>       | Maximum Low Level  | 3.0             | 0.002            | 0.1    | 90           | 0.1              |       |              | 0.1                        | 1 0111  | m cayman   | I <sub>OUT</sub> = | 50 μΑ                              |
| MIN V28.              | Output Voltage     | 4.5             | 0.001            | 0.1    | - 60         | 0.1              |       |              | 0.1                        |         | V          | 10010              | GHO                                |
|                       |                    | 5.5             | 0.001            | 0.1    | nas          | 0.1              |       |              | 0.1                        |         | n Oulest   | umixaM             |                                    |
|                       |                    |                 |                  |        |              |                  |       |              | 1                          |         | - Inemi    | *VIN =             | V <sub>IL</sub> or V <sub>IH</sub> |
|                       |                    | 3.0             |                  | 0.36   |              | 0.50             |       | due rilliw b | 0.44                       |         | e abiorism | traded; th         | 12 mA                              |
|                       |                    | 4.5             |                  | 0.36   |              | 0.50             |       | t at a title | 0.44                       |         | emy s n    | loL                | 24 mA                              |
|                       |                    | 5.5             |                  | 0.36   |              | 0.50             |       | D'85 R       | 0.44                       |         | 28°C is id | OF SKACT O         | 24 mA                              |

±50 mA

175°C

140°C

±50 mA

-65°C to +150°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol                  | Parameter                           | V <sub>CC</sub><br>(V) | $T_A = +25^{\circ}C$ $T_A = T_A = -55^{\circ}C \text{ to } +125^{\circ}C -40^{\circ}C \text{ to } +85^{\circ}C$ |           |                   | Units | Conditions |  |  |
|-------------------------|-------------------------------------|------------------------|---|-----------|-------------------|-------|------------|--|--|
| ooV of Y                |                                     |                        | Тур   | alloV tuq | Guaranteed Limits |       | sell ther  | DC Input Diode Cur                       |  |
| I <sub>IN</sub> oV of V | Maximum Input<br>Leakage Current    | 5.5                    | lago (Vo)<br>Temperatu  | ±0.1      | ±1.0              | ±1.0  | μА         | $V_I = V_{CC}$ , GND                     |  |
| lold                    | †Minimum Dynamic                    | 5.5                    | 13  | A NOAJES  | 50                | 75 (w | mA         | V <sub>OLD</sub> = 1.65V Max             |  |
| I <sub>OHD</sub>        | Output Current                      | 5.5                    | agbil Juqn  | nimum I   | -50               | -75   | mA         | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc<br>an\vm            | Maximum Quiescent<br>Supply Current | 5.5                    | 00% to 70<br>30% to 70  | 8.0       | 160.0             | 80.0  | μА         | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $l_{IN}$  and  $l_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $l_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

|                                 |                                     |            | 744                                    | ACT                   | 54ACT                       | 74ACT                           |                    | 9109   |  |
|---------------------------------|-------------------------------------|------------|--|-----------------------|-----------------------------|---------------------------------|--------------------|--|--|
| Symbol                          | ymbol Parameter                     |            | / <sub>CC</sub> T <sub>A</sub> = +25°C |                       | ***                         | T <sub>A</sub> = -40°C to +85°C | Units              | Conditions   |  |
|                                 |                                     |            | Тур                                    | Typ Guaranteed Limits |                             |                                 | o alluctio M       | mend operation of PACT   |  |
| V <sub>IH</sub>                 | Minimum High Level<br>Input Voltage | 4.5<br>5.5 | 1.5<br>1.5                             | 2.0<br>2.0            | 2.0<br>2.0                  | 2.0<br>2.0                      | V                  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>                 | Maximum Low Level Input Voltage     | 4.5<br>5.5 | 1.5<br>1.5                             | 0.8                   | 0.8<br>0.8                  | 0.8                             | V                  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VoH                             | Minimum High Level Output Voltage   | 4.5<br>5.5 | 4.49<br>5.49                           | 4.4<br>5.4            | 4.4<br>5.4                  | 4.4 5.4                         | V                  | $I_{OUT} = -50 \mu\text{A}$  |  |
|                                 | Vout =                              | 4.5<br>5.5 |  | 3.86<br>4.86          | 3.70 4.8<br>4.70 4.8        | 3.76                            | figh Leve<br>ige V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$         |  |
| V <sub>OL</sub> V <sub>LO</sub> | Maximum Low Level<br>Output Voltage | 4.5<br>5.5 | 0.001                                  | 0.1<br>0.1            | 8.6 0.1 9.0<br>6.1 0.1 38.1 | 4.5 1.0 2.25                    | ve V               | $I_{OUT} = 50 \mu A$   |  |
| Ац 08-                          | = TUO! V                            | 4.5<br>5.5 |  | 0.36<br>0.36          | 0.50<br>0.50                | 0.44                            | fighy.eve          | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$ |  |
| NI OF VIH                       | Maximum Input<br>Leakage Current    | 5.5        |  | ±0.1                  | ±1.0                        | 94.8 3.8<br>± 1.0               | μΑ                 | $V_{I} = V_{CC}$ , GND   |  |
| ICCT                            | Maximum<br>I <sub>CC</sub> /Input   | 5.5        | 0.6                                    |                       | 1.6 88.8                    | 1.5 3.4                         | mA                 | $V_I = V_{CC} - 2.1V$  |  |
| IOLD                            | †Minimum Dynamic                    | 5.5        |  |                       | 50                          | 75                              | mA                 | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub>                | Output Current                      | 5.5        |  |                       | -50                         | -75                             | mA                 | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc                             | Maximum Quiescent<br>Supply Current | 5.5        |  | 8.0                   | 160.0                       | 80.08                           | μΑ                 | V <sub>IN</sub> = V <sub>CC</sub> or GND                                       |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| Symbol           | Parameter  | (V)        |            | $A = +25$ $C_L = 50 p$ |             | St. Moral Hills | 125°C<br>50 pF | 20.000     | 85°C<br>50 pF | Units | Fig.<br>No. |
|------------------|--|------------|------------|------------------------|-------------|-----------------|----------------|------------|---------------|-------|-------------|
|                  |  |            | Min        | Тур                    | Max         | Min             | Max            | Min        | Max           | itua  | n1-8        |
| t <sub>PLH</sub> | Propagation Delay  An to On                            | 3.3<br>5.0 | 4.0<br>3.0 | 8.0<br>6.5             | 11.5<br>8.5 | 1.0<br>1.0      | 14.5<br>11.0   | 3.5<br>2.5 | 13.0<br>9.5   | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay                                      | 3.3<br>5.0 | 3.0        | 7.0<br>5.5             | 10.0<br>7.5 | 1.0             | 12.5           | 2.5        | 11.0<br>8.5   | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay $\overline{E}_n$ to $\overline{O}_n$ | 3.3<br>5.0 | 4.5<br>3.5 | 9.5<br>7.0             | 12.0<br>8.5 | 1.0<br>1.0      | 14.5<br>11.0   | 3.5<br>3.0 | 13.0<br>10.0  | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $\overline{E}_n$ to $\overline{O}_n$ | 3.3<br>5.0 | 4.0<br>2.5 | 8.0<br>6.0             | 10.0<br>7.5 | 1.0             | 12.5<br>10.0   | 3.0<br>2.5 | 11.0<br>8.5   | ns    | 2-3, 4      |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

## AC Electrical Characteristics: See Section 2 for waveforms

|                  | Assignment                                  | Pin    |  | 74ACT | namnglee  | A nin 54/ | ACT  | 74  | ACT   |             |        |
|------------------|---|--------|--|-------|---|-----------|--|-----|-------|-------------|--------|
| Symbol           | ymbol Parameter                             |        | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ |           | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |     | Units | Fig.<br>No. |        |
|                  | el El Blo                                   | TE TEL | Min  | Тур   | Max   | Min       | Max  | Min | Max   |             | 13     |
| t <sub>PLH</sub> | Propagation Delay $A_n$ to $\overline{O}_n$ | 5.0    | 1.5  | 6.0   | 8.5   | 1.0       | 12.0   | 1.5 | 9.5   | ns          | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay An to On                  | 5.0    | 1.5  | 6.0   | 9.5   | 1.0       | 11.0   | 1.5 | 10.5  | ns          | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay<br>En to On               | 5.0    | 2.5  | 7.0   | 10.0  | 1.0       | 12.5   | 2.0 | 11.0  | ns          | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay                           | 5.0    | 2.0  | 7.0   | 9.5   | 1.0       | 12.0   | 1.5 | 10.5  | ns          | 2-3, 4 |

\*Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions             |
|-----------------|-------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation Capacitance | 40.0 | pF    | V <sub>CC</sub> = 5.0V |

4



# 54AC/74AC151 • 54ACT/74ACT151 8-Input Multiplexer

#### **General Description**

The 'AC/'ACT151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 'AC/'ACT151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

#### **Features**

- Outputs source/sink 24 mA
- 'ACT151 has TTL-compatible inputs

AC Electrical Characteristics: see Section 2 for waveforms

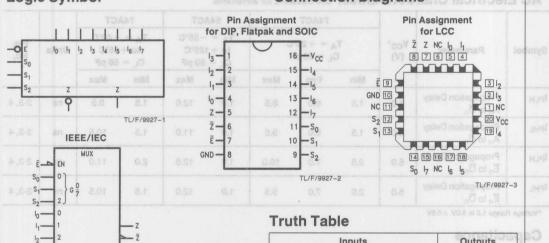
Symbol

- Standard Military Drawing (SMD)—'AC151: 5962-87691
  - -'ACT151: 5962-88756

Ordering Code: See Section 8

# **Logic Symbol**

# Connection Diagrams 10 Isolated A



|   |   |    |     |                | Out            | puts           |                |      |
|---|---|----|-----|----------------|----------------|----------------|----------------|------|
| Ē |   | Q) | T   | S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> | Z              | IZ   |
| H | 1 | 8  | ģi. | X              | X              | age X uga      | Н              | L    |
| 1 | - |    |     | L              | L              | L L            | Ī <sub>0</sub> | 10   |
| L | _ | 0. |     | L              | netaqu         | П              | Ī <sub>1</sub> | 1100 |
| 1 | _ | -  |     | L              | H ®            | Capapitani     | Ī <sub>2</sub> | 12   |
| L | _ |    |     | L              | Н              | Н              | Ī <sub>3</sub> | 13   |
| L |   |    |     | Н              | L              | L              | Ī <sub>4</sub> | 14   |
| L | - |    |     | Н              | L              | Н              | Ī <sub>5</sub> | 15   |
| L | _ |    |     | Н              | Н              | L              | Ī <sub>6</sub> | 16   |
| L |   |    |     | Н              | Н              | H              | Ī <sub>7</sub> | 17   |

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

| Pin Names                      | Description          |
|--------------------------------|----------------------|
| 10-17                          | Data Inputs          |
| S <sub>0</sub> -S <sub>2</sub> | Select Inputs        |
| Ē                              | Enable Input         |
| Z                              | Data Output          |
| Z                              | Inverted Data Output |

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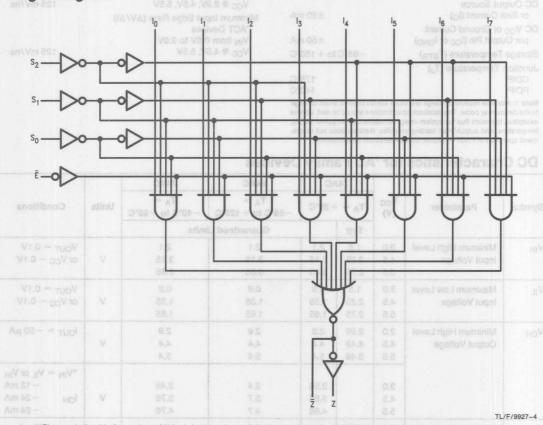
#### **Functional Description**

The 'AC/'ACT151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both true and complementary outputs are provided. The Enable input ( $\overline{E}$ ) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet S_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The 'AC/'ACT151 provides the ability, in one package to select from eight sources of data or control information. By proper manipulation of the inputs, the 'AC/'ACT151 can provide any logic function of four variables and its complement.

# Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| V |  |  | Output Voltage |  |
|---|--|--|----------------|--|
|   |  |  |                |  |
|   |  |  |                |  |

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|   |                                   | AU 1 4.5V to 5.5V  |
|---|-----------------------------------|--|
| DC Input Diode Current (I <sub>IK</sub> )   | .inem                             | Input Voltage (V <sub>I</sub> ) 0V to V <sub>CC</sub>                                    |
| $V_1 = -0.5V$<br>$V_1 = V_{CC} + 0.5V$  | −20 mA<br>+20 mA                  | Output Voltage (V <sub>O</sub> ) 0V to V <sub>CO</sub>                                   |
| DC Input Voltage (V <sub>I</sub> ) DC Output Diode Current (I <sub>OK</sub> )                 | $-0.5V$ to $V_{CC} + 0.5V$        | Operating Temperature (T <sub>A</sub> ) 74AC/ACT -40°C to +85°C 54AC/ACT -55°C to +125°C |
| $V_O = -0.5V$ $V_O = V_{CC} + 0.5V$   | - 20 mA<br>+ 20 mA                | Minimum Input Edge Rate (ΔV/Δt) 'AC Devices  |
| DC Output Voltage (V <sub>O</sub> )   | $-0.5$ V to to $V_{CC}$ + $0.5$ V | V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub>                                       |
| DC Output Source<br>or Sink Current (Io)  | ±50 mA                            | $V_{CC} @ 3.3V, 4.5V, 5.5V$ 125 mV/ns<br>Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) |
| DC V <sub>CC</sub> or Ground Current<br>per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                            | 'ACT Devices<br>V <sub>IN</sub> from 0.8V to 2.0V  |
| Storage Temperature (T <sub>STG</sub> )   | -65°C to +150°C                   | V <sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns   |
| Junction Temperature (T <sub>J</sub> ) CDIP   | 175°C                             | 10000  |
| PDIP  | 140°C                             |  |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

| Symbol          | Parameter                            | V <sub>CC</sub> (V) | 74AC<br>T <sub>A</sub> = +25°C |                       | 54AC                             | 74AC<br>T <sub>A</sub> =<br>-40°C to +85°C | Units | Conditions   |
|-----------------|--------------------------------------|---------------------|--------------------------------|-----------------------|----------------------------------|--|-------|--|
|                 |                                      |                     |                                |                       | T <sub>A</sub> = -55°C to +125°C |  |       |  |
|                 |                                      |                     | Тур                            | Typ Guaranteed Limits |                                  |  |       |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75            | 2.1<br>3.15<br>3.85   | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85                        | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75            | 0.9<br>1.35<br>1.65   | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65                        | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| VOH             | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49           | 2.9<br>4.4<br>5.4     | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4                          | ٧     | $I_{OUT} = -50 \mu A$  |
|                 |                                      | 3.0<br>4.5<br>5.5   |                                | 2.56<br>3.86<br>4.86  | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76                       | ٧     | $^*$ V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> $-12$ mA $_{OH}$ $-24$ mA $_{-24}$ mA          |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001        | 0.1<br>0.1<br>0.1     | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1                          | V     | Ι <sub>ΟυΤ</sub> = 50 μΑ   |
|                 |                                      | 3.0<br>4.5<br>5.5   |                                | 0.36<br>0.36<br>0.36  | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44                       | ٧     | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}OL$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                 |                                | ±0.1                  | ±1.0                             | ±1.0                                       | μΑ    | $V_I = V_{CC}$ , GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### 4

# DC Characteristics for 'AC Family Devices (Continued) Continued Continued

| Symbol           | 74AC                                | V <sub>CC</sub> (V) | 74AC<br>T <sub>A</sub> =<br>+25°C |       | 54AC<br>T <sub>A</sub> =<br>-55°C to + 125°C | 74AC<br>T <sub>A</sub> =<br>-40°C to +85°C | Units | Conditions                               |
|------------------|-------------------------------------|---------------------|-----------------------------------|-------|--|--|-------|--|
|                  | Parameter 40 00 = 30                |                     |                                   |       |  |  |       |  |
|                  |                                     |                     | Тур                               | 76    | Guaranteed                                   | Limits                                     |       |  |
| IOLD             | †Minimum Dynamic<br>Output Current  | 5.5                 | 2000<br>2000                      | THE S | 50   | 75   | mA    | V <sub>OLD</sub> = 1.65V Max             |
| I <sub>OHD</sub> |                                     | 5.5                 | 81                                | 1.0   | 0.01-50 8.8                                  | as -75 oa                                  | mA    | V <sub>OHD</sub> = 3.85V Min             |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5                 | 22                                | 8.0   | 160.0  | 80.0                                       | μΑ    | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

| Symbol                   | Parameter d.                        | V <sub>CC</sub> (V) | 74ACT<br>T <sub>A</sub> =<br>+ 25°C |              | 54ACT                            | 74ACT                           | Units     | Conditions  |
|--------------------------|-------------------------------------|---------------------|-------------------------------------|--------------|----------------------------------|---------------------------------|-----------|---|
|                          |                                     |                     |                                     |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C |           |   |
|                          |                                     |                     | Тур                                 |              | Guaranteed L                     | imits                           | V8.0± V0  | Voltage Range 5.0 is 6  |
| V <sub>IH</sub>          | Minimum High Level<br>Input Voltage | 4.5<br>5.5          | 1.5<br>1.5                          | 2.0          | 2.0                              | 2.0<br>2.0                      | V         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub>          | Maximum Low Level Input Voltage     | 4.5<br>5.5          | 1.5<br>1.5                          | 0.8          | 0.8<br>0.8                       | 0.8<br>0.8                      | V         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub>          | Minimum High Level Output Voltage   | 4.5<br>5.5          | 4.49<br>5.49                        | 4.4<br>5.4   | 4.4 6 5.4                        | 4.4 (V)<br>5.4                  | ٧         | $I_{OUT} = -50 \mu\text{A}$   |
| 2-3,4                    | 3.0 17.0 ns                         | 4.5<br>5.5          | 19,5                                | 3.86<br>4.86 | 3.70 a.s.<br>4.70                | 3.76 A 8<br>4.76                | on Delay  | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |
| VOL                      | Maximum Low Level Output Voltage    | 4.5<br>5.5          | 0.001                               | 0.1          | 12.5 1.0 18.5<br>0.1             | 8.8 0.1 0.8<br>0.1              | V         | $I_{OUT} = 50 \mu\text{A}$  |
| 2-3,4                    | 3.0 16.5 ns                         | 4.5<br>5.5          | 19.5                                | 0.36<br>0.36 | 0.50<br>0.50<br>0.50 76.6        | 0.44<br>0.44                    | gel oV no | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub><br>4.8-8 | Maximum Input Leakage Current       | 5.5                 | 0.21                                | ±0.1         | a.e ±1.0                         | a.s ±1.0 <sub>0.8</sub>         | μА        | $V_I = V_{CC}$ , GND  |
| ГССТ                     | Maximum I <sub>CC</sub> /Input      | 5.5                 | 0.6                                 | 0.1          | 0.9 1.6 0.8                      | a.s 1.5 <sub>0.8</sub>          | mA        | $V_I = V_{CC} - 2.1V$   |
| I <sub>OLD</sub>         | †Minimum Dynamic<br>Output Current  | 5.5                 |                                     |              | 50                               | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max  |
| IOHD                     |                                     | 5.5                 | USI                                 | Ues          | -50                              | -75                             | mA        | V <sub>OHD</sub> = 3.85V Min  |
| Icc e                    | Maximum Quiescent<br>Supply Current | 5.5                 | 12.5                                | 8.0          | 0.01160.0                        | 5.008 9.0                       | μΑ        | $V_{IN} = V_{CC}$ or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{\rm IN}$  and  $I_{\rm CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.  $I_{\rm CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics: See Section 2 for Waveforms OA not applications and OD

|                  |  | 0              | 744        | 74AC   | MARE         | 54  | AC           | 74   | AC           |          |       |
|------------------|--|----------------|------------|--|--------------|---|--------------|--|--------------|----------|-------|
| Symbol           | Parameter  | Parameter Vcc* |            | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ |              | $T_A = -40^{\circ}C$<br>$to +85^{\circ}C$<br>$C_L = 50 pF$ |              | Units    | Fig.  |
|                  |  |                | Min        | Тур  | Max          | Min   | Max          | Min  | Max          |          |       |
| tPLH<br>nim vas. | Propagation Delay $S_n$ to $Z$ or $\overline{Z}$ | 3.3<br>5.0     | 3.0<br>2.5 | 11.5<br>8.5                                      | 18.0<br>13.0 | 1.0   | 22.0<br>15.5 | 3.0<br>2.0   | 20.0<br>15.0 | ns       | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay $S_n$ to $Z$ or $\overline{Z}$ | 3.3<br>5.0     | 2.5<br>2.0 | 12.0<br>8.5                                      | 18.0<br>13.0 | 1.0   | 22.0<br>15.5 | 2.5  | 20.0         | ns<br>ns | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay<br>E to Z or Z                 | 3.3<br>5.0     | 2.5<br>2.0 | 8.0<br>6.0                                       | 13.0<br>10.0 | 1.0<br>1.0  | 15.5<br>12.0 | 2.0<br>1.5   | 14.0<br>11.0 | ns       | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay<br>E to Z or Z                 | 3.3<br>5.0     | 1.5<br>1.5 | 8.5<br>6.5                                       | 13.0<br>10.0 | 1.0<br>1.0  | 15.5<br>12.0 | 1.5<br>1.5   | 14.0<br>11.0 | ns       | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay $I_n$ to Z or $\overline{Z}$   | 3.3<br>5.0     | 2.5<br>1.5 | 9.5<br>7.0                                       | 14.0<br>10.5 | 1.0   | 16.0<br>12.0 | 2.0<br>1.5   | 15.5<br>11.0 | ns       | 2-3,4 |
| tpHL             | Propagation Delay                                | 3.3<br>5.0     | 2.5<br>1.5 | 9.5<br>7.0                                       | 15.0<br>11.0 | 1.0   | 18.0<br>13.0 | 2.0<br>1.5   | 16.0<br>12.0 | ns       | 2-3,4 |

\*Voltage Range 3.3 is 3.3V  $\pm$  0.3V Voltage Range 5.0 is 5.0V  $\pm$  0.5V

### AC Electrical Characteristics: See Section 2 for Waveforms

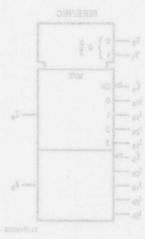
| VIV                 | N V                                       | 0                 |  | 74ACT                   | 5    | 4ACT  | 7   | 4ACT   | Maxi  | VIL   |
|---------------------|---|-------------------|--|-------------------------|------|---|-----|--|-------|-------|
| Symbol              | Parameter                                 | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |                         | to - | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |     | $T_{A} = -40^{\circ}C$ $to +85^{\circ}C$ $C_{L} = 50 \text{ pF}$ |       | Fig.  |
|                     |   |                   | Min  | Тур Мах                 | Min  | Max   | Min | Max  | Outp  |       |
| tpLH                | Propagation Delay S <sub>n</sub> to Z     | 5.0               | 3.5  | 12.5 15.5               | 1.0  | 19.5  | 3.0 | 17.0   | ns    | 2-3,4 |
| t <sub>PHL</sub> Au | Propagation Delay<br>S <sub>n</sub> to Z  | 5.0               | 3.5  | 12.5 10 15.5            | 1.0  | 20.0  | 3.0 | 16.5   | ns    | 2-3,4 |
| tPLH<br>HIV 10 J    | Propagation Delay $S_n$ to $\overline{Z}$ | 5.0               | 3.5  | 12.5 15.0               | 1.0  | 19.5  | 3.0 | 16.5   | ns    | 2-3,4 |
| t <sub>PHL</sub>    | Propagation Delay $S_n$ to $\overline{Z}$ | 5.0               | 4.0  | 12.5 08 0 16.5          | 1.0  | 20.0  | 3.5 | 18.5   | ns    | 2-3,4 |
| t <sub>PLH</sub>    | Propagation Delay E to Z                  | 5.0               | 2.5  | 6.0 <sup>0.1±</sup> 9.5 | 1.0  | 12.0  | 2.5 | 10.0   | ns    | 2-3,4 |
| t <sub>PHL</sub>    | Propagation Delay E to Z                  | 5.0               | 2.5  | 6.0 9.0                 | 1.0  | 12.5  | 2.5 | 10.0   | \_ns  | 2-3,4 |
| t <sub>PLH</sub>    | Propagation Delay E to Z                  | 5.0               | 2.5  | 6.0 8.5                 | 1.0  | 12.0  | 2.5 | 9.5  | ns    | 2-3,4 |
| t <sub>PHL</sub>    | Propagation Delay                         | 5.0               | 3.0  | 6.5 0.00 10.0           | 1.0  | 12.5  | 2.5 | 10.5   | ns    | 2-3,4 |
| t <sub>PLH</sub>    | Propagation Delay                         | 5.0               | 3.5  | 7.5 11.5                | 1.0  | 15.0  | 3.0 | 12.5   | ns    | 2-3,4 |
| t <sub>PHL</sub>    | Propagation Delay                         | 5.0               | 3.5  | 8.0 12.0                | 1.0  | 16.0  | 3.0 | 13.5   | ns ns | 2-3,4 |
| t <sub>PLH</sub>    | Propagation Delay $I_n$ to $\overline{Z}$ | 5.0               | 3.5  | 8.0 12.0                | 1.0  | 15.0  | 3.0 | 13.0   | ns    | 2-3,4 |
| t <sub>PHL</sub>    | Propagation Delay                         | 5.0               | 4.0  | 8.0 12.5                | 1.0  | 16.0  | 3.0 | 14.0   | ns    | 2-3,4 |

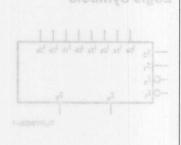
\*Voltage Range 5.0 is 5.0V  $\pm$  0.5V

#### Capacitance

| Symbol          | Parameter                        | Тур  | Units      | Conditions      | mosime?  |
|-----------------|----------------------------------|------|------------|-----------------|----------|
| CIN             | Input Capacitance                | 4.5  | pF         | $V_{CC} = 5.0V$ |          |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 70.0 | ) A pF \ T | $V_{CC} = 5.0V$ | IACITAAC |







| 400000 |             |
|--------|-------------|
|        |             |
|        |             |
|        |             |
|        | <b>图 40</b> |

|    | Description        |
|----|--------------------|
|    | Side A Data Inputs |
|    |                    |
|    |                    |
| Eg |                    |
|    |                    |
|    |                    |
|    |                    |



## 54AC/74AC153 • 54ACT/74ACT153 **Dual 4-Input Multiplexer**

#### **General Description**

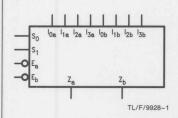
The 'AC/'ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (noninverted) form. In addition to multiplexer operation, the 'AC/ 'ACT153 can act as a function generator and generate any two functions of three variables.

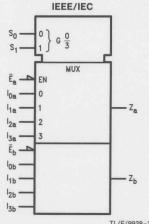
#### **Features**

- Outputs source/sink 24 mA
- 'ACT153 has TTL-compatible inputs
- Standard Military Drawings (SMD)
  - 'AC153: 5962-87625
  - 'ACT153: 5962-87698

Ordering Code: See Section 8

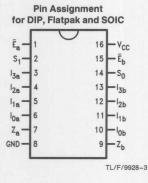
#### **Logic Symbols**

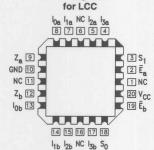




|   | IEEE/IEC   | _              |
|---|--|----------------|
| s <sub>0</sub> —                        | $\begin{bmatrix} 0 \\ 1 \end{bmatrix}$ G $\frac{0}{3}$ | ]              |
| Ē <sub>a</sub> —                        | MUX  |                |
| l <sub>0a</sub> —                       | 1  | Z <sub>a</sub> |
| l <sub>2a</sub>                         | 2  |                |
| l <sub>3a</sub> —<br>Ē <sub>b</sub> — ► | 3  | 1              |
| 10ь —                                   |  |                |
| 1ь —                                    |  | Z <sub>b</sub> |
| l <sub>2b</sub> —                       |  |                |
| 1 <sub>3b</sub> —                       |  |                |
|   |  | TL/F/9928-2    |

## **Connection Diagrams**





Pin Assignment

TL/F/9928-4

| Pin Names                        | Description          |  |  |  |  |
|----------------------------------|----------------------|--|--|--|--|
| I <sub>0a</sub> -I <sub>3a</sub> | Side A Data Inputs   |  |  |  |  |
| I <sub>0b</sub> -I <sub>3b</sub> | Side B Data Inputs   |  |  |  |  |
| S <sub>0</sub> , S <sub>1</sub>  | Common Select Inputs |  |  |  |  |
| Ēa                               | Side A Enable Input  |  |  |  |  |
| E <sub>b</sub>                   | Side B Enable Input  |  |  |  |  |
| Za                               | Side A Output        |  |  |  |  |
| 7h                               | Side B Output        |  |  |  |  |

#### Functional Description

The 'AC/'ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S<sub>0</sub>, S<sub>1</sub>). The two 4-input multiplexer circuits have individual active-LOW Enables ( $\overline{E}_a, \, \overline{E}_b$ ) which can be used to strobe the outputs indepedently. When the Enables ( $\overline{E}_a, \, \overline{E}_b$ ) are HIGH, the corresponding outputs  $Z_a, \, Z_b$ ) are forced LOW. The 'AC/'ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_{a} = \overline{E}_{a} \circ (I_{0a} \circ \overline{S}_{1} \circ \overline{S}_{0} + I_{1a} \circ \overline{S}_{1} \circ S_{0} + a_{00})$$

$$I_{2a} \circ S_{1} \circ S_{0} + I_{3a} \circ S_{1} \circ S_{0}$$

$$Z_{b} = \overline{E}_{b} \circ (I_{0b} \circ \overline{S}_{1} \circ \overline{S}_{0} + I_{1b} \circ \overline{S}_{1} \circ S_{0} + I_{2b} \circ S_{1} \circ S_{0}$$

#### Truth Table Its I mumixs M stuload A

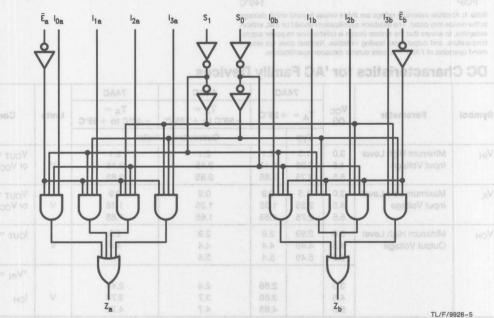
| Select<br>Inputs |                | niconi<br>nd spe | Output         |                |                |                |              |
|------------------|----------------|------------------|----------------|----------------|----------------|----------------|--------------|
| S <sub>0</sub>   | S <sub>1</sub> | Ē                | I <sub>0</sub> | I <sub>1</sub> | l <sub>2</sub> | l <sub>3</sub> | stloV Zqq    |
| X                | X              | Н                | X              | X              | X              | X              | iC tugni     |
| LOS              | L              | L                | L              | X              | X              | X              | L            |
| LOS              | L              | L                | Н              | X              | X              | X              | DOY H        |
| Н                | ool√ o         | A.F.O.           | X              | L<br>(lok)     | X              | X              | Output Vo    |
| H                | L              | L                | X              | Н              | X              | X              | HO           |
| Lus              | Н              | L                | X              | X              | L              | X              | DA FOA       |
| SP +             | OH O           | or LAS           | X              | X              | H              | X              | H            |
| Н                | Н              | L                | X              | X              | X              | BOLRO          | s Judition s |
| H                | Н              | L                | X              | X              | X              | H              | H            |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

|  | 1.0<br>t.0 | 1.0 | 4.5 0.001<br>5.5 0.001 | Output Voltage |
|--|------------|-----|------------------------|----------------|
|  |            |     |                        |                |
|  |            |     |                        |                |

1

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for availab   | omity and specifications.                                 |
|--|---|
| Supply Voltage (V <sub>CC</sub> )  | -0.5V to +7.0V  |
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$<br>$V_I = V_{CC} + 0.5V$<br>DC Input Voltage ( $V_I$ )  | -20 mA<br>+20 mA<br>-0.5V to V <sub>CC</sub> + 0.5V       |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$<br>DC Output Voltage ( $V_O$ )<br>DC Output Source<br>or Sink Current ( $I_O$ )                                     | $-20$ mA $+20$ mA $-0.5$ V to to VCC $+~0.5$ V $\pm50$ mA |
| DC V <sub>CC</sub> or Ground Current<br>per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )<br>Storage Temperature (T <sub>STG</sub> )<br>Junction Temperature (T <sub>J</sub> )<br>CDIP<br>PDIP | ±50 mA<br>-65°C to +150°C<br>175°C<br>140°C               |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating

| Supply Voltage (V <sub>CC</sub> )  'AC 'ACT   | 2.0V to 6.0V<br>4.5V to 5.5V  |
|---|---|
| Input Voltage (V <sub>I</sub> )   | 0V to V <sub>CC</sub>   |
| Output Voltage (V <sub>O</sub> )  | 0V to V <sub>CC</sub>   |
| Operating Temperature (T <sub>A</sub> ) 74AC/ACT 54AC/ACT   | -40°C to +85°C<br>-55°C to +125°C                                   |
| Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V | Z <sub>a</sub> = D <sub>a</sub> * (lo <sub>a</sub> * S <sub>b</sub> |
| Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V <sub>IN</sub> from 0.8V to 2.0V V <sub>CC</sub> @ 4.5V, 5.5V                       |   |
|   |   |

#### DC Characteristics for 'AC Family Devices

|                 |                                      | Auto-             | 74                      | AC                              | 54AC                 | 74AC                 |    |  |
|-----------------|--------------------------------------|-------------------|-------------------------|---------------------------------|----------------------|----------------------|----|--|
| Symbol          | Parameter                            |                   |                         | T <sub>A</sub> = -40°C to +85°C | Units                | Conditions           |    |  |
|                 | plane.                               | -                 | Typ Guarant             |                                 | Guaranteed Li        | mits                 |    |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85             | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85  | V  | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65             | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65  | v  | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4               | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4    | V  | $I_{OUT} = -50 \mu A$  |
|                 | 1050 IX                              | 3.0<br>4.5<br>5.5 |                         | 2.56<br>3.86<br>4.86            | 2.4<br>3.7<br>4.7    | 2.46<br>3.76<br>4.76 | V  | $^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $I_{OH} -24 \text{ mA}$ $-24 \text{ mA}$ |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1               | 0.1<br>0.1<br>0.1    | 0.1<br>0.1           | V  | Ι <sub>ΟυΤ</sub> = 50 μΑ   |
|                 |                                      | 3.0<br>4.5<br>5.5 |                         | 0.36<br>0.36<br>0.36            | 0.50<br>0.50<br>0.50 | 0.44<br>0.44<br>0.44 | v  | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>12 mA<br>I <sub>OL</sub> 24 mA<br>24 mA   |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5               |                         | ±0.1                            | ±1.0                 | ±1.0                 | μΑ | $V_I = V_{CC}$ , GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  | 4d de = 70                          |     | Тур   | 10   | Guaranteed |             |    |  |
|------------------|-------------------------------------|-----|-------|------|------------|-------------|----|--|
| I <sub>OLD</sub> | †Minimum Dynamic                    | 5.5 | O. b. | 110W | 50         | 75          | mA | V <sub>OLD</sub> = 1.65V Max             |
| IOHD             | Output Current                      | 5.5 | do i  | 0.1  | 0.11-50    | 0.5 −75 o a | mA | V <sub>OHD</sub> = 3.85V Min             |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5 | 13    | 8.0  | 160.0      | 80.0        | μΑ | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{|N}$  and  $I_{|CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{|CC|}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

## DC Characteristics for 'ACT Family Devices

| 7,60            | 1.6 10.6                               |                        | 744                     | СТ           | 54ACT                            | 74ACT                           |               | 42 of 41  |
|-----------------|--|------------------------|-------------------------|--------------|----------------------------------|---------------------------------|---------------|---|
| Symbol          | Parameter 2.1                          | V <sub>CC</sub><br>(V) | T <sub>A</sub> = + 25°C |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units         | Conditions  |
|                 |  |                        | Тур                     |              | Guaranteed L                     | imits                           | 46.05 A6      | Voltage Flange 3.0 is 5   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage    | 4.5<br>5.5             | 1.5<br>1.5              | 2.0<br>2.0   | See Se 0.2 2 for W               | 2.0<br>2.0                      | V             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage        | 4.5<br>5.5             | 1.5                     | 0.8          | 0.8<br>0.8                       | 0.8                             | ٧             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49            | 4.4<br>5.4   | 4.4 00 = 10<br>5.4               | 4.4<br>5.4                      | V             | $I_{OUT} = -50 \mu\text{A}$   |
| 2-3,4           | ### #### #### ######################## | 4.5<br>5.5             | 0.8)                    | 3.86<br>4.86 | 3.70 O.V<br>4.70                 | 3.76<br>4.76                    | on Delay      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ m/s}$ $-24 \text{ m/s}$  |
| Vols            | Maximum Low Level Output Voltage       | 4.5<br>5.5             | 0.001                   | 0.1          | 0.1 0.7<br>0.1                   | 0.8 0.1 o.a<br>0.1              | on Delay<br>V | $I_{OUT} = 50 \mu\text{A}$  |
|                 | en 3.51 0.5                            | 4.5<br>5.5             | 8.67<br>Err             | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44                            | on Delay      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| IIN<br>4,8,9    | Maximum Input<br>Leakage Current       | 5.5                    | 1.2.1                   | ±0.1         | ±1.0                             | ±1.0                            | μА            | V <sub>I</sub> = V <sub>CC</sub> , GND  |
| ICCT<br>4,8-S   | Maximum I <sub>CC</sub> /Input         | 5.5                    | 0.6                     | 0.1          | 1.6                              | 1.5<br>0.s                      | mA            | $V_{\rm I} = V_{\rm CC} - 2.1V$   |
| IOLD            | †Minimum Dynamic                       | 5.5                    |                         |              | 50                               | 75                              | mA            | V <sub>OLD</sub> = 1.65V Max  |
| lohd            | Output Current                         | 5.5                    |                         |              | -50                              | -75                             | mA            | V <sub>OHD</sub> = 3.85V Mir  |
| lcc             | Maximum Quiescent Supply Current       | 5.5                    | 0                       | 8.0          | 160.0                            | 80.0                            | μΑ            | $V_{IN} = V_{CC}$ or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics: See Section 2 for Waveforms | OA not applied a page 1000

|                  |   | 0)                | 76.  | 74AC       | SAAI         | 54   | AC           | 74   | AC           |       |       |
|------------------|---|-------------------|--|------------|--------------|--|--------------|--|--------------|-------|-------|
| Symbol           | Parameter   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |              | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |              | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |              | Units | Fig.  |
|                  |   | -                 | Min  | Тур        | Max          | Min  | Max          | Min  | Max          |       |       |
| t <sub>PLH</sub> | Propagation Delay<br>S <sub>n</sub> to Z <sub>n</sub> | 3.3<br>5.0        | 2.5<br>2.0                                       | 9.5<br>6.5 | 15.0<br>11.0 | 1.0  | 19.5<br>14.0 | 2.5  | 17.5<br>12.5 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay<br>S <sub>n</sub> to Z <sub>n</sub> | 3.3<br>5.0        | 3.0<br>2.5                                       | 8.5<br>6.5 | 14.5<br>11.0 | 1.0  | 18.0<br>13.5 | 2.5  | 16.5<br>12.0 | ns    | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay<br>E to Z <sub>n</sub>              | 3.3<br>5.0        | 2.5<br>1.5                                       | 8.0<br>5.5 | 13.5<br>9.5  | 1.0<br>1.0   | 16.5<br>12.5 | 2.0<br>1.5   | 16.0<br>11.0 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay<br>E to Z <sub>n</sub>              | 3.3<br>5.0        | 2.5<br>2.0                                       | 7.0<br>5.0 | 11.0<br>8.0  | 1.0<br>1.0   | 14.0<br>10.0 | 2.0<br>1.5   | 12.5<br>9.0  | ns    | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay                                     | 3.3<br>5.0        | 2.5  | 7.5<br>5.5 | 12.5<br>9.0  | 1.0<br>1.0   | 16.0<br>11.5 | 2.0  | 14.5<br>10.5 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay                                     | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.0 | 11.5<br>8.5  | 1.0  | 14.5<br>10.5 | 1.5<br>1.5   | 13.0<br>10.0 | ns    | 2-3,4 |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for Waveforms

| No. of the state o | 1000  |   | 360  |           | V/3 V/3 V/0 V/0 V  |  |  |  | MARRIED V. BURZER                                      |  |
|--|---|---|--|-----------|--|--|--|--|--|--|
| = TUOV   | 8.4   |   | 74ACT  |           | 8 54   | ACT  | 74/  | ACT  | Max  | JIV  |
| Parameter  | V <sub>CC</sub> *   |   | -  |           | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |  | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |  | Units  | Fig.<br>No.  |
|  |   | Min   | Тур  | Max       | Min  | Max  | Min  | Max  | 0.00   |  |
| Propagation Delay S <sub>n</sub> to Z <sub>n</sub>   | 5.0   | 3.0   | 7.0 0.7  | 11.5      | 1.0  | 15.0   | 2.0  | 13.5   | ns   | 2-3,4  |
| Propagation Delay S <sub>n</sub> to Z <sub>n</sub>   | 5.0   | 3.0   | 7.0  | 11.5      | 1.0  | 14.5   | 2.5  | 13.5   | ns   | 2-3,4  |
| Propagation Delay $\overline{E}_n$ to $Z_n$  | 5.0   | 2.0   | 6.5  | 10.5      | 1.0  | 13.5   | 2.0  | 12.5   | ns   | 2-3,4  |
| Propagation Delay $\overline{E}_n$ to $Z_n$  | 5.0   | 3.0   | 6.0  | 9.5       | 1.0  | 11.5   | 2.5  | 11.0   | ns   | 2-3,4  |
| Propagation Delay  | 5.0   | 2.5   | 5.5  | 9.5       | 1.0  | 12.5   | 2.0  | 11.0   | ns   | 2-3,4  |
| Propagation Delay  | 5.0   | 2.0   | 5.5  | 9.5       | 1.0  | 12.0   | 2.0  | 11.0   | ns   | 2-3,4  |
|  | Propagation Delay S <sub>n</sub> to Z <sub>n</sub> Propagation Delay S <sub>n</sub> to Z <sub>n</sub> Propagation Delay E <sub>n</sub> to Z <sub>n</sub> Propagation Delay E <sub>n</sub> to Z <sub>n</sub> Propagation Delay I <sub>n</sub> to Z <sub>n</sub> Propagation Delay I <sub>n</sub> to Z <sub>n</sub> | Parameter  Vcc* (V)  Propagation Delay Sn to Zn  Propagation Delay En to Zn  Propagation Delay In to Zn | Parameter  Vcc* (V)  Min  Propagation Delay Sn to Zn  Propagation Delay En to Zn  Propagation Delay In to Zn | Parameter | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$         | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$       | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ |

\*Voltage Range 5.0 is 5.0V ±0.5V

### Capacitance

| Symbol          | Parameter                        | Тур  | Units       | Conditions             |
|-----------------|----------------------------------|------|-------------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF property | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 65.0 | pF          | V <sub>CC</sub> = 5.0V |



## 54AC/74AC157 • 54ACT/74ACT157 **Quad 2-Input Multiplexer**

#### **General Description**

The 'AC/'ACT157 is a high-speed guad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'AC/'ACT157 can also be used as a function generator.

#### **Features**

- Outputs source/sink 24 mA
- 'ACT157 has TTL-compatible inputs
- Standard Military Drawing (SMD) - 'AC157: 5962-89539
  - 'ACT157: 5962-89688 AA and to eau nominoo A

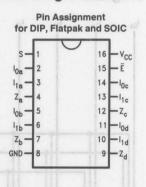
#### Ordering Code: See Section 8

#### **Logic Symbols**

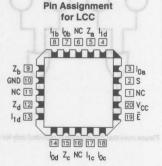
# TL/F/9929-1 IEEE/IEC G1 ОЬ 116 l<sub>1d</sub>

| Pin Names                        | Description          |
|----------------------------------|----------------------|
| I <sub>0a</sub> -I <sub>0d</sub> | Source 0 Data Inputs |
| I <sub>1a</sub> -I <sub>1d</sub> | Source 1 Data Inputs |
| Ē                                | Enable Input         |
| S                                | Select Input         |
| Za-Zd                            | Outputs              |

#### Connection Diagrams



TL/F/9929-3



TL/F/9929-4

TL/F/9929-2

#### **Functional Description**

The 'AC/'ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\overline{\rm E}$ ) is active-LOW. When  $\overline{\rm E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'AC/'ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$

$$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the 'AC/ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is

as a function generator. The 'AC/'ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

#### **Truth Table**

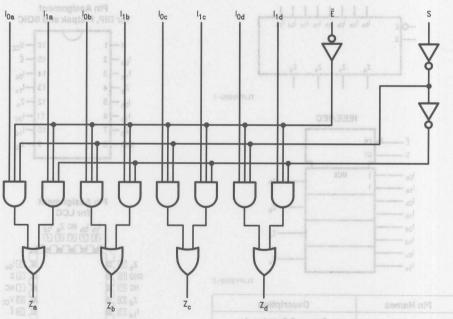
|             | Inputs     |           |              |              |  |  |  |  |  |  |
|-------------|------------|-----------|--------------|--------------|--|--|--|--|--|--|
| Ē           | S          | lo        | nadri i      | nameZn       |  |  |  |  |  |  |
| HEATH SALES | X          | X         | X            | TI-L'AC/A    |  |  |  |  |  |  |
| etchies     | d mH as    | X         | most Litab i | Folir bits o |  |  |  |  |  |  |
| ne fdur t   | inpHts. T  | Ide X ba  | n SiHect :   | the commo    |  |  |  |  |  |  |
| bettevnin   | on) Luti e |           | bottxlea     | prosent the  |  |  |  |  |  |  |
| neg Frolis  | not aga ba | eu eqpets | OTIX car     | A'\OA' HIT   |  |  |  |  |  |  |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

#### Logic Diagram



TL/F/9929-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Recommended Operating Absolute Maximum Rating (Note 1) If Military/Aerospace specified devices are required, Conditions please contact the National Semiconductor Sales Supply Voltage (V<sub>CC</sub>) Office/Distributors for availability and specifications. 'AC 2.0V to 6.0V -0.5V to +7.0V Supply Voltage (V<sub>CC</sub>) 'ACT 4.5V to 5.5V DC Input Diode Current (I<sub>IK</sub>) OV to Vcc Input Voltage (V<sub>I</sub>) $V_1 = -0.5V$ -20 mA Output Voltage (Vo) +20 mA $V_I = V_{CC} + 0.5V$ Operating Temperature (T<sub>A</sub>) -0.5V to V<sub>CC</sub> + 0.5V DC Input Voltage (VI) -40°C to +85°C 74AC/ACT DC Output Diode Current (IOK) 1necseiu0 m-55°C to +125°C 54AC/ACT -20 mA $V_0 = -0.5V$ Minimum Input Edge Rate (ΔV/Δt) +20 mA $V_O = V_{CC} + 0.5V$ 'AC Devices V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> DC Output Voltage (VO) -0.5V to to $V_{CC} + 0.5$ V V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V DC Output Source or Sink Current (IO) ±50 mA Minimum Input Edge Rate (ΔV/Δt) DC V<sub>CC</sub> or Ground Current 'ACT Devices V<sub>IN</sub> from 0.8V to 2.0V per Output Pin (ICC or IGND) ±50 mA V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns -65°C to +150°C Storage Temperature (TSTG) Junction Temperature (T<sub>J</sub>) 175°C PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### **DC Characteristics for 'AC Family Devices**

| V1.02           | 3.14.10                          | 9,1                 |                  |        | 0.0        |                  | 427V    | 9.0                         | 1         | - difform    | A SEATTH I                            |
|-----------------|----------------------------------|---------------------|------------------|--------|------------|------------------|---------|-----------------------------|-----------|--------------|---------------------------------------|
| 50 pA           | - = 1001 V                       | 4.5                 | 74               | AC     | 4.4        | 54AC             | 4,4     | 74AC                        | lev       | n Higir Le   | North Minimun                         |
| Symbol          | Parameter                        | V <sub>CC</sub> (V) | T <sub>A</sub> = | + 25°C | +.8<br>-55 | T <sub>A</sub> = |         | T <sub>A</sub> = -40°C to + | 85°C      | Units        | Conditions                            |
| - 24 mA         |                                  | .76                 | Тур              |        |            | Guara            | nteed L | imits 8.4                   |           |              |                                       |
| VIH             | Minimum High Level               | 3.0                 | 1.5              | 2.1    | 4.70       | 2.1              | 4,85    | 2.1                         |           |              | $V_{OUT} = 0.1V$                      |
| Au C            | Input Voltage                    | 4.5                 | 2.25             | 3.15   | 1.0        | 3.15             |         | 100.0 3.15                  |           | LVVJm        | or V <sub>CC</sub> - 0.1V             |
|                 |                                  | 5.5                 | 2.75             | 3.85   | 1.0        | 3.85             | 1.0     | 100.0 3.85                  |           | (oltage      | / fueluO                              |
| VILIV TO J      | Maximum Low Level                | 3.0                 | 1.5              | 0.9    |            | 0.9              |         | 0.9                         |           |              | $V_{OUT} = 0.1V$                      |
| 24 mA           | Input Voltage                    | 4.5                 | 2.25             | 1.35   | 0.50       | 1.35             |         | 1.35                        |           | V            | or V <sub>CC</sub> - 0.1V             |
| Am AS           | 101                              | 5.5                 | 2.75             | 1.65   | 0.50       | 1.65             |         | 1.65                        |           |              |                                       |
| V <sub>OH</sub> | Minimum High Level               | 3.0                 | 2.99             | 2.9    | ±1.0       | 2.9              | 1.01    | 2.9                         |           | Jugal at     | $I_{OUT} = -50 \mu A$                 |
|                 | Output Voltage                   | 4.5                 | 4.49             | 4.4    | 0.12       | 4.4              |         | 4.4                         |           | tne VIO      |                                       |
| VI.S -          | opV = IV                         | 5.5                 | 5.49             | 5.4    |            | 5.4              |         | 5.4                         |           | FE           | umixeM                                |
|                 | Am Am                            | C.                  |                  |        | 0.1        |                  |         | 9,0 6.0                     | 1         | h            | *VIN = VIL or VII                     |
| xsM Vaa.        | = ouoV Am                        | 3.0                 |                  | 2.56   | 08         | 2.4              |         | 2.46                        |           | m Dynan      |                                       |
|                 |                                  | 4.5                 |                  | 3.86   | 0.0        | 3.7              |         | 3.76                        |           |              | IOH -24 m/                            |
| niM Vas.        | = gHoV Am                        | 5.5                 |                  | 4.86   | 00-        | 4.7              |         | 4.76                        | 1         |              | -24 m/                                |
| V <sub>OL</sub> | Maximum Low Level                | 3.0                 | 0.002            | 0.1    | 160.0      | 0.1              |         | 0.1.2                       |           | n Quiesc     | $I_{OUT} = 50 \mu\text{A}$            |
|                 | Output Voltage                   | 4.5                 | 0.001            | 0.1    |            | 0.1              |         | 0.1                         |           | V            |                                       |
|                 |                                  | 5.5                 | 0.001            | 0.1    |            | 0.1              |         | 0.1                         |           | resholds or  |                                       |
|                 |                                  |                     |                  |        |            |                  |         | ent e is beboot a           | ine outpi | ) um 0.8 n   | $*V_{IN} = V_{IL} \text{ or } V_{II}$ |
|                 |                                  | 3.0                 |                  | 0.36   |            | 0.50             |         | 0.44                        |           | 1 25°C is is | 12 m                                  |
|                 |                                  | 4.5                 |                  | 0.36   |            | 0.50             |         | 0.44                        |           | V            | I <sub>OL</sub> 24 m/                 |
|                 |                                  | 5.5                 |                  | 0.36   |            | 0.50             |         | 0.44                        |           |              | 24 m/                                 |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current | 5.5                 |                  | ±0.1   |            | ±1.0             |         | ±1.0                        |           | μА           | $V_{I} = V_{CC}$ , GND                |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) This is murning the state of the continued of the cont

|          | OS Parameter                        |                        | 74                 | 74AC 54AC 74AC |  | 74AC         | ice spei    | H Military/Aerosp |  |  |
|----------|-------------------------------------|------------------------|--------------------|----------------|--|--------------|-------------|-------------------|--|--|
| Symbol V |                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> + 2 |                | T <sub>A</sub> = T <sub>A</sub> =<br>-55°C to + 125°C -40°C to +85°C |              |             | Units             | Conditions                               |  |
|          |                                     |                        | Тур                | Voltag         | hight  | Guaranteed I | Limits      | (Spi) Iner        | DC Input Diode Cur                       |  |
| IOLD     | †Minimum Dynamic                    | 5.5                    | oV) agi            | HoV I          | Outp   | 50           | 75          | mA                | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD     | Output Current                      | 5.5                    | Empera             | l geite        | Open   | -50 0 0 0    | V of V8.⊕75 | mA                | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc      | Maximum Quiescent<br>Supply Current | 5.5                    | T<br>out Eda       | 8.0            | Sal<br>Minin   | 160.0        | 80.0        | μA                | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

### DC Characteristics for 'ACT Family Devices

|                                   |                                      |                        | 74A             | CT                         |                     | 54ACT                   |                                   | 74ACT                         |                               | AT) an                  |   |
|-----------------------------------|--------------------------------------|------------------------|-----------------|----------------------------|---------------------|-------------------------|-----------------------------------|-------------------------------|-------------------------------|-------------------------|---|
| Symbol                            | Parameter                            | V <sub>CC</sub><br>(V) |                 | T <sub>A</sub> =<br>+ 25°C |                     | T <sub>A</sub> = C to + |                                   | T <sub>A</sub> = -40°C to +85 | 5°C                           | Units                   | Conditions  |
|                                   |                                      |                        | Тур             |                            |                     | Guarar                  | teed L                            | imits                         | te sices                      | epoilus mu<br>The datab | Mote 1: Absolubs madm<br>to the device may occur.                                     |
| V <sub>IH</sub>                   | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5      | 2.0<br>2.0                 |                     | 2.0                     | cower eu<br>is not rei<br>itions. | 2.0<br>2.0                    | ni desi<br>ding ve<br>stoutsi | Meta sch                | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub>                   | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5      | 0.8                        | ces                 | 0.8                     |                                   | 0.8                           | 80                            | V                       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub>                   | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49    | 4.4<br>5.4                 | SGAC<br>TA =        | 4.4<br>5.4              | 3/                                | 4.4<br>5.4                    |                               | ٧                       | $I_{OUT} = -50 \mu\text{A}$   |
| anoun                             | anou on                              | 4.5<br>5.5             | o*0* -<br>atins | 3.86<br>4.86               | C to +              | 3.70<br>4.70            | 200                               | 3.76<br>4.76                  | loc                           | ٧                       | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$              |
| V <sub>OL</sub> TO -              | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001  | 0.1                        | 3.15                | 0.1                     | 3,15                              | 0.1a a                        |                               | Vage                    | $I_{OUT} = 50 \mu A$  |
|                                   | = TUOV<br>00V 10 V                   | 4.5<br>5.5             |                 | 0.36<br>0.36               | 0.0<br>1.35<br>1.65 | 0.50<br>0.50            | 8.0<br>1.35                       | 0.44                          | levi                          | Low Le                  | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{IOL}$ $^{24 \text{ mA}}$ $^{24 \text{ mA}}$ |
| I <sub>IN</sub> <sub>4</sub> oa – | Maximum Input<br>Leakage Current     | 5.5                    |                 | ±0.1                       | 2.9                 | ±1.0                    | 2.8                               | 09.5 ± 1.0 0                  | isk                           | μΑ                      | V <sub>I</sub> = V <sub>CC</sub> , GND  |
| ICCT                              | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6             |                            | 5,4                 | 1.6                     | 5.4                               | 94.8 8.8                      |                               | mA                      | $V_I = V_{CC} - 2.1V$   |
| IOLD                              | †Minimum Dynamic                     | 5.5                    |                 | 41.                        | 2,4                 | 50                      | 88.8                              | 75                            |                               | mA                      | V <sub>OLD</sub> = 1.65V Max  |
| I <sub>OHD</sub>                  | Output Current                       | 5.5                    |                 |                            | 3.7                 | -50                     | 2.60                              | -75                           |                               | mA                      | V <sub>OHD</sub> = 3.85V Min  |
| Icc <sub>AA</sub> 08              | Maximum Quiescent<br>Supply Current  | 5.5                    |                 | 8.0                        | 0.1                 | 160.0                   | 0.1                               | 80.0                          | leive                         | μΑ                      | V <sub>IN</sub> = V <sub>CC</sub> or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{|N}$  and  $I_{|CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{|CC}$ .  $I_{|CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for waveforms.

|                  |  |                   | 74AC  T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF |            |             | 54AC  T <sub>A</sub> = -55°C  to +125°C  C <sub>L</sub> = 50 pF |                       | 74AC  T <sub>A</sub> = -40°C  to +85°C  C <sub>L</sub> = 50 pF |              | Units |        |
|------------------|--|-------------------|---|------------|-------------|---|-----------------------|--|--------------|-------|--------|
| Symbol Parameter | Parameter                                | V <sub>CC</sub> * |   |            |             |   |                       |  |              |       | Fig.   |
|                  |  |                   | Min   | Тур        | Max         | Min   | Max                   | Min  | Max          | L¢ h  | au O   |
| t <sub>PLH</sub> | Propagation Delay<br>S to Z <sub>n</sub> | 3.3<br>5.0        | 1.5<br>1.5  | 7.0<br>5.5 | 11.5<br>9.0 | 1.0<br>1.0  | 16.0<br>12.0          | 1.5<br>1.5   | 13.0<br>10.0 | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>S to Z <sub>n</sub> | 3.3<br>5.0        | 1.5   | 6.5<br>5.0 | 11.0<br>8.5 | 1.0   | 14.0<br>11.5          | 1.5<br>1.0   | 12.0<br>9.5  | ns    | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay<br>E to Z <sub>n</sub> | 5.0               | 1.5   | 7.0<br>5.5 | 9.0         | 1.0<br>1.0  | 16.0<br>12.0          | 1.5  | 13.0<br>10.0 | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay                        | 3.3<br>5.0        | 1.5<br>1.5  | 6.5<br>5.5 | 11.0<br>9.0 | 1.0<br>1.0  | 14.0<br>11.5          | 1.5<br>1.0   | 12.0<br>9.5  | ns    | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay                        | 3.3<br>5.0        | 1.5<br>1.5  | 5.0<br>4.0 | 8.5<br>6.5  | 1.0<br>1.0  | 11.0 <sup>8</sup> 9.0 | 1.0<br>1.0   | 9.0<br>7.0   | ns    | 2-3, 4 |
| tpHL             | Propagation Delay                        | 3.3<br>5.0        | 1.5<br>1.5  | 5.0<br>4.0 | 8.0<br>6.5  | 1.0<br>1.0  | 11.0<br>9.0           | 1.0<br>1.0   | 9.0<br>7.0   | ns    | 2-3, 4 |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for waveforms.

|                  | 400000                                   | 9                 |  | 74ACT | B)   | 54A0   | CT   | 74   | ACT  | 181 92 |             |
|------------------|--|-------------------|--|-------|------|--|------|--|------|--------|-------------|
| Symbol           | Parameter                                | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units  | Fig.<br>No. |
|                  |  | E EL              | Min  | Тур   | Max  | Min  | Max  | Min  | Max  | TY     |             |
| t <sub>PLH</sub> | Propagation Delay<br>S to Z <sub>n</sub> | 5.0               | 2.0  | 5.5   | 9.0  | 1.0  | 11.5 | 1.5  | 10.0 | ns     | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>S to Z <sub>n</sub> | 5.0               | 2.0  | 5.5   | 9.5  | 1.0  | 11.5 | 2.0  | 10.5 | ns     | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay<br>E to Z <sub>n</sub> | 5.0               | 1.5  | 6.0   | 10.0 | 1.0  | 12.0 | 1.5  | 11.5 | ns     | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>E to Z <sub>n</sub> | 5.0               | 1.5  | 5.0   | 8.5  | 1.0  | 10.0 | 1.0  | 9.0  | ns     | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay                        | 5.0               | 1.5  | 4.0   | 7.0  | 1.0  | 8.5  | 1.0  | 8.5  | ns     | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay                        | 5.0               | 1.5  | 4.5   | 7.5  | 1.0  | 9.0  | 1.0  | 8.5  | ns     | 2-3, 4      |

\*Voltage Range 5.0 is 5.0V  $\pm$  0.5V

#### Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 50.0 | pF    | V <sub>CC</sub> = 5.0V |



# 54AC/74AC158 • 54ACT/74ACT158 Quad 2-Input Multiplexer

#### **General Description**

The 'AC/'ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'AC/'ACT158 can also be used as a function generator.

#### **Features**

- Outputs source/sink 24 mA
- 'ACT158 has TTL-compatible inputs

AC Electrical Characteristics: See Section 2 for waveforms

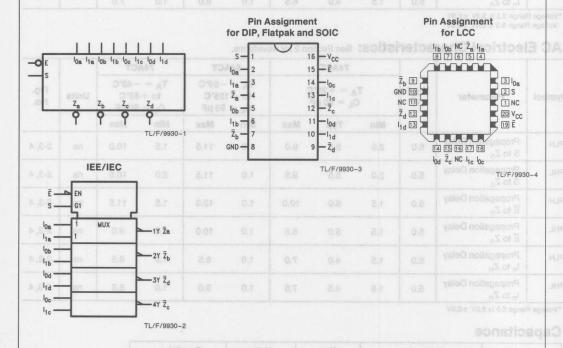
lodmy2

- Standard Military Drawing (SMD)
- 'AC158: 5962-89729
  - 'ACT158: 5962-88755

Ordering Code: See Section 8

**Logic Symbols** 

#### **Connection Diagrams**



| Pin Names                         | Description          |  |  |  |  |  |
|-----------------------------------|----------------------|--|--|--|--|--|
| I <sub>0a</sub> -I <sub>0d</sub>  | Source 0 Data Inputs |  |  |  |  |  |
| I <sub>1a</sub> -I <sub>1d</sub>  | Source 1 Data Inputs |  |  |  |  |  |
| Ē                                 | Enable Input         |  |  |  |  |  |
| S                                 | Select Input         |  |  |  |  |  |
| $\overline{Z}_a - \overline{Z}_d$ | Inverted Outputs     |  |  |  |  |  |

#### Functional Description

The 'AC/'ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ( $\overline{E}$ ) is active-LOW. When  $\overline{E}$  is HIGH, all of the outputs ( $\overline{Z}$ ) are forced HIGH regardless of all other inputs. The 'AC/'ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the 'AC/'ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

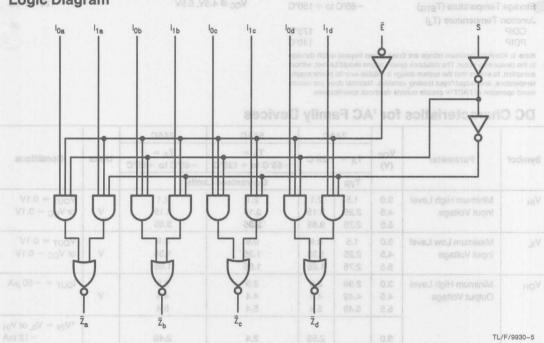
#### Truth Table in a mumix of studed A

| nequired, | Inputs    |                |                 |                             |  |  |  |  |  |
|-----------|-----------|----------------|-----------------|-----------------------------|--|--|--|--|--|
| .a Entha  | S         | I <sub>0</sub> | ilitive 141 are | ituditate <b>Z</b> \soltifC |  |  |  |  |  |
| VO.TH- OF | /a.o.x    | Χ              | X (00           | A) ebsyl.H, Alddng          |  |  |  |  |  |
| L         | L         | L              | (Sel) Xemu      | OC Input Digde C            |  |  |  |  |  |
| Am 92-    | L         | Н              | X               | A9'0 E = IA                 |  |  |  |  |  |
| Am QE+    | Н         | X              | L               | 10 + 00H = 14               |  |  |  |  |  |
| ASTOF+ OS | V of Halo | X              | H (V)           | OC input Voltage            |  |  |  |  |  |

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

|  | 7.5 | 88.k |  |  |
|--|-----|------|--|--|
|  |     |      |  |  |
|  |     |      |  |  |
|  |     |      |  |  |

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V<sub>CC</sub>) -0.5V to +7.0V DC Input Diode Current (I<sub>IK</sub>)

 $V_{I} = -0.5V$  -20 mA $V_{I} = V_{CC} + 0.5V$  +20 mA

DC Input Voltage ( $V_{\rm I}$ )  $-0.5{\rm V}$  to  $V_{\rm CC}+0.5{\rm V}$  DC Output Diode Current ( $I_{\rm OK}$ )

 $V_O = -0.5V$   $V_O = V_{CC} + 0.5V$  -0.5V to to  $V_{CC} + 0.5V$  -0.5V to to  $V_{CC} + 0.5V$ 

DC Output Voltage (V<sub>O</sub>) -0.5V to to V<sub>CC</sub> + 0.5V
DC Output Source
or Sink Current (I<sub>O</sub>) ±50 mA

DC V<sub>CC</sub> or Ground Current
per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±50 mA

Storage Temperature (T<sub>STG</sub>) -65°C to +150°C

Junction Temperature (T<sub>J</sub>)

CDIP 175°C 140°C 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating moltons Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 'AC
 2.0V to 6.0V

 'ACT
 4.5V to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

 Output Voltage (V<sub>O</sub>)
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 -40°C to +85°C

 54AC/ACT
 -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)
'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

#### **DC Characteristics for 'AC Family Devices**

|                  | - 6                              | L               | 74                     | AC   | 54AC                             | 74AC                            |        | many later to the           |  |
|------------------|----------------------------------|-----------------|------------------------|------|----------------------------------|---------------------------------|--------|-----------------------------|--|
| Symbol Parameter | Parameter                        | V <sub>CC</sub> | T <sub>A</sub> = +25°C |      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units  | Conditions                  |  |
|                  | have middle to a set of          | 10/10/10/10/10  | Тур                    | T    | Guaranteed Limits                |                                 |        |                             |  |
| VIH              | Minimum High Level               | 3.0             | 1.5                    | 2.1  | 2.1                              | 2.1                             | Lyppia | V <sub>OUT</sub> = 0.1V     |  |
|                  | Input Voltage                    | 4.5             | 2.25                   | 3.15 | 3.15                             | 3.15                            | V      | or V <sub>CC</sub> - 0.1V   |  |
|                  |                                  | 5.5             | 2.75                   | 3.85 | 3.85                             | 3.85                            |        | T                           |  |
| VIL              | Maximum Low Level                | 3.0             | 1.5                    | 0.9  | 0.9                              | 0.9                             | -      | V <sub>OUT</sub> = 0.1V     |  |
|                  | Input Voltage                    | 4.5             | 2.25                   | 1.35 | 1.35                             | 1.35                            | V      | or V <sub>CC</sub> - 0.1V   |  |
|                  |                                  | 5.5             | 2.75                   | 1.65 | 1.65                             | 1.65                            |        |                             |  |
| V <sub>OH</sub>  | Minimum High Level               | 3.0             | 2.99                   | 2.9  | 2.9                              | 2.9                             | 1      | $I_{OUT} = -50 \mu\text{A}$ |  |
|                  | Output Voltage                   | 4.5             | 4.49                   | 4.4  | 4.4                              | 4.4                             | V      |                             |  |
|                  |                                  | 5.5             | 5.49                   | 5.4  | 5.4                              | 5.4                             |        |                             |  |
|                  |                                  |                 |                        | 1/2  | #2                               | I I                             |        | *VIN = VIL or VIH           |  |
|                  | TT .                             | 3.0             |                        | 2.56 | 2.4                              | 2.46                            |        | -12 mA                      |  |
|                  | astimate propagation dataya:     | 4.5             | ton bkjoda             | 3.86 | 3.7                              | 3.76                            | V      | lOH −24 mA                  |  |
|                  |                                  | 5.5             |                        | 4.86 | 4.7                              | 4.76                            |        | -24 mA                      |  |
| VOL              | Maximum Low Level                | 3.0             | 0.002                  | 0.1  | 0.1                              | 0.1                             |        | $I_{OUT} = 50 \mu A$        |  |
|                  | Output Voltage                   | 4.5             | 0.001                  | 0.1  | 0.1                              | 0.1                             | V      |                             |  |
|                  |                                  | 5.5             | 0.001                  | 0.1  | 0.1                              | 0.1                             |        |                             |  |
|                  |                                  |                 |                        |      |                                  |                                 |        | *VIN = VIL or VIH           |  |
|                  |                                  | 3.0             |                        | 0.36 | 0.50                             | 0.44                            |        | 12 mA                       |  |
|                  |                                  | 4.5             |                        | 0.36 | 0.50                             | 0.44                            | V      | I <sub>OL</sub> 24 mA       |  |
|                  |                                  | 5.5             |                        | 0.36 | 0.50                             | 0.44                            |        | 24 mA                       |  |
| IIN              | Maximum Input<br>Leakage Current | 5.5             |                        | ±0.1 | ±1.0                             | ±1.0                            | μА     | $V_{I} = V_{CC}$ , GND      |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## 

|        | ZAAC                                |                        | 74AC             |        | 54AC                             | 74AC                            |       |                              |  |
|--------|-------------------------------------|------------------------|------------------|--------|----------------------------------|---------------------------------|-------|------------------------------|--|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                   |  |
| 50 pF  | CL = 50 pF                          |                        | Тур              | 10     | Guaranteed L                     | imits                           |       |                              |  |
| IOLD   | †Minimum Dynamic                    | 5.5                    | XBM2             | THEFT  | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max |  |
| IOHD   | Output Current                      | 5.5                    | 0.7.1            | 0.1    | 0.6 -50 8.8                      | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min |  |
| lcc    | Maximum Quiescent<br>Supply Current | 5.5                    |                  | 8.0    | 160.00                           | 80.08                           | μА    | $V_{IN} = V_{CC}$ or GND     |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time. Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5,5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### **DC Characteristics for 'ACT Family Devices**

|                  | 6.7 0.                               |                        | 74A                    | СТ           | 54ACT                            | 74ACT                           |                     | 0/2 OJ UJ   |  |
|------------------|--------------------------------------|------------------------|------------------------|--------------|----------------------------------|---------------------------------|---------------------|---|--|
| Symbol           | Parameter 0.                         | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | ASTON AS            | Conditions  |  |
|                  |                                      |                        | Тур                    |              | Guaranteed L                     | imits                           | /8.0± Vo.           |   |  |
| V <sub>IH</sub>  | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5             | 2.0          | 2.0                              | 2.0                             | riv la              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                  |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5             | 0.8          | 0.8<br>0.8                       | 0.8<br>0.8                      | ٧                   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                  |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4   | 4.4 8 = 5.4                      | 4.4<br>5.4                      | V                   | $I_{OUT} = -50 \mu\text{A}$   |  |
| 2-3, 4           | an 0.11 0                            | 4.5<br>5.5             | 12.0                   | 3.86<br>4.86 | 3.70 A<br>4.70                   | 3.76<br>4.76                    | sted not            | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |  |
| VOL              | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001                  | 0.1          | 0.9 0.1 a.a<br>0.1               | 0.10.8<br>0.1                   | V V                 | $I_{OUT} = 50 \mu A$  |  |
|                  | an 10.5 ns                           | 4.5                    | 11.0                   | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44                            | on V <sub>ela</sub> | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $24 \text{ m/s}$ $24 \text{ m/s}$ |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     | 5.5                    | 8.5                    | ±0.1         | ±1.0                             | ±1.0                            | μΑ                  | $V_I = V_{CC}$ , GND  |  |
| Ісст             | Maximum I <sub>CC</sub> /Input 3.7   | 5.5                    | 0.6                    | 1.0          | a.a 1.6 <sub>0.4</sub>           | a.r 1.5 <sub>0.8</sub>          | mA                  | $V_{\rm I} = V_{\rm CC} - 2.1 V$  |  |
| IOLD             | †Minimum Dynamic                     | 5.5                    |                        |              | 50                               | 75                              | mA                  | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub> | Output Current                       | 5.5                    | ELAIN                  |              | -50                              | -75                             | mA                  | V <sub>OHD</sub> = 3.85V Min  |  |
| lcc              | Maximum Quiescent<br>Supply Current  | 5.5                    | 50 [                   | 8.0          | 160.0                            | 80.0                            | μΑ                  | $V_{IN} = V_{CC}$ or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics: See Section 2 for waveforms.

|                  |  | DAG  | T.         | 74AC        |             | 54         | AC           | 74         | IAC          |    |        |
|------------------|--|--|------------|-------------|-------------|------------|--------------|------------|--------------|----|--------|
| Symbol           | Parameter  | $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Units      | Fig.<br>No. |             |            |              |            |              |    |        |
|                  |  |  | Min        | Тур         | Max         | Min        | Max          | Min        | Max          |    |        |
| t <sub>PLH</sub> | Propagation Delay S to $\overline{Z}_n$              | 3.3<br>5.0   | 1.5<br>1.5 | 7.0<br>5.5  | 11.5<br>9.0 | 1.0<br>1.0 | 14.0<br>11.0 | 1.5<br>1.0 | 12.5<br>9.5  | ns | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay S to $\overline{Z}_n$              | 3.3<br>5.0   | 1.5<br>1.5 | 7.0<br>5.5  | 11.5<br>9.0 | 1.0        | 14.0<br>11.0 | 1.5<br>1.5 | 12.5<br>10.0 | ns | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay<br>E to Z <sub>n</sub>             | 3.3<br>5.0   | 1.5<br>1.5 | 7.5<br>6.0  | 12.0<br>9.5 | 1.0<br>1.0 | 15.0<br>12.0 | 1.5<br>1.5 | 13.0<br>10.5 | ns | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay $\overline{E}$ to $\overline{Z}_n$ | 3.3<br>5.0   | 1.5<br>1.5 | 7.0<br>5.5  | 11.0<br>8.5 | 1.0<br>1.0 | 14.0<br>10.0 | 1.5        | 12.0<br>9.5  | ns | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay $I_n$ to $\overline{Z}_n$          | 3.3<br>5.0   | 1.5<br>1.5 | 5.5<br>4.0  | 9.0<br>7.0  | 1.0<br>1.0 | 11.0<br>8.5  | 1.5<br>1.0 | 10.0<br>7.5  | ns | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay $I_n$ to $\overline{Z}_n$          | 3.3<br>5.0   | 1.5<br>1.5 | 5.0<br>4.0  | 8.0<br>6.5  | 1.0        | 10.0<br>7.5  | 1.0<br>1.0 | 8.5<br>6.5   | ns | 2-3, 4 |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for waveforms.

| VE                                | = TUOV V   | 8.0               |     | 74ACT  |     | 54   | ACT                          | 74   | ACT    | nixal/i | υV     |
|-----------------------------------|--|-------------------|-----|--|-----|------|------------------------------|--|--------|---------|--------|
| Symbol                            | 1000   | V <sub>CC</sub> * |     | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |     | to + | - 55°C<br>- 125°C<br>= 50 pF | $T_A = -40$ °C<br>to $+85$ °C<br>$C_L = 50 \text{ pF}$ |        | Units   | Fig.   |
|                                   |  | ***               | Min | Тур  | Max | Min  | Max                          | Min  | Max    | populo  |        |
| t <sub>PLH</sub>                  | Propagation Delay S to $\overline{Z}_n$              | 5.0               | 2.5 | 6.0 07.8   | 9.5 | 1.0  | 12.0                         | 2.0  | 11.0   | ns      | 2-3, 4 |
| t <sub>PHL</sub> A <sub>M</sub> 0 | Propagation Delay S to $\overline{Z}_n$              | 5.0               | 1.5 | 5.5  | 9.0 | 1.0  | 1011.5                       | 1.5  | 10.0   | ns      | 2-3, 4 |
| tpLH<br>HIV 10 J                  | Propagation Delay $\overline{E}$ to $\overline{Z}_n$ | 5.0               | 1.5 | 5.5  | 9.5 | 1.0  | 11.0                         | 1.5  | 10.5   | ns      | 2-3, 4 |
| tPHLS                             | Propagation Delay $\overline{E}$ to $\overline{Z}_n$ | 5.0               | 1.5 | 5.5 08.0   | 9.5 | 1.0  | 11.0                         | 1.5  | 10.5   | ns      | 2-3, 4 |
| t <sub>PLH</sub>                  | Propagation Delay $I_n$ to $\overline{Z}_n$          | 5.0               | 1.5 | 4.5  | 8.0 | 1.0  | 9.5                          | 1.0  | 8.5    | ns      | 2-3, 4 |
| t <sub>PHL</sub>                  | Propagation Delay $I_n$ to $\overline{Z}_n$          | 5.0               | 1.5 | 4.0  | 6.5 | 1.0  | 8.0                          | 1.0  | 7.5149 | ns ns   | 2-3, 4 |

\*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol          | Parameter                        | Тур  | Units           | Conditions             |  |
|-----------------|----------------------------------|------|-----------------|------------------------|--|
| C <sub>IN</sub> | Input Capacitance                | 4.5  | Jaap Flore tugi | $V_{CC} = 5.0V$        |  |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 45.0 | pF              | V <sub>CC</sub> = 5.0V |  |



## 54AC/74AC161 • 54ACT/74ACT161 Synchronous Presettable Binary Counter

#### **General Description**

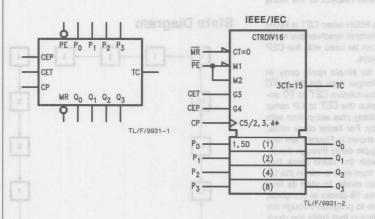
The 'AC/'ACT161 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW.

#### **Features**

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT161 has TTL-compatible inputs
- Standard Military Drawing (SMD)"AC161: 5962-89561

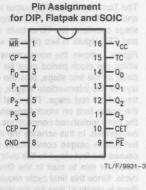
Ordering Code: See Section 8
Logic Symbols

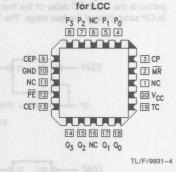
#### **Connection Diagrams**



| Pin Names                      | Description                     |
|--------------------------------|---------------------------------|
| CEP                            | Count Enable Parallel Input     |
| CET                            | Count Enable Trickle Input      |
| CP                             | Clock Pulse Input               |
| MR                             | Asynchronous Master Reset Input |
| P <sub>0</sub> -P <sub>3</sub> | Parallel Data Inputs            |
| PE                             | Parallel Enable Inputs          |
| Q <sub>0</sub> -Q <sub>3</sub> | Flip-Flop Outputs               |
| TC                             | Terminal Count Output           |

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Pin Assignment

#### **Functional Description**

The 'AC/'ACT161 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Five control inputs-Master Reset, Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on MR overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on PE overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and MR HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET

The 'AC/'ACT161 use D-type edge-triggered flip-flops and changing the PE, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle requires 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject

to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters.

When the Output Enable  $(\overline{OE})$  is LOW, the parallel data outputs  $O_0-O_3$  are active and follow the flip-flop Q outputs. A HIGH signal on  $\overline{OE}$  forces  $O_0-O_3$  to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET •  $\overline{\text{PE}}$  $\text{TC} = \text{Q}_0 \bullet \text{Q}_1 \bullet \text{Q}_2 \bullet \text{Q}_3 \bullet \text{CET}$ 

#### Mode Select Table

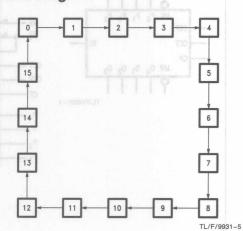
| PE       | CET      |             | Action on the Rising<br>Clock Edge () |
|----------|----------|-------------|---------------------------------------|
| X        | X cour   | X           | Reset (Clear)                         |
| Til teas | X        | X           | Load $(P_n \rightarrow Q_n)$          |
| H        | mo H sea | not the etc | Count (Increment)                     |
| Н        | L        | X           | No Change (Hold)                      |
| Н        | X        | L           | No Change (Hold)                      |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

#### **State Diagram**



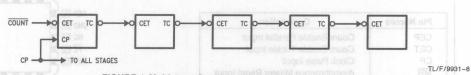
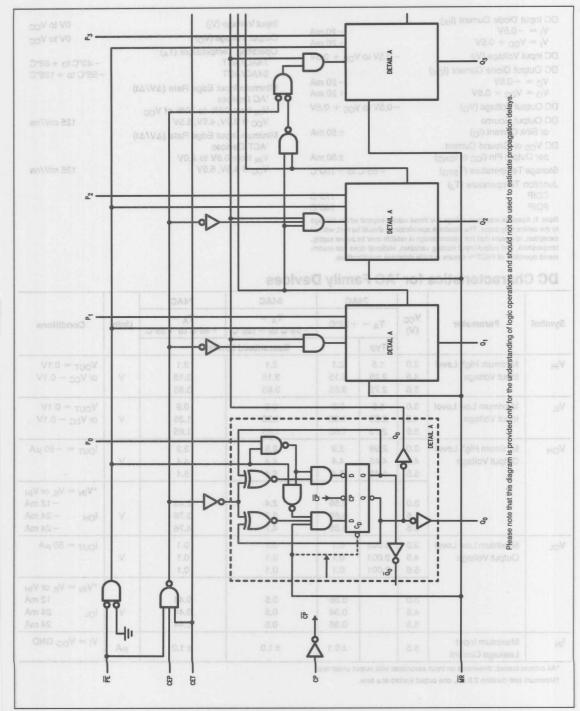


FIGURE 1. Multistage Counter with Ripple Carry

COUNT — CET TC — CEP — CEP — CET TC — C

FIGURE 2. Multistage Counter with Lookahead Carry

.TL/F/9931-9



CDIP

PDIP

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> ) | -0.5V  to  +7.0V      |
|-----------------------------------|-----------------------|
| DC Input Diode Current (IIK)      |                       |
| $V_{I} = -0.5V$                   | -20 mA                |
| $V_I = V_{CC} + 0.5V$             | + 20 mA               |
| DC Input Voltage (Vi)             | -0.5V to Vcc $+0.5$ V |

| DC Output Diode Current (IOK)       |                              |
|-------------------------------------|------------------------------|
| $V_{O} = -0.5V$                     | -20 mA                       |
| $V_O = V_{CC} + 0.5V$               | + 20 mA                      |
| DC Output Voltage (V <sub>O</sub> ) | $-0.5$ V to $V_{CC} + 0.5$ V |

DC Output Voltage (V<sub>O</sub>) = 0.5V to V<sub>CC</sub> + 0.5V

DC Output Source
or Sink Current (I<sub>O</sub>) ±50 mA

DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±50 mA
Storage Temperature (T<sub>STG</sub>) -65°C to +150°C
Junction Temperature (T<sub>J</sub>)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating 10 10018 Conditions

| Supply Voltage (V <sub>CC</sub> ) |                       |
|-----------------------------------|-----------------------|
| 'AC                               | 2.0V to 6.0V          |
| 'ACT                              | 4.5V to 5.5V          |
| Input Voltage (V <sub>I</sub> )   | 0V to V <sub>CC</sub> |
| Output Voltage (V <sub>O</sub> )  | 0V to V <sub>CC</sub> |

 Operating Temperature (T<sub>A</sub>)
 -40°C to +85°C

 74AC/ACT
 -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'ACT Devices  $V_{IN}$  from 0.8V to 2.0V

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

125 mV/ns

#### DC Characteristics for 'AC Family Devices

|                 |  |                        | 74                      | AC                   | 54AC                             | 74AC                            |       |   |  |
|-----------------|--|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|---|--|
| Symbol          | Parameter  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |  |
|                 | B. Company   |                        | Тур                     | 1                    | Guaranteed Li                    | mits                            |       |   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage   | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 | ्या प्रकार का अप का अप<br>क्रिक्ट स्थापित स्थापि | 3.0<br>4.5<br>5.5      | -00                     | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | ٧     | $\label{eq:VIN} \begin{split} * V_{\text{IN}} &= V_{\text{IL}}  \text{or}  V_{\text{IH}} \\ &- 12  \text{mA} \\ I_{\text{OH}} &- 24  \text{mA} \\ &- 24  \text{mA} \end{split}$   |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V     | I <sub>OUT</sub> = 50 μA  |  |
|                 |  | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.5<br>0.5<br>0.5                | 0.44<br>0.44<br>0.44            | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current   | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μА    | $V_I = V_{CC}$ , GND  |  |

175°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### 4

## DC Characteristics for 'AC Family Devices (Continued) The Indian Indiana India

|        | 74AC                                |                        | 74                     | AC  | 54AC                             | 74AC                            |       |  |  |
|--------|-------------------------------------|------------------------|------------------------|-----|----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |     | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                               |  |
|        | CL = 50 pF                          | 1 3                    | Тур                    |     | Guaranteed L                     | imits                           |       |  |  |
| lold   | †Minimum Dynamic                    | 5.5                    | E 201                  | 2.0 | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD   | Output Current                      | 5.5                    | 0                      |     | 50 011                           | 0.8 -75                         | mA    | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | 0.                     | 4.0 | 80.0                             | 40.0                            | μΑ    | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### DC Characteristics for 'ACT Family Devices

|                  | 1.5 11                               | 0.81                | 74/            | ACT          | 54ACT                             | 74ACT                           | veloci e     | pitagago19 HJql  |  |
|------------------|--------------------------------------|---------------------|----------------|--------------|-----------------------------------|---------------------------------|--------------|--|--|
| Symbol           | Parameter                            | V <sub>CC</sub> (V) | VCC TA = +25°C |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units        | Conditions   |  |
|                  | 1.5 9.5 n                            | 0.11                | Тур            | 1 2          | Guaranteed L                      |                                 | OET (6 TC    |  |  |
| V <sub>IH</sub>  | Minimum High Level Input Voltage     | 4.5<br>5.5          | 1.5<br>1.5     | 2.0          | 2.0                               | 2.0<br>2.0                      | n Delay      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VILS             | Maximum Low Level Input Voltage      | 4.5<br>5.5          | 1.5<br>1.5     | 0.8          | 0.8                               | 0.8<br>0.8                      | n Delay<br>V | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ASTO AO      | $I_{OUT} = -50 \mu A$  |  |
|                  |                                      | 4.5<br>5.5          |                | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | V            | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ m/}$ $-24 \text{ m/}$           |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 4.5<br>5.5          | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | V            | $I_{OUT} = 50 \mu A$   |  |
|                  |                                      | 4.5<br>5.5          |                | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | V            | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = 24 \text{ m/s}$ $24 \text{ m/s}$ |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     | 5.5                 |                | ±0.1         | ±1.0                              | ± 1.0                           | μΑ           | $V_I = V_{CC}$ , GND   |  |
| ГССТ             | Maximum I <sub>CC</sub> /Input       | 5.5                 | 0.6            |              | 1.6                               | 1.5                             | mA           | $V_{\rm I} = V_{\rm CC} - 2.1V$  |  |
| I <sub>OLD</sub> | †Minimum Dynamic                     | 5.5                 |                |              | 50                                | 75                              | mA           | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD             | Output Current                       | 5.5                 |                |              | -50                               | -75                             | mA           | V <sub>OHD</sub> = 3.85V Mir   |  |
| lcc              | Maximum Quiescent<br>Supply Current  | 5.5                 |                | 4.0          | 80.0                              | 40.0                            | μΑ           | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

 $<sup>\</sup>dagger$ Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{CC}$  for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics: See Section 2 for waveforms OA not applied to the section 2 for waveforms

|                      |  |                           |            | 25                |            | 74AC                  |            | 54           | AC                      | 74           | 1AC                       |       |     |
|----------------------|--|---------------------------|------------|-------------------|------------|-----------------------|------------|--------------|-------------------------|--------------|---------------------------|-------|-----|
| Symbol               | base3 Pa   | arameter                  |            | V <sub>CC</sub> * | Jase C     | A = +25°<br>CL = 50 p | °C         | to +         | -55°C<br>125°C<br>50 pF | to H         | -40°C<br>-85°C<br>- 50 pF | Units | Fig |
|                      |  |                           |            |                   | Min        | Тур                   | Max        | Min          | Max                     | Min          | Max                       |       |     |
| f <sub>max</sub>     | Maximum<br>Frequency   |                           | 75         | 3.3<br>5.0        | 70<br>110  | 111<br>167            |            | 55<br>80     | 8.8                     | 60<br>95     | andmorph<br>sut Curren    | MHz   | OHO |
| t <sub>PLH</sub>     | (PE Input HIGH or LOW)   |                           |            | 3.3<br>5.0        | 2.0<br>1.5 | 7.0<br>5.0            | 12<br>9.0  | 1.0<br>1.0   | 15.0<br>11.0            | 1.5<br>1.0   | 13.5<br>9.5               | ns    | 2-3 |
| <sup>t</sup> PHL     | Propagation Delay CP to Q <sub>n</sub><br>(PE Input HIGH or LOW) |                           |            | 3.3<br>5.0        | 1.5<br>1.5 | 7.0<br>5.0            | 12<br>9.5  | 1.0          | 15.0<br>11.0            | 1.5          | 13<br>10                  | ns    | 2-3 |
| t <sub>PLH</sub>     | Propagation Delay<br>CP to TC                                    |                           | 3.3<br>5.0 | 3.0<br>2.0        | 9          | 15<br>10.5            | 1.0<br>1.0 | 18.5<br>13.0 | 2.5<br>1.5              | 16.5<br>11.5 | ns                        | 2-3   |     |
| t <sub>PHL</sub>     | Propagation CP to TC   | on Delay                  |            | 3.3<br>5.0        | 3.5        | 8.5<br>6.5            | 14         | 1.0          | 17.5<br>13.0            | 2.5<br>2.0   | 15.5<br>11.5              | ns    | 2-3 |
| t <sub>PLH</sub>     | Propagation CET to TC  |                           | 10         | 3.3<br>5.0        | 2.0<br>1.5 | 5.5<br>3.5            | 9.5<br>6.5 | 1.0<br>1.0   | 13.0<br>8.5             | 1.5<br>1.0   | 11<br>7,5                 | ns    | 2-3 |
| t <sub>PHL</sub>     | Propagation<br>CET to TC   |                           | 3.58 + 8   | 3.3<br>5.0        | 2.5<br>2.0 | 6.5<br>5              | 11<br>8.5  | 1.0          | 14.5<br>11.0            | 2.0<br>1.5   | 12.5<br>9.5               | ns    | 2-3 |
| t <sub>PHL</sub> Vt. | Propagation MR to Qn   | on Delay                  | 9          | 3.3<br>5.0        | 2.0<br>1.5 | 6.5<br>5.5            | 12<br>9.5  | 1.0          | 14.5<br>10.5            | 1.5          | 13.5                      | ns    | 2-3 |
| t <sub>PHL</sub> VI  | Propagation MR to TC   | n Delay                   | 8          | 3.3               | 3.5<br>2.5 | 10<br>8.5             | 15<br>13   | 1.0          | 18.5<br>14.0            | 3.0<br>2.5   | 17.5<br>13.5              | ns    | 2-3 |
|                      |  | 1aily6 3.0 18 3.0 4 ±0.34 |            | 4.<br>5.          |            | 4.6                   | A.         |              |                         |              |                           |       | НО  |
|                      |  |                           |            |                   |            |                       |            |              |                         |              |                           |       |     |
|                      |  |                           |            |                   |            |                       |            |              |                         |              |                           |       |     |
|                      |  |                           |            |                   |            |                       |            |              |                         |              |                           |       |     |
|                      |  |                           |            |                   |            |                       |            |              |                         |              |                           |       |     |
|                      |  |                           |            |                   |            |                       |            |              |                         |              |                           |       |     |
|                      |  |                           |            |                   |            |                       |            |              |                         |              |                           |       |     |
|                      |  |                           |            |                   |            |                       |            |              |                         |              |                           |       |     |
|                      |  |                           |            | 40                |            |                       |            |              |                         |              |                           |       |     |

All outputs loaded; thresholds on input associated with output

Note: Icc for 54ACT @ 1870 is identical to 74ADT @ 2510.

| - |  |
|---|--|
|   |  |

|                  |                         |                               |    | SAACS                 | 744   | C           | 54AC  | 74AC                 |          |      |
|------------------|-------------------------|-------------------------------|----|-----------------------|---|-------------|---|----------------------|----------|------|
| Symbol           | MnU                     | Parameter                     |    | V <sub>CC</sub> * (V) | V <sub>CC</sub> * T <sub>A</sub> = + C <sub>L</sub> = 5 |             | $T_A = -55^{\circ}$<br>to + 125°0<br>$C_L = 50 p$ | to +85°C             | Units    | Fig. |
|                  |                         |                               |    |                       | Тур   | mark.       | Guaranteed  | Minimum              |          |      |
| t <sub>s</sub>   | Setup Time, HIGH or LOW |                               | OW | 3.3<br>5.0            | 6.0<br>3.5  | 13.5<br>8.5 | 16.0<br>10.5                                      | WO 1 16<br>10.5      | dura ins | 2-7  |
| t <sub>h</sub>   | Hold T                  | ime, HIGH or LO               | WC | 3.3<br>5.0            | -7.0<br>-4.0  | -1<br>00    | 0.5   | -0.5<br>0            | Tolons   | 2-7  |
| t <sub>s</sub>   | Setup<br>PE to          | Time, HIGH or I               | OW | 3.3<br>5.0            | 6.5<br>4.0  | 11.5<br>7.5 | 15.0<br>10.5                                      | 14<br>8.5            | ns ns    | 2-7  |
| t <sub>h</sub>   | Hold T                  | ime, HIGH or LO               | WC | 3.3<br>5.0            | -6.0<br>-3.5  | 0<br>0.5    | -1.0<br>0.0                                       | WOU to HEAH or UCW   | loins    | 2-7  |
| t <sub>s</sub>   |                         | Time, HIGH or I               | OW | 3.3<br>5.0            | 3.0<br>2.0  | 6.0<br>4.5  | 7.5<br>5.5  | WO J to HO 7 6 6 6 7 | ns       | 2-7  |
| t <sub>h</sub>   |                         | ime, HIGH or LO               | WC | 3.3<br>5.0            | -3.5<br>-2  | 0           | 2.0   | 0 0.5                | ns       | 2-7  |
| t <sub>w</sub>   |                         | Pulse Width<br>HIGH or LOW    |    | 3.3<br>5.0            | 2.0   | 3.5<br>2.5  | 5.0<br>5.0  | 4 3                  | oolins   | 2-3  |
| t <sub>w</sub>   |                         | Pulse Width<br>t) HIGH or LOW |    | 3.3<br>5.0            | 2.0<br>2.0  | 4.0<br>3.0  | 5.0<br>5.0  | 4.5<br>3.5           | ns       | 2-3  |
| tw               | MR Pu<br>LOW            | lse Width,                    |    | 3.3<br>5.0            | 3.0<br>2.5  | 5.5<br>4.5  | 5.0<br>5.0  | 7.5<br>6.0           | Ans      | 2-3  |
| t <sub>rec</sub> | Recov<br>MR to          | ery Time<br>CP                |    |                       | -2<br>-1  | -0.5<br>0   | 0.1.5<br>2.0                                      | 0<br>0.5             | ns       | 2-3, |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

## AC Electrical Characteristics: See Section 2 for Waveforms

|                  | Vo.8 =  | Vac               |  | 74ACT |      | 54/    | ACT                     | 74   | ACT  | City  |       |
|------------------|---|-------------------|--|-------|------|--------|-------------------------|--|------|-------|-------|
| Symbol           | Parameter   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | * to + | −55°C<br>125°C<br>50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.  |
|                  |   |                   | Min  | Тур   | Max  | Min    | Max                     | Min  | Max  |       |       |
| f <sub>max</sub> | Maximum Count<br>Frequency                                    | 5.0               | 115  | 125   |      |        |                         | 100  |      | MHz   |       |
| t <sub>PLH</sub> | Propagation Delay CP to Qn<br>(PE Input HIGH or LOW)          | 5.0               | 1.5  | 5.5   | 9.5  |        |                         | 1.5  | 10.5 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay CP to Q <sub>n</sub> (PE Input HIGH or LOW) | 5.0               | 1.5  | 6.0   | 10.5 |        |                         | 1.5  | 11.5 | ns    | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay<br>CP to TC                                 | 5.0               | 2.0  | 7.0   | 11.0 |        |                         | 1.5  | 12.5 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay<br>CP to TC                                 | 5.0               | 1.5  | 8.0   | 12.5 |        |                         | 1.5  | 13.5 | ns    | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay<br>CET to TC                                | 5.0               | 1.5  | 5.5   | 8.5  |        | 11.7                    | 1.5  | 10.0 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay<br>CET to TC                                | 5.0               | 1.5  | 6.5   | 9.5  |        |                         | 1.5  | 10.5 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay MR to Qn                                    | 5.0               | 1.5  | 6.0   | 10.0 |        |                         | 1.5  | 11.0 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay MR to TC                                    | 5.0               | 2.5  | 8.0   | 13.5 |        |                         | 2.0  | 14.5 | ns    | 2-3,4 |

# AC Operating Requirements: See Section 2 for Waveforms

|                   |                           | UNION                               | DANG      | 74A                | СТ   | 54ACT   | 74ACT  |       |             |
|-------------------|---------------------------|-------------------------------------|-----------|--------------------|------|---|--|-------|-------------|
| Symbol            | atinU                     | Parameter                           | (-)       | T <sub>A</sub> = - |      | $T_A = -55^{\circ}C$ to + 125°C $C_L = 50 \text{ pF}$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig.<br>No. |
|                   |                           |                                     | Cuerantes | Тур                | dåi  | Guaranteed Min  | nimum  |       |             |
| ts                | Setu<br>P <sub>n</sub> to | p Time, HIGH or LOW                 | 5.0       | 4.0                | 9.5  | 8.8 W   | 11.5 90  | ns    | 2-3,4       |
| th-S              | Hold<br>P <sub>n</sub> to | Time, HIGH or LOW                   | 5.0       | -5.0               | 0.7  | W 8.3   | CP 0   | ns    | 2-3,4       |
| ts                | Setu<br>PE to             | p Time, HIGH or LOW<br>CP           | 5.0       | 4.0                | 8.5  | 0.8   | 9.5  | ns    | 2-3,4       |
| th                | Hold<br>PE to             | Time, HIGH or LOW                   | 5.0       | -5.5               | -0.5 | 5.8 W   |  | ns    | 2-3,4       |
| ts                |                           | p Time, HIGH or LOW<br>or CET to CP | 5.0       | 2.5                | 5.5  | 6.8 -W.C  | 906.513010   | ns    | 2-3,4       |
| th-S              | College College           | Time, HIGH or LOW or CET to CP      | 0.5.0     | -3.0               | 0    | 8.8 W   | or CET 10 CP   | 99 ns | 2-3,4       |
| t <sub>w</sub> -S |                           | k Pulse Width<br>d) HIGH or LOW     | 5.0       | 2.0                | 3.0  | 0,8   | WOJ 3.5 IDIH (t                                      | ns    | 2-3         |
| t <sub>w</sub>    |                           | k Pulse Width<br>nt) HIGH or LOW    | 5.0       | 2.0                | 3.0  | 8.0   | WOLL 3.5 DIH (In                                     |       | 2-3         |
| tw                | ∘MR F                     | Pulse Width, LOW                    | 5.0       | 3.0                | 3.0  | 6.6   | 7.5  | ns    | 2-3         |
| t <sub>rec</sub>  | Reco                      | overy Time<br>o CP                  | 5.0       | 0                  | 0    |   | 0.5 T yray   | ns    | 2-3,7       |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

### Capacitance

|      | Symbo           | ol | Para                 | meter            | T | ур  | Units | 3              | Cor | nditions                       |        |
|------|-----------------|----|----------------------|------------------|---|-----|-------|----------------|-----|--------------------------------|--------|
|      | CIN             |    | Input Ca             | pacitance        | 4 | 1.5 | pF    |                | Vcc | ; = 5.0V                       |        |
| Fig. | C <sub>PD</sub> | 0  | Power Di<br>Capacita | ssipation<br>nce | 4 | 5.0 | pF    | T <sub>a</sub> | Vcc | ; = 5.0V                       | Symbol |
|      |                 |    |                      |                  |   |     |       |                |     |                                |        |
|      |                 |    | 100                  |                  |   |     |       |                |     |                                |        |
|      |                 |    |                      |                  |   |     |       |                |     |                                |        |
|      | an              |    |                      |                  |   |     |       |                |     |                                |        |
|      |                 |    |                      |                  |   |     |       |                |     |                                |        |
|      |                 |    |                      |                  |   |     |       |                |     | Propagation Dalay<br>CP to TC  |        |
|      |                 |    |                      |                  |   |     |       |                |     |                                |        |
|      |                 |    |                      |                  |   |     |       |                |     | Propagation Dalay<br>CET to TC |        |
|      |                 |    |                      |                  |   |     |       |                |     |                                |        |
|      |                 |    |                      |                  |   |     |       |                |     |                                |        |



## 54AC/74AC163 • 54ACT/74ACT163 **Synchronous Presettable Binary Counter**

#### **General Description**

The 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/ 'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

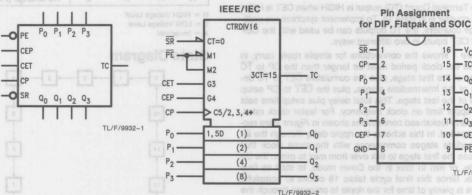
#### **Features**

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count rate of 125 MHz
- Outputs source/sink 24 mA
- 'ACT163 has TTL-compatible inputs
- Standard Military Drawing (SMD)

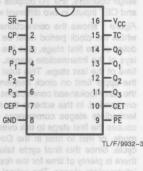
- 'AC163: 5962-89582

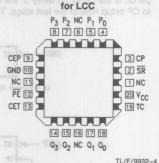
## Ordering Code: See Section 8 **Logic Symbols**

#### **Connection Diagrams**



| Pin Names                      | Description                 |  |  |  |  |  |
|--------------------------------|-----------------------------|--|--|--|--|--|
| CEP                            | Count Enable Parallel Input |  |  |  |  |  |
| CET                            | Count Enable Trickle Input  |  |  |  |  |  |
| CP                             | Clock Pulse Input           |  |  |  |  |  |
| SR                             | Synchronous Reset Input     |  |  |  |  |  |
| P <sub>0</sub> -P <sub>3</sub> | Parallel Data Inputs        |  |  |  |  |  |
| PE                             | Parallel Enable Input       |  |  |  |  |  |
| Q <sub>0</sub> -Q <sub>3</sub> | Flip-Flop Outputs           |  |  |  |  |  |
| TC                             | Terminal Count Output       |  |  |  |  |  |





Pin Assignment

#### **Functional Description**

The 'AC/'ACT163 counts in modulo-16 binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: synchronous reset, parallel load, count-up and hold. Four control inputs-Synchronous Reset (SR), Parallel Enable (PE), Count Enable Parallel (CEP) and Count Enable Trickle (CET)-determine the mode of operation, as shown in the Mode Select Table. A LOW signal on SR overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on PE overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With PE and SR HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT163 uses D-type edge-triggered flip-flops and changing the  $\overline{SR}$ ,  $\overline{PE}$ , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways.

Figure 1 shows the connections for simple ripple carry, in which the clock period must be longer than the CP to TC delay of the first stage, plus the cumulative CET to TC delays of the intermediate stages, plus the CET to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure 2 are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 16 clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to TC delay of the first stage plus the CEP to CP setup time of the last stage. The TC output is subject

to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry  $(\overline{CC})$  output is provided. The  $\overline{CC}$  output is normally HIGH. When  $\overline{CEP}$ ,  $\overline{CET}$ , and  $\overline{TC}$  are LOW, the  $\overline{CC}$  output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the  $\overline{CC}$  Truth Table. When the Output Enable  $(\overline{OE})$  is LOW, the parallel data outputs  $O_0-O_3$  are active and follow the flip-flop Q outputs. A HIGH signal on  $\overline{OE}$  forces  $O_0-O_3$  to the High Z state but does not prevent counting, loading or resetting.

Logic Equations: Count Enable = CEP • CET •  $\overline{PE}$  $TC = Q_0 • Q_1 • Q_2 • Q_3 • CET$ 

#### Mode Select Table

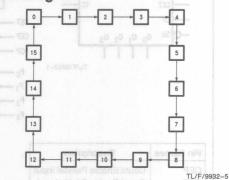
| SR | PE  | CET | CEP  | Action on the Rising Clock Edge () |
|----|-----|-----|------|------------------------------------|
| L  | X   | X   | X    | Reset (Clear)                      |
| Н  | L 8 | X   | X    | Load $(P_n \rightarrow Q_n)$       |
| Н  | Н   | Н   | Holo | Count (Increment)                  |
| Н  | Н   | L   | X    | No Change (Hold)                   |
| Н  | Н   | X   | L    | No Change (Hold)                   |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

#### **State Diagram**



CET TC O CET

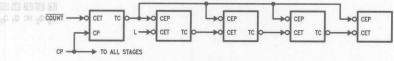
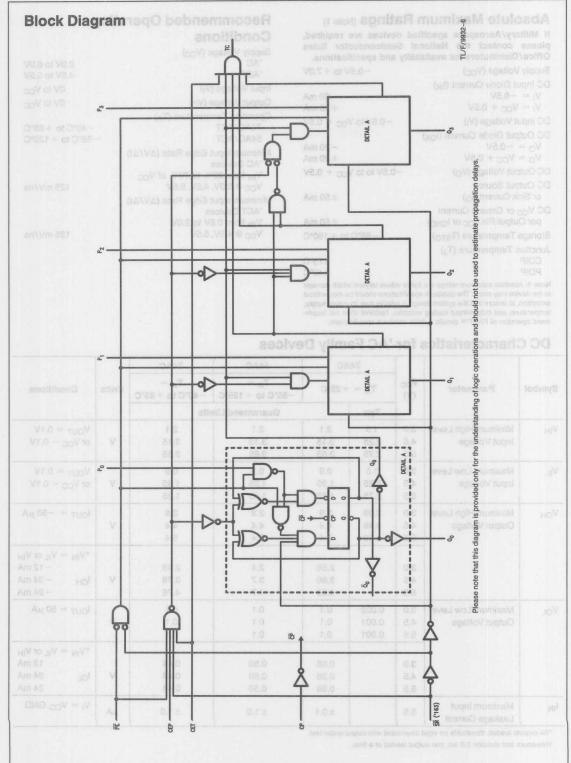


FIGURE 2

TL/F/9932-9



#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (VCC) -0.5V to +7.0VDC Input Diode Current (I<sub>IK</sub>)  $V_1 = -0.5V$ -20 mA  $V_I = V_{CC} + 0.5V$ +20 mA

DC Input Voltage (V<sub>I</sub>) DC Output Diode Current (IOK)

 $V_0 = -0.5V$ -20 mA  $V_O = V_{CC} + 0.5V$ + 20 mA DC Output Voltage (Vo) -0.5V to to  $V_{CC} + 0.5V$ 

-0.5V to  $V_{CC} + 0.5V$ 

±50 mA

175°C

140°C

-65°C to +150°C

DC Output Source  $\pm$  50 mA or Sink Current (IO) DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) Storage Temperature (TSTG) Junction Temperature (T<sub>J</sub>)

CDIP PDIP Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without

#### Recommended Operating Conditions

Supply Voltage (VCC) 'AC 'ACT

Input Voltage (VI)

2.0V to 6.0V 4.5V to 5.5V OV to VCC OV to VCC

Output Voltage (Vo) Operating Temperature (TA)

74AC/ACT -40°C to +85°C 54AC/ACT -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

#### DC Characteristics for 'AC Family Devices

exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

|                 | 18 95                                |                        | 74                      | AC                   | 54AC                             | 74AC                            | -     |   |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|---|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |
|                 |                                      | Locate                 | Тур                     | projection of        | Guaranteed Lin                   | nits                            |       |   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu\text{A}$   |
|                 | aidt taitr aton so                   | 3.0<br>4.5<br>5.5      | 7                       | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | V     | $\label{eq:VIN} \begin{split} * V_{\text{IN}} &= V_{\text{IL}}  \text{or}  V_{\text{IH}} \\ &- 12  \text{mA} \\ I_{\text{OH}} &- 24  \text{mA} \\ &- 24  \text{mA} \end{split}$ |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V     | I <sub>OUT</sub> = 50 μA  |
|                 | \$                                   | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | V     | $^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $^{12} \text{ mA}$ $^{\text{IOL}}$ $^{24} \text{ mA}$   |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μΑ    | $V_{I} = V_{CC}$ , GND  |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'AC Family Devices (Continued)

|               | TAAC                                |                        | 74A                | C      | 54AC                             | 74AC                            |       |  |
|---------------|-------------------------------------|------------------------|--------------------|--------|----------------------------------|---------------------------------|-------|--|
| Symbol        | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = + | - 25°C | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                               |
|               | CL = 50 pF                          | - 3                    | Тур                |        | Guaranteed Lir                   | nits                            |       |  |
| IOLD          | †Minimum Dynamic                    | 5.5                    | 1910               | XSN    | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max             |
| IOHD          | Output Current                      | 5.5                    | 0.0                |        | -50                              | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min             |
| lcc<br>A.S.S. | Maximum Quiescent<br>Supply Current | 5.5                    | 0.1                | 8.0    | 160.0                            | 8.6 80.0 61 90 3                | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

### DC Characteristics for 'ACT Family Devices

| 2-8,4           | 2.0 11.5                                      | 11.0                   | 744                            | CT           |                   | 54ACT                         | 0.7         | 74ACT                          | A Delay       | UPPL PROPERTY OF TO   |
|-----------------|---|------------------------|--------------------------------|--------------|-------------------|-------------------------------|-------------|--------------------------------|---------------|---|
| Symbol          | Parameter                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub>                 | + 25°C       |                   | T <sub>A</sub> = 2 to + 125°C | 1 1000      | T <sub>A</sub> =<br>C to +85°C | Units         | Conditions  |
|                 | 2.0 12.6                                      | 0.81                   | Тур                            | 0            | 11 (              | Guaranteed L                  | imits       |                                | velaCi n      | tour Propagation  |
| VIH             | Minimum High Level<br>Input Voltage           | 4.5<br>5.5             | 1.5                            | 2.0          | 8                 | 2.0                           | 0.7         | 2.0                            | V VS O E VE   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage            | 4.5<br>5.5             | 1.5<br>1.5                     | 0.8          | acus soli S       | 0.8                           | Saire       | 0.8                            | ٧             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage          | 4.5<br>5.5             | 4.49<br>5.49                   | 4.4<br>5.4   | DA.               | 4.4<br>5.4                    |             | 4.4<br>5.4                     | ٧             | $I_{OUT} = -50 \mu\text{A}$   |
|                 | TA = -49°C<br>to +85°C<br>Units<br>Ct = 50 pF | 4.5<br>5.5             | 1 = -88<br>2 + 126<br>1 = 80 p | 3.86<br>4.86 | +25°C<br>50 pF    |                               | Vcc*<br>(V) | 3.76<br>4.76                   | Paronse       | $V_{\rm IN} = V_{\rm IL} \text{ or } V_{\rm IH} \\ -24 \text{ mA} \\ -24 \text{ mA}$  |
| VoL             | Maximum Low Level Output Voltage              | 4.5<br>5.5             | 0.001<br>0.001                 | 0.1<br>0.1   | 18.6              | 0.1                           | 8.8         | 0.1<br>0.1/O.J to H            | ime, Htd      | I <sub>OUT</sub> = 50 μA  |
|                 | en 0.5  | 4.5<br>5.5             | 11.0<br>- 0.6                  | 0.36<br>0.36 | 8.6<br>3.1 —<br>0 | 0.50                          | 8.8<br>8.0  | 0.44                           | ne, yildi     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current              | 5.5                    | 17:0                           | ±0.1         | 14.0              | ±1.0                          | 8.3         | ±1.0                           | μА            | V <sub>I</sub> = V <sub>CC</sub> , GND  |
| ICCT            | Maximum 8.0—<br>I <sub>CC</sub> /Input        | 5.5                    | 0.6                            |              | 0.1-<br>5.0-      | 1.6                           | 9.3         | 1.5                            | mA            | $V_I = V_{CC} - 2.1V$   |
| IOLD            | †Minimum Dynamic                              | 5.5                    | 18.0                           |              | 3.15              | 50                            | 8.8         | 75 OJ 10 H                     | mA            | V <sub>OLD</sub> = 1.65V Max  |
| IOHD            | Output Current                                | 5.5                    | 8.5                            |              | 2.5               | -50                           | 6.8         | -75                            | mA            | V <sub>OHD</sub> = 3.85V Min  |
| Icc             | Maximum Quiescent<br>Supply Current           | 5.5                    | 6,0-                           | 8.0          | 1.0-              | 160.0                         | 8,8         | 80.0                           | μА            | V <sub>IN</sub> = V <sub>CC</sub> or GND  |
|                 |   |                        | TER                            |              | 0.8               | 20                            | 67.87       | THE UNITED THE SECOND          | Called morney | Causes I to   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## AC Electrical Characteristics: See Section 2 for waveforms 3 O.A. 103 apite harbaranto 3 O.A.

|                  | DAN   |                   |            | 74AC  |                 | 54         | AC                      | 74         | IAC                     |       |       |
|------------------|---|-------------------|------------|---|-----------------|------------|-------------------------|------------|-------------------------|-------|-------|
| Symbol           | Parameter Parameter   | V <sub>CC</sub> * | 0.981      | T <sub>A</sub> = +25<br>C <sub>L</sub> = 50 p | and the same of | to +       | −55°C<br>125°C<br>50 pF | to +       | -40°C<br>-85°C<br>50 pF | Units | Fig.  |
| Se NR 3/2(5)     | and American  | 8391              | Min        | Тур   | Max             | Min        | Max                     | Min        | Max                     |       |       |
| f <sub>max</sub> | Maximum Clock<br>Frequency  | 3.3<br>5.0        | 70<br>110  | 95<br>140                                     |                 | 55<br>90   | 8.6                     | 60<br>95   | ut Current              | MHz   | ariol |
| t <sub>PLH</sub> | Propagation Delay, CP to Q <sub>n</sub><br>(PE Input HIGH or LOW) | 3.3<br>5.0        | 2.0<br>1.5 | 7.5<br>5.5                                    | 12.5<br>9.0     | 1.0<br>1.0 | 13.5<br>9.5             | 1.5<br>1.0 | 13.5<br>9.5             | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay, CP to Q <sub>n</sub><br>(PE Input HIGH or LOW) | 3.3<br>5.0        | 1.5<br>1.5 | 8.5<br>6.0                                    | 12.0<br>9.5     | 1.0        | 12.5<br>9.5             | 1.5<br>1.5 | 13.0<br>10.0            | ns    | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay<br>CP to TC                                     | 3.3<br>5.0        | 3.0<br>2.0 | 9.5<br>7.0                                    | 15.0<br>10.5    | 1.0        | 16.5<br>11.0            | 2.5<br>1.5 | 16.5<br>11.5            | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay<br>CP to TC                                     | 3.3<br>5.0        | 3.5<br>2.0 | 11.0<br>8.0                                   | 14.0<br>11.0    | 1.0<br>1.0 | 15.0<br>11.0            | 2.5<br>2.0 | 15.5<br>11.5            | ns    | 2-3,4 |
| tpLHsnob         | Propagation Delay<br>CET to TC                                    | 3.3<br>5.0        | 2.0        | 7.5<br>5.5                                    | 9.5<br>6.5      | 1.0        | 11.0<br>7.5             | 1.5        | 11.0<br>7.5             | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay CET to TC                                       | 3.3<br>5.0        | 2.5        | 8.5<br>6.0                                    | 11.0<br>8.5     | 1.0        | 12.0<br>9.0             | 2.0        | 12.5                    | ns    | 2-3,4 |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Operating Requirements: See Section 2 for waveforms

| AAI US-                | 5.4 V 1007                                      |                   | 74.                               | AC           | 513      | 54AC                 | Ø. A              | 74AC   | Intribio | HO.           |
|------------------------|---|-------------------|-----------------------------------|--------------|----------|----------------------|-------------------|--|----------|---------------|
| Symbol                 |   | V <sub>CC</sub> * | T <sub>A</sub> = C <sub>L</sub> = |              | t        | o + 125°<br>c = 50 p | C                 | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | Units    | Fig.          |
| A., 02                 | = -rusl t.0                                     |                   | Тур                               |              | Gua      | aranteed             | Mini              | mum  | nive M   | To the second |
| ts                     | Setup Time, HIGH or LOW<br>P <sub>n</sub> to CP | 3.3<br>5.0        | 5.5<br>4.0                        | 13.5<br>8.5  | 1,0      | 17.0<br>11.0         | 8.8               | 16.0<br>10.5   | ns       | 2-7           |
| Ath AS<br>Am AS        | Hold Time, HIGH or LOW                          | 3.3<br>5.0        | -7.0<br>-5.0                      | -1.0<br>0    | 0.38     | -0.5<br>0            | #.5<br>8.6        | -0.5<br>0  | ns       | 2-7           |
| ts GND o               | Setup Time, HIGH or LOW<br>SR to CP             | 3.3<br>5.0        | 5.5<br>4.0                        | 14.0<br>9.5  | .D±      | 17.0<br>12.0         | 5,5               | 16.5<br>11.0   | ns       | 2-7           |
| th/1.5 - o             | Hold Time, HIGH or LOW<br>SR to CP              | 3.3<br>5.0        | -7.5<br>-5.5                      | -1.0<br>-0.5 |          | -0.5<br>0            | 6.8               | -0.5 mu  | ns       | 2-7           |
| t <sub>s</sub> A Vaa.r | Setup Time, HIGH or LOW<br>PE to CP             | 3.3<br>5.0        | 5.5<br>4.0                        | 11.5<br>7.5  |          | 16.0<br>9.5          | 8.8               | 14.0<br>8.5  | ns       | 2-7           |
| t <sub>h</sub>         | Hold Time, HIGH or LOW                          | 3.3<br>5.0        | -7.5<br>-5.0                      | -1.0<br>-0.5 | 0.8      | -0.5<br>0            | 3.6               | -0.5<br>0  | ns       | 2-7           |
| t <sub>s</sub>         | Setup Time, HIGH or LOW<br>CEP or CET to CP     | 3.3<br>5.0        | 3.5<br>2.5                        | 6.0<br>4.5   | ione Jac | 8.0<br>5.5           | fricosi<br>Secola | 7.0<br>5.0   | ns       | 2-7           |
| t <sub>h</sub>         | Hold Time, HIGH or LOW<br>CEP or CET to CP      | 3.3<br>5.0        | -4.5<br>-3.0                      | 0            |          | 0.5                  | 74AC              | 0.5  | ns       | 2-7           |
| t <sub>w</sub>         | Clock Pulse Width (Load)<br>HIGH or LOW         | 3.3<br>5.0        | 3.0<br>2.0                        | 3.5<br>2.5   |          | 5.0<br>5.0           |                   | 4.0<br>3.0   | ns       | 2-3           |
| t <sub>w</sub>         | Clock Pulse Width (Count)<br>HIGH or LOW        | 3.3<br>5.0        | 3.0<br>2.0                        | 4.0<br>3.0   |          | 5.0<br>5.0           |                   | 4.5<br>3.5   | ns       | 2-3           |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### 4

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  | anothibac   | 25                |     | 74ACT                            | Typ  | 54   | ACT                     | 74   | ACT                    | Symbol |             |
|------------------|---|-------------------|-----|----------------------------------|------|------|-------------------------|------|------------------------|--------|-------------|
| Symbol           | V0.8 = oc<br>Parameter<br>V0.8 = oc                               | V <sub>CC</sub> * |     | A = +25<br>C <sub>L</sub> = 50 p |      | to + | −55°C<br>125°C<br>50 pF | to + | -40°C<br>85°C<br>50 pF | Units  | Fig.<br>No. |
|                  |   |                   | Min | Тур                              | Max  | Min  | Max                     | Min  | Max                    |        |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency  | 5.0               | 120 | 140                              |      |      |                         | 105  |                        | MHz    |             |
| t <sub>PLH</sub> | Propagation Delay, CP to Q <sub>n</sub><br>(PE Input HIGH or LOW) | 5.0               | 1.5 | 5.5                              | 10.0 |      |                         | 1.5  | 11.0                   | ns     | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay, CP to Q <sub>n</sub><br>(PE Input HIGH or LOW) | 5.0               | 1.5 | 6.0                              | 11.0 |      |                         | 1.5  | 12.0                   | ns     | 2-3,4       |
| t <sub>PLH</sub> | Propagation Delay<br>CP to TC                                     | 5.0               | 2.5 | 7.0                              | 11.5 |      |                         | 2.0  | 13.5                   | ns     | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay<br>CP to TC                                     | 5.0               | 3.0 | 8.0                              | 13.5 |      |                         | 2.0  | 15.0                   | ns     | 2-3,4       |
| t <sub>PLH</sub> | Propagation Delay<br>CET to TC                                    | 5.0               | 2.0 | 5.5                              | 9.0  |      |                         | 1.5  | 10.5                   | ns     | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay<br>CET to TC                                    | 5.0               | 2.0 | 6.0                              | 10.0 |      |                         | 2.0  | 11.0                   | ns     | 2-3,4       |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

### AC Operating Requirements: See Section 2 for waveforms

|                |  | A 176-            | 74/  | ACT             | 54ACT   | 74ACT  |       |      |
|----------------|--|-------------------|------|-----------------|---|--|-------|------|
| Symbol         | Parameter                                      | V <sub>CC</sub> * |      | + 25°C<br>50 pF | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|                |  |                   | Тур  |                 | Guaranteed Min  | imum   |       |      |
| ts             | Setup Time, HIGH or LOW<br>Pn to CP            | 5.0               | 4.0  | 10.0            |   | 12.0   | ns    | 2-7  |
| th             | Hold Time, HIGH or LOW<br>P <sub>n</sub> to CP | 5.0               | -5.0 | 0.5             |   | 0.5  | ns    | 2-7  |
| ts             | Setup Time, HIGH or LOW SR to CP               | 5.0               | 4.0  | 10.0            |   | 11.5   | ns    | 2-7  |
| t <sub>h</sub> | Hold Time, HIGH or LOW<br>SR to CP             | 5.0               | -5.5 | -0.5            | 4   | -0.5   | ns    | 2-7  |
| ts             | Setup Time, HIGH or LOW PE to CP               | 5.0               | 4.0  | 8.5             |   | 10.5   | ns    | 2-7  |
| t <sub>h</sub> | Hold Time, HIGH or LOW<br>PE to CP             | 5.0               | -5.5 | -0.5            |   | 0  | ns    | 2-7  |
| ts             | Setup Time, HIGH or LOW<br>CEP or CET to CP    | 5.0               | 2.5  | 5.5             |   | 6.5  | ns    | 2-7  |
| t <sub>h</sub> | Hold Time, HIGH or LOW<br>CEP or CET to CP     | 5.0               | -3.0 | 0               |   | 0.5  | ns    | 2-7  |
| t <sub>w</sub> | Clock Pulse Width (Load)<br>HIGH or LOW        | 5.0               | 2.0  | 3.5             |   | 3.5  | ns    | 2-3  |
| t <sub>w</sub> | Clock Pulse Width<br>(Count) HIGH or LOW       | 5.0               | 2.0  | 3.5             |   | 3.5  | ns    | 2-3  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

|       | Symbo           | 1   | THACT     | Para   | ameter           | 54                       | Тур  | TOANG    | Jnits | C     | conditions           |  |
|-------|-----------------|-----|-----------|--------|------------------|--------------------------|------|----------|-------|-------|----------------------|--|
| 1,000 | CIN             | 970 | Inp       | out Ca | apacitance       | - A7                     | 4.5  |          | pF    | V     | <sub>CC</sub> = 5.0V |  |
| .obt  | C <sub>PD</sub> | 40  | 100 - 100 | wer E  | Dissipation ance | 10 +<br>C <sub>L</sub> = | 45.0 | q 08 = j | pF    | (V) V | CC = 5.0V            |  |
|       |                 | xsA | ā ni      | 86     | Mex              | nilii                    | Make | Typ      | niss  |       |                      |  |
|       | MHz             |     |           |        |                  |                          |      |          |       |       |                      |  |
|       |                 |     |           |        |                  |                          |      |          |       |       |                      |  |
|       |                 |     |           |        |                  |                          |      |          |       |       |                      |  |
|       |                 | 3.6 |           |        |                  |                          |      |          |       |       |                      |  |
|       |                 |     |           |        |                  |                          |      |          |       |       |                      |  |
|       |                 |     |           |        |                  |                          |      |          |       | 5.0   |                      |  |
|       |                 | 1.0 |           |        |                  |                          |      |          |       |       |                      |  |

Voltage No.5 of 5.5 aproaff spectroV\*

#### AC Operating Requirements: see Section 2 for waveform

|      |     | ZAACT   |      |  |  |
|------|-----|---|------|--|--|
| Fig. |     | $T_A = -40^{\circ}C$<br>to +85°C<br>$C_L = 50 \text{ pF}$ |      |  |  |
|      |     |   |      |  |  |
|      |     |   |      |  |  |
|      |     |   |      |  |  |
|      |     |   | 10.0 |  |  |
|      | en  |   |      |  |  |
|      |     |   |      |  |  |
|      |     |   |      |  |  |
|      |     |   |      |  |  |
|      | En  |   |      |  |  |
|      |     |   |      |  |  |
|      | BiT |   |      |  |  |

V8.011 V8.8 et 0.5 aprinR squiloV



## 54AC/74AC169 • 54ACT/74ACT169 4-Stage Synchronous Bidirectional Counter

#### **General Description**

The 'AC/'ACT169 is fully synchronous 4-stage up/down counter. The 'AC/'ACT169 is a modulo-16 binary counter. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

#### **Features**

- Synchronous counting and loading
- Built-In lookahead carry capability
- Presettable for programmable operation
- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs

#### Ordering Code: See Section 8

#### Logic Symbol

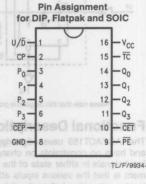
TL/F/9934-1

IEEE/IEC M1 (LOAD) M2 (COUNT) M3 (UP) 3,5CT = 15 M4 (DOWN) 4.5CT = 0 CEP\_ >2.3.5.6+/C7 2,4,5,6-Po-1,7D (2) (4) - Q2 (8)

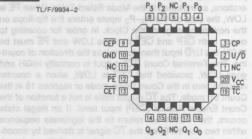
TL/F/9934-2

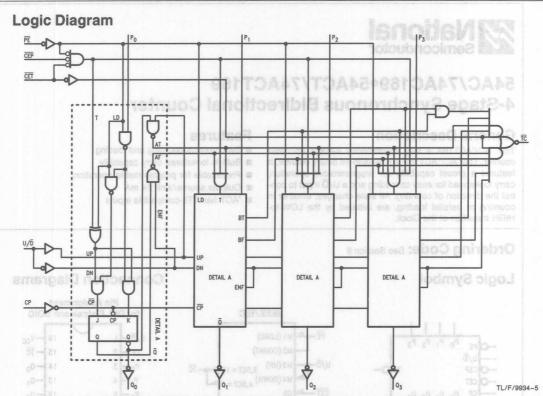
| Pin Names                      | Description                 |
|--------------------------------|-----------------------------|
| CEP                            | Count Enable Parallel Input |
| CET                            | Count Enable Trickle Input  |
| CP                             | Clock Pulse Input           |
| P <sub>0</sub> -P <sub>3</sub> | Parallel Data Inputs        |
| PE                             | Parallel Enable Input       |
| U/D                            | Up-Down Count Control Input |
| Q <sub>0</sub> -Q <sub>3</sub> | Flip-Flop Outputs           |
| TC                             | Terminal Count Output       |

#### **Connection Diagrams**



Pin Assignment for LCC





#### Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Functional Description**

The 'AC/'ACT169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When PE is LOW, the data on the P<sub>0</sub>-P<sub>3</sub> inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both CEP and CET must be LOW and PE must be HIGH; the U/D input then determines the direction of counting. The Terminal Count (TC) output is normally HIGH and goes LOW, provided that CET is LOW, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The TC output state is not a function of the Count Enable Parallel (CEP) input level. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the TC signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on TC. For this reason the use of TC as a clock signal is not recommended (see logic equations below).

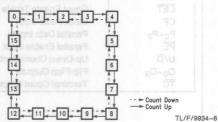
- 1) Count Enable = CEP•CET•PE
- 2) Up:  $\overline{TC} = Q_0 \circ Q_1 \circ Q_2 Q_3 \circ (Up) \circ \overline{CET}$
- 3) Down:  $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

#### Mode Select Table

| PE | CEP | CET | U/D | Action on Rising<br>Clock Edge |  |  |  |  |
|----|-----|-----|-----|--------------------------------|--|--|--|--|
| L  | X   | X   | X   | Load (Pn to Qn)                |  |  |  |  |
| Н  | L   | L   | Н   | Count Up (Increment)           |  |  |  |  |
| H  | L   | L   | L   | Count Down (Decrement)         |  |  |  |  |
| Н  | Н   | X   | X   | No Change (Hold)               |  |  |  |  |
| Н  | X   | Н   | X   | No Change (Hold)               |  |  |  |  |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial

#### **State Diagrams**



#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V Supply Voltage (Vcc) DC Input Diode Current (IIK)  $V_1 = -0.5V$ -20 mA  $V_I = V_{CC} + 0.5V$ +20 mA -0.5V to V<sub>CC</sub> + 0.5V DC Input Voltage (V<sub>I</sub>) DC Output Diode Current (IOK) -20 mA  $V_0 = -0.5V$  $V_O = V_{CC} + 0.5V$ +20 mA -0.5V to to  $V_{CC}$  + 0.5V DC Output Voltage (Vo)

DC Output Source or Sink Current (IO) ±50 mA DC V<sub>CC</sub> or Ground Current ±50 mA per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>)

Storage Temperature (TSTG) Junction Temperature (T,I) CDIP PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating **Conditions**

Supply Voltage (V<sub>CC</sub>) 2.0V to 6.0V 'AC 'ACT 4.5V to 5.5V OV to VCC Input Voltage (V<sub>I</sub>) OV to V<sub>CC</sub> Output Voltage (VO) Operating Temperature (T<sub>A</sub>)

74AC/ACT -40°C to +85°C 54AC/ACT -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

V<sub>CC</sub> @ 4.5V, 5.5V

V<sub>IN</sub> from 0.8V to 2.0V 125 mV/ns

#### DC Characteristics for 'AC Family Devices

-65°C to +150°C

175°C

140°C

| Symbol Am AS —                 | Parameter                            | 4,1                 | 74AC                    |                        | 4.4   | 54AC<br>T <sub>A</sub> =<br>-55°C to + 125°C |                    | 74AC<br>T <sub>A</sub> =<br>-40°C to +85°C | Units               | Conditions  |
|--------------------------------|--------------------------------------|---------------------|-------------------------|------------------------|-------|--|--------------------|--|---------------------|---|
|                                |                                      | V <sub>CC</sub> (V) | T <sub>A</sub> =        | T <sub>A</sub> = +25°C |       |  |                    |  |                     |   |
|                                |                                      |                     | Тур                     | Typ Guaranteed Limits  |       |  |                    |  |                     |   |
| V <sub>IH</sub> A <sub>A</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85    | 0.1   | 2.1<br>3.15<br>3.85                          | 1.0                | 2.1<br>3.15<br>3.85                        | n Lye Le            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| L or Villy<br>Am AS<br>Am AS   | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65    | 0.50  | 0.9<br>1.35<br>1.65                          | 86.0<br>85.0       | 0.9<br>1.35<br>1.65                        | V                   | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$   |
| V <sub>OH</sub>                | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4      | 0.f±  | 2.9<br>4.4<br>5.4                            | F.0.1              | 2.9<br>4.4<br>5.4                          | o Input             | $I_{OUT} = -50 \mu\text{A}$   |
|                                | = cuoV Am                            | 3.0<br>4.5<br>5.5   |                         | 2.56<br>3.86<br>4.86   | 80    | 2.4<br>3.7<br>4.7                            |                    | 2.46<br>3.76<br>4.76                       | n Dynar<br>Sun V st | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>-12 mA<br>I <sub>OH</sub> -24 mA<br>-24 mA |
| Vol                            | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1      | 160.0 | 0.1<br>0.1<br>0.1                            | 0.0<br>rebnu tuder | 0.1<br>0.1<br>0.1                          |                     | Ι <sub>ΟΟΤ</sub> = 50 μΑ  |
|                                |                                      | 3.0<br>4.5<br>5.5   |                         | 0.36<br>0.36<br>0.36   |       | 0.50<br>0.50<br>0.50                         |                    | 0.44<br>0.44<br>0.44                       | V                   | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA I <sub>OL</sub> 24 mA 24 mA             |
| I <sub>IN</sub>                | Maximum Input<br>Leakage Current     | 5.5                 |                         | ±0.1                   |       | ±1.0   |                    | ±1.0                                       | μА                  | $V_I = V_{CC}$ , GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued) with a murning M style ad A

|        |                                     |                        | 74AC               |                                  | 54AC |                            | 74AC                            | legs so:                    | If Military/Acrosp                       |  |
|--------|-------------------------------------|------------------------|--------------------|----------------------------------|------|----------------------------|---------------------------------|-----------------------------|--|--|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> + 2 |                                  | 2.6% | T <sub>A</sub> = to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                       | Conditions                               |  |
|        |                                     |                        | Тур                | Type show fund Guaranteed Limits |      |                            | Limits                          | C Input Diode Current (Ind) |  |  |
| IOLD   | †Minimum Dynamic                    | 5.5                    | dV) egs            | sloV h                           | Quip | 50                         | 75                              | mA                          | V <sub>OLD</sub> = 1.65V Max             |  |
| Iонр   | Output Current                      | 5.5                    | snegms<br>T        | T gride                          | PagO | -50 0.0 + 5                | oV of V8.⊕75                    | mA                          | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | Tr<br>out Edg      | 8.0                              | Sel  | 160.0                      | 80.0                            | μΑ                          | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# DC Characteristics for 'ACT Family Devices

|                      |                                      |                     | 744                    | CT           |                  | 4ACT         | e1 + a                              | 74ACT                             | (ara1) e   |  |
|----------------------|--------------------------------------|---------------------|------------------------|--------------|------------------|--------------|-------------------------------------|-----------------------------------|--|--|
| Symbol               | Parameter                            | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = |              |                                     | T <sub>A</sub> = -40°C to +85°    | Unite  | Conditions   |
|                      |                                      |                     | Тур                    |              | (                | Guara        | nteed L                             | imits                             | m retings are  | Mote 1: Absolute maxima  |
| V <sub>IH</sub>      | Minimum High Level<br>Input Voltage  | 4.5<br>5.5          | 1.5<br>1.5             | 2.0<br>2.0   |                  | 2.0          | power sup<br>es not nec<br>alicins. | 2.0<br>2.0                        | the system de<br>lept <b>V</b> locting<br>IN croults out | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>      | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5          | 1.5<br>1.5             | 0.8          | dees             | 0.8          | yllm                                | 0.8<br>0.8                        | es lite <b>X</b> re                                      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub>      | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49           | 4.4<br>5.4   | SAAC<br>TA =     | 4.4<br>5.4   | 0/                                  | 4.4<br>5.4                        | V  | $I_{OUT} = -50 \mu\text{A}$  |
| anoiss               | 900 SIBU 003                         | 4.5<br>5.5          | 0°08 —<br>aslan        | 3.86<br>4.86 | F 07 0 F         | 3.70<br>4.70 | 3.68                                | 3.76<br>4.76                      | V  | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| V <sub>OL</sub>      | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5          | 0.001<br>0.001         | 0.1          | 3.16<br>3.85     | 0.1          | 3.15                                | 0.1 <sub>a</sub> 0.1 <sub>a</sub> | A St   | I <sub>OUT</sub> = 50 μA   |
|                      | VOUT 90 V 00 V 00 V                  | 4.5<br>5.5          |                        | 0.36<br>0.36 | 1,35             | 0.50<br>0.50 | 1.35                                | 0.44                              | Low Level  | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| IN <sub>M</sub> oa-  | Maximum Input<br>Leakage Current     | 5.5                 |                        | ±0.1         | 2.9              | ±1.0         | 2.9                                 | 98.2 ±1.08                        | μΑ   | $V_I = V_{CC}$ , GND   |
| ICCT                 | Maximum<br>I <sub>CC</sub> /Input    | 5.5                 | 0.6                    |              | 5.4              | 1.6          | 5,4                                 | 1.5                               | mA   | $V_i = V_{CC} - 2.1V$  |
| IOLD                 | †Minimum Dynamic                     | 5.5                 |                        |              | 2.4              | 50           | 2.56                                | 75                                | mA   | V <sub>OLD</sub> = 1.65V Max   |
| I <sub>OHD</sub>     | Output Current                       | 5.5                 |                        |              | 3.7              | -50          | 3.86                                | -75                               | mA   | V <sub>OHD</sub> = 3.85V Min   |
| Icc <sub>Au 08</sub> | Maximum Quiescent<br>Supply Current  | 5.5                 |                        | 8.0          | 1.0              | 160.0        | 1.0                                 | \$00.0 80.0                       | μΑ   | V <sub>IN</sub> = V <sub>CC</sub> or GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  | TAAC   |                   | SAAG   | 74AC        | CAN  | 5        | 4AC  | 7          | 4AC                             |                |       |
|------------------|--|-------------------|--|-------------|--|----------|--|------------|---------------------------------|----------------|-------|
| Symbol           | Orot — AT<br>office Parameter of<br>Agos = JO      | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |          | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |            | Units                           | Fig.           |       |
|                  |  | in in             | verterialt to                                    | Min         | Тур  | Max      | Min  | Max        | Min                             | Max            |       |
| f <sub>max</sub> | Maximum Clock<br>Frequency                         | 3.3<br>5.0        | 75<br>100  | 118<br>154  | 4.5  | 55<br>75 | 8.8  | 65<br>90   | ap Time,<br>H or LOW            | MHz            |       |
| t <sub>PLH</sub> | Propagation Delay CP to Qn (PE HIGH or LOW)        | 3.3<br>5.0        | 2.5  | 9.5<br>7.0  | 13.0   | 1.0      | 15.0<br>12.0   | 2.0<br>1.5 | 14.5<br>11.0                    | ins            | 2-3,4 |
| <sup>†</sup> PHL | Propagation Delay CP to Qn (PE HIGH or LOW)        | 3.3<br>5.0        | 2.5  |             | 14.5   | 1.0      | 16.5<br>13.0   | 2.0<br>1.5 | 16.0<br>12.0                    | Olivins<br>130 | 2-3,4 |
| tplH             | Propagation Delay<br>CP to TC                      | 3.3<br>5.0        | 4.5  | 13.5<br>9.5 | 18.0   | 1.0      | 22.0<br>16.0   | 3.5        | 22.0<br>14.0                    | ns             | 2-3,4 |
| tPHL             | Propagation Delay CP to TC                         | 3.3<br>5.0        | 3.5<br>2.5                                       | 13.5<br>9.5 | 18.0   | 1.0      | 22.0<br>16.0   | 3.0<br>2.0 | 20.5                            | ns             | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay CET to TC                        | 3.3<br>5.0        | 3.5  | 11.0        | 15.0   | 1.0      | 18.5   | 3.0        | 16.5<br>12.0                    | ns             | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay CET to TC                        | 3.3<br>5.0        | 3.0<br>2.0                                       | 9.5<br>7.0  | 12.5<br>9.0  | 1.0      | 16.0<br>11.0   | 2.5<br>1.5 | 14.5<br>10.0                    | ns             | 2-3,4 |
| <sup>t</sup> PLH | Propagation Delay                                  | 3.3<br>5.0        | 3.5<br>2.5                                       | 11.0        | 15.0<br>10.5   | 1.0      | 18.5<br>13.0   | 3.0<br>2.0 | 17.0<br>12.0                    | ns             | 2-3,4 |
| tPHL             | Propagation Delay                                  | 3.3<br>5.0        | 2.5<br>1.5                                       | 10.0        | 13.5<br>9.5  | 1.0      | 16.5<br>12.0   | 2.0<br>1.5 | 15.5<br>10.5                    | 3 ns           | 2-3,4 |
|                  | lange 3.3 is 3.3V ±0.3V<br>Range 5.0 is 5.0V ±0.5V |                   | 0.81   |             | 10.0   | 7.0      | 3.3<br>6.0   |            | ip Time,<br>H or LOW<br>I to CP |                |       |
| 7-9              |  |                   |  |             |  | 7.0      |  |            |                                 |                |       |
|                  |  |                   |  |             |  |          |  |            |                                 |                |       |

# AC Operating Requirements: See Section 2 for waveforms, and labeled as a section 2 for waveforms.

|                    | YAAC                                    | DAN               | 3 7  | AAC DA      | 54AC  | 74AC   |                  |      |
|--------------------|---|-------------------|--|-------------|---|--|------------------|------|
| Symbol             | Parameter :                             | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units            | Fig. |
|                    | xsM nM                                  | xeM               | тур хам съ                                       |             | Guaranteed Minimum  |  |                  |      |
| t <sub>s</sub>     | Setup Time,<br>HIGH or LOW              | 3.3<br>5.0        | 3.0<br>1.5                                       | 4.5<br>2.5  | 7.0<br>4.5  | 5.0<br>2.5   | exet/            | 2-7  |
| t <sub>h</sub> o-s | Hold Time, HIGH or LOW<br>Pn to CP      | 3.3<br>5.0        | 1.5<br>0.5                                       | 0.5<br>1.5  | 2.0<br>2.5  | 0.5<br>(A/1.5 HE   | ns               | 2-   |
| t <sub>s</sub>     | Setup Time,<br>HIGH or LOW<br>CEP to CP | 3.3<br>5.0        | 7.5<br>4.5                                       | 10.5 2.0    | 13.5<br>9.0   | 12.5<br>8.0  | 19019<br>11 9 ns | 2-   |
| t <sub>h</sub>     | Hold Time, HIGH or LOW                  | 3.3<br>5.0        | 4.5<br>2.0                                       | 0.90 0.5    | 2.5 0.8   | 1.0 5T   | ns               | 2-   |
| t <sub>s</sub>     | Setup Time,<br>HIGH or LOW<br>CET to CP | 3.3<br>5.0        | 7.0<br>4.0                                       | 10.0<br>6.5 | 13.5<br>9.5   | 12.0<br>8.0  | ns               | 2-   |
| th                 | Hold Time, HIGH or LOW                  | 3.3<br>5.0        | 6.0  | 0.5         | 0.5   | 0 5T o   | ns               | 2-   |
| t <sub>s</sub>     | Setup Time,<br>HIGH or LOW<br>PE to CP  | 3.3<br>5.0        | 3.5  | 5.5         | 8.5<br>6.5  | 6.5<br>4.0   | ns               | 2-   |
| t <sub>h</sub>     | Hold Time, HIGH or LOW                  | 3.3<br>5.0        | 3.5<br>1.5                                       | 0.5         | 0.5<br>2.0  | 0<br>0.5   | ns               | 2-   |
| ts                 | Setup Time,<br>HIGH or LOW<br>U/D to CP | 3.3<br>5.0        | 7.0<br>4.5                                       | 10.0<br>6.5 | 13.0<br>9.0   | 11.5<br>7.5  | 6.8 ognsfi       | 2-   |
| t <sub>h</sub>     | Hold Time, HIGH or LOW U/D to CP        | 3.3<br>5.0        | 7.0<br>4.0                                       | 0<br>0.5    | 0.5<br>2.0  | 0<br>0.5   | ns               | 2-7  |
| t <sub>w</sub>     | CP Pulse Width,<br>HIGH or LOW          | 3.3<br>5.0        | 2.0  | 3.0         | 5.0<br>5.0  | 4.0  | ns               | 2-3  |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

|                  | TAACT                                       |                   | BAAC | 74ACT                  | 54ACT   | 74ACT  |        |       |
|------------------|---|-------------------|------|------------------------|---|--|--------|-------|
| Symbol           | Parameter of                                | V <sub>CC</sub> * | T/   | A = +25°C<br>L = 50 pF | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units  | Fig.  |
|                  | 00  | d Wichma          | Min  | Тур Мах                | Min Max   | Min Max  |        |       |
| f <sub>max</sub> | Maximum Clock<br>Frequency                  | 5.0               | 90   | 2.5                    | 0,8   | emit q<br>emit q<br>e VOJ vo H                               |        | el    |
| t <sub>PLH</sub> | Propagation Delay CP to Qn (PE HIGH or LOW) | 5.0               | 2.0  | 6.5 8.19.0             | 5.0   | 2.0 10.5   | ns     | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay CP to Qn (PE HIGH or LOW) | 5.0               | 2.0  | 6.5 0.79.0             | 6.0   | 2.0 10.5   | old ns | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay CP to TC                  | 5.0               | 3.0  | 9.0 11.5               | 0.8   | 3.0 14.0   | ns     | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay                           | 5.0               | 3.0  | 9.0 0.711.5            | 5.0   | 3.0 14.0   | ns     | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay CET to TC                 | 5.0               | 2.5  | 7.5 10.0               | 8.0   | 2.5  | ns     | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay CET to TC                 | 5.0               | 2.5  | 7.5 10.0               |   | 2.5 11.5   | ns     | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay                           | 5.0               | 2.5  | 8.0 10.5               | 0.6   | 2.5 12.0   | ns     | 2-3,4 |
| tPHL             | Propagation Delay U/D to TC                 | 5.0               | 2.5  | 8.0 10.5               | 6,0   | 2.5 12.0   | ns     | 2-3,4 |
| *Voltage R       | ange 5.0 is 5.0V ±0.5V                      |                   |      | 0.7                    | 5.0   | P Time.<br>H or LOW<br>to CP                                 |        | 81    |
|                  |   |                   |      |                        |   |  |        |       |
|                  |   |                   |      | 4.0                    |   |  |        |       |

| efinti |                                  |  |
|--------|----------------------------------|--|
|        |                                  |  |
|        | Power Dissipation<br>Capacitance |  |

| .01/1                   | Gt = 50 pF                              | (v) | O CL | = 50 pr         | 98 - | C <sub>L</sub> = 50 | pF      | C <sub>L</sub> = 50 pF            |                  | No.                         |
|-------------------------|---|-----|------|-----------------|------|---------------------|---------|-----------------------------------|------------------|-----------------------------|
|                         | yest nist                               | жей | Тур  | Guaranteed Mini |      |                     | d Minin | num                               |                  |                             |
| t <sub>s</sub>          | Setup Time, HIGH or LOW Pn to CP        | 5.0 |      | 2.5             |      | 09                  | 5.0     | ApolO mun<br>2.5 <sub>yonet</sub> | ixsM<br>per ns   | 2-7                         |
| thes                    | Hold Time, HIGH or LOW                  | 5.0 |      | 0.0 1.5         | 8.5  | 2.0                 | 5.0     | 1.5 nO                            | ns               | 2-7                         |
| t <sub>s</sub><br>4.8-9 | Setup Time,<br>HIGH or LOW<br>CEP to CP | 5.0 |      | 0.87.0          | d.8  | 2.0                 | 0.8     | rgation Delay<br>On 0.7           | 19019<br>13 cgns | 2-7                         |
| t <sub>h</sub><br>N.B-S | Hold Time, HIGH or LOW                  | 5.0 |      | 0 11.5          | 0.8  | 3.0                 | 5.0     | rgation Colay                     | ns               | 2-7                         |
| t <sub>s</sub>          | Setup Time, HIGH or LOW CET to CP       | 5.0 |      | 8.117.0         | 0.4  | 0.8                 | 0.8     | ysled noisegs<br>7.0 57           | qo19<br>o q ns   | 2-7                         |
| th                      | Hold Time, HIGH or LOW                  | 5.0 |      | 0.07            | 8.1  | 2.5                 | 0.8     | 0 57                              | ns               | 2-7                         |
| t <sub>s</sub>          | Setup Time,<br>HIGH or LOW<br>PE to CP  | 5.0 |      | 6.0             | 0.8  | 2.5<br>2.6          | 5.0     | 6.0<br>Yale L noilega             | ns<br>gora       | 2-7<br>HJ9                  |
| t <sub>h</sub>          | Hold Time, HIGH or LOW                  | 5.0 |      | 0.5             | 0.6  | 2.5                 | 0.8     | ve 0.5 noteps                     | go ns            | 2-7                         |
| ts                      | Setup Time,<br>HIGH or LOW<br>U/D to CP | 5.0 |      | 7.0             |      |                     |         | 7.0                               | 0.8 egra9<br>ns  | epatioV <sup>e</sup><br>2-7 |
| t <sub>h</sub>          | Hold Time, HIGH or LOW                  | 5.0 |      | 0.5             |      |                     |         | 0.5                               | ns               | 2-7                         |
| t <sub>w</sub>          | CP Pulse Width,<br>HIGH or LOW          | 5.0 |      | 4.0             |      |                     |         | 4.0                               | ns               | 2-3                         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 60.0 | pF    | V <sub>CC</sub> = 5.0V |



# 54AC/74AC174 • 54ACT/74ACT174 Hex D Flip-Flop with Master Reset

#### **General Description**

The 'AC/'ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

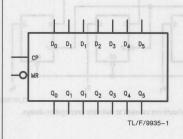
#### **Features**

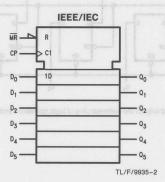
- Outputs source/sink 24 mA
- 'ACT174 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC174: 5962-87626
  - 'ACT174: 5962-87757

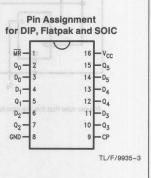
Ordering Code: See Section 8

**Logic Symbols** 

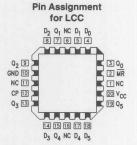
### **Connection Diagrams**







|   | Pin Names                      | Description        |
|---|--------------------------------|--------------------|
|   | D <sub>0</sub> -D <sub>5</sub> | Data Inputs        |
| 1 | CP                             | Clock Pulse Input  |
| ١ | MR                             | Master Reset Input |
|   | Q <sub>0</sub> -Q <sub>5</sub> | Outputs            |



TL/F/9935-4

#### **Functional Description**

The 'AC/'ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset (MR) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset (MR) will force all outputs LOW independent of Clock or Data inputs. The 'AC/ 'ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

# Truth Table

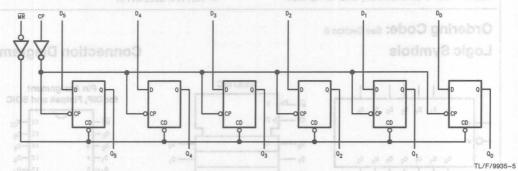
|       | Inputs        |         |           |  |  |  |
|-------|---------------|---------|-----------|--|--|--|
| MR    | CP            | D       | Q         |  |  |  |
| L     | X             | X       | Los a Jan |  |  |  |
| H     | 0 5           | J H     | H         |  |  |  |
| HA .C | Mary Jones H. | 5_a4103 | M wall    |  |  |  |
| Н     | STAR FRANCE   | X       | Q         |  |  |  |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- X = Immaterial

  = LOW-to-HIGH Transition

#### **Logic Diagram**

m 图You



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| DC Input Diode Current (I <sub>IK</sub> )   |                           | Guaranteed LI          | Input Voltag          | e (V <sub>I</sub> )    |                       | 0\                                     | / to V <sub>CC</sub> |
|---|---------------------------|------------------------|-----------------------|------------------------|-----------------------|--|----------------------|
| $V_1 = -0.5V$<br>$V_1 = V_{CC} + 0.5V$  |                           | -20 mA<br>+20 mA       | Output Volta          |                        |                       |  | / to V <sub>CC</sub> |
| DC Input Voltage (V <sub>I</sub> )  | -0.5V to                  |                        | Operating T           |                        | ire (T <sub>A</sub> ) | -40°C to                               | +85°C                |
| DC Output Diode Current (IOK)   |                           |                        | 54AC/AC               |                        |                       | medealuO -55°C to                      |                      |
| $V_{O} = -0.5V$<br>$V_{O} = V_{CC} + 0.5V$  |                           | -20 mA<br>+20 mA       | Minimum In            |                        | Rate (                | Supply Current (tΔ\VΔ                  |                      |
| DC Output Voltage (V <sub>O</sub> )   | -0.5V to to               | V <sub>CC</sub> + 0.5V | V <sub>IN</sub> from  | Spinster of the second | 0% of                 | VCC                                    |                      |
| DC Output Source  |                           | olve tight & 5.5V Voc  | V <sub>CC</sub> @ 3.3 | 3V, 4.5V,              | 5.5V                  | evinavag ste vo.e e pol 125            | mV/ns                |
| or Sink Current (IO)  |                           | ±50 mA                 |                       |                        | Rate (                | $\Delta V/\Delta t$ ) a Dras a DASS to |                      |
| DC V <sub>CC</sub> or Ground Current<br>per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) |                           | ± 50 mA                | 'ACT Dev              |                        | .0V                   |  |                      |
| Storage Temperature (T <sub>STG</sub> )   | -65°C                     | to +150°C              | V <sub>CC</sub> @ 4.5 | 5V, 5.5V               |                       | 125                                    | mV/ns                |
| Junction Temperature (T <sub>J</sub> ) CDIP PDIP  |                           | 175°C<br>140°C         |                       |                        |                       | Paramotor                              | lodmy                |
| Note 1: Absolute maximum ratings are to the device may occur. The databook s                  |                           |                        |                       |                        |                       |  |                      |
| exception, to ensure that the system destemperature, and output/input loading to              | sign is reliable over its | s power supply,        |                       |                        |                       |  |                      |

# DC Characteristics for 'AC Family Devices

|  | - = ruol v                           | 14                     | 74.                     | AC                   | 104   | 54AC                 |                  | 74AC   | a High Le         | V <sub>OH</sub> Minimun   |
|--|--------------------------------------|------------------------|-------------------------|----------------------|-------|----------------------|------------------|--|-------------------|---|
| Symbol                                   | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | -55   | T <sub>A</sub> =     | 125°C            | T <sub>A</sub> = -40°C to +85°C  | Units             | Conditions  |
| Am AS -                                  | Hol V                                | 78                     | Тур                     |                      | 3.70  | Guara                | nteed L          | imits  |                   |   |
| V <sub>IH</sub>                          | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 1.0   | 2.1<br>3.15<br>3.85  | 0.1              | 2.1<br>3.15<br>3.85  | egs#o             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                            |
| V <sub>IL</sub> V TO 1<br>AM AS<br>Am AS | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.50  | 0.9<br>1.35<br>1.65  |                  | 0.9<br>1.35<br>1.65  | ٧                 | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                            |
| V <sub>OH</sub>                          | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 0.f±  | 2.9                  | f,0 ±            | 2.9<br>4.4   | n Input<br>Ouvent | $I_{OUT} = -50 \mu\text{A}$                                       |
| Vt.s -                                   | coV = IV Am                          | 5.5                    | 5.49                    | 5.4                  | 0.1   | 5.4                  |                  | 5.4  | 1                 | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>             |
| xxM V38.                                 | = auoV Am                            | 3.0                    |                         | 2.56                 | 80    | 2.4                  |                  | The second secon | m Dynan           | -12 mA  |
| nlM Vas.)                                | = co+oV Am                           | 4.5<br>5.5             |                         | 3.86<br>4.86         | 08-   | 3.7<br>4.7           |                  | 3.76<br>4.76   | 1/Vmul            | l <sub>OH</sub> −24 mA<br>−24 mA                                  |
| V <sub>OL</sub>                          | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.001 | 0.1<br>0.1<br>0.1    | 0.0<br>reicnu su | 0.1<br>0.1<br>0.1  | Americal<br>V     | I <sub>OUT</sub> = 50 μA  |
|  |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 |       | 0.50<br>0.50<br>0.50 |                  | 0.44<br>0.44<br>0.44   | V                 | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA |
| I <sub>IN</sub>                          | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 |       | ±1.0                 |                  | ±1.0   | μΑ                | $V_{I} = V_{CC}$ , GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) and a mumix a Metable and A

|         |                                     |                     | 74               | AC           | 54AC                              | 74AC                            | qa epai<br>dt aiti | If Military/Aeros                        |
|---------|-------------------------------------|---------------------|------------------|--------------|-----------------------------------|---------------------------------|--------------------|--|
| Symbol  | VOS Parameter                       | V <sub>CC</sub> (V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units              | Conditions                               |
| to Vec  | VO                                  |                     | Тур              | gsitoV tuer  | Guaranteed Lin                    | nits                            | rent (lig          | DC Input Diode Cu                        |
| IOLD    | †Minimum Dynamic                    | 5.5                 | (oV) eg          | alloV tuettu | 50                                | 75                              | mA                 | V <sub>OLD</sub> = 1.65V Max             |
| IOHD    | Output Current                      | 5.5                 | anperatur<br>T   | parading I   | +50 + 00V                         | of Va.0 -75                     | mA                 | V <sub>OHD</sub> = 3.85V Min             |
| Icc ast | Maximum Quiescent<br>Supply Current | 5.5                 |                  | 8.0          | 160.0                             | 80.0                            | μА                 | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.
I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

### DC Characteristics for 'ACT Family Devices

|                      |                                      |                        | 744              | CT           | 54AC                        | rer + o                          | 74ACT                           | (4T) en                                  | Storage Temperatu  |
|----------------------|--------------------------------------|------------------------|------------------|--------------|-----------------------------|----------------------------------|---------------------------------|--|--|
| Symbol               | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to + |                                  | T <sub>A</sub> = -40°C to +85°C | Units                                    | Conditions   |
|                      |                                      |                        | Тур              |              | Guara                       | nteed L                          | imits                           | m resinge ar<br>De detaboer              | Note its Absolute maximum. In the device your accur.                   |
| V <sub>IH</sub>      | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   | 2.0<br>2.0                  | ower supp<br>s net reed<br>sens. | 2.0<br>2.0                      | nelays ent<br>InpoVescin<br>M circuits o | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                 |
| V <sub>IL</sub>      | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8                         | ylim                             | 0.8                             | olida                                    | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                 |
| V <sub>OH</sub>      | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                  | 9                                | 4.4<br>5.4                      | V  | $I_{OUT} = -50 \mu\text{A}$  |
| tilons               | PC Units Cond                        | 4.5<br>5.5             | orox —<br>eden   | 3.86<br>4.86 | 3.70<br>4.70                | U-65                             | 3.76<br>4.76                    | V  | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |
| VOL                  | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1   | ar.s 0.1                    | 3.15<br>3.15                     | 0.1                             | V  | $I_{OUT} = 50 \mu A$   |
|                      | V arVcc                              | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                |                                  | 0.44                            | Low Leve                                 | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $24 \text{ mA}$ $24 \text{ mA}$  |
| I <sub>IN</sub> oz – | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | 8.5 ±1.0                    | 2.9                              | 80.1 ± 2.89                     | μА                                       | $V_I = V_{CC}$ , GND   |
| ГССТ                 | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |              | 1.6                         | 5.4                              | 69.8 1.5                        | mA                                       | $V_I = V_{CC} - 2.1V$  |
| IOLD                 | †Minimum Dynamic                     | 5.5                    |                  |              | 50                          | 2,56                             | 750.8                           | mA                                       | V <sub>OLD</sub> = 1.65V Max   |
| IOHD                 | Output Current                       | 5.5                    |                  |              | -50                         | 98.8                             | -75                             | mA                                       | V <sub>OHD</sub> = 3.85V Min   |
| Icc                  | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 160.0                       | 0.1                              | 200.080.0 8                     | μΑ                                       | V <sub>IN</sub> = V <sub>CC</sub> or GND                               |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C.

# AC Electrical Characteristics: See Section 2 for waveforms and an analysis of publication of the section 2 for waveforms and an analysis of 2 for waveforms and 2 for wav

|                  | PARCT                         |                   | SAACT      | 74ACT                 | 74AC        | 54       | AC                      | 74         | AC                     |         |       |
|------------------|-------------------------------|-------------------|------------|-----------------------|-------------|----------|-------------------------|------------|------------------------|---------|-------|
| Symbol           | Parameter 6                   | V <sub>CC</sub> * |            | A = +25°<br>CL = 50 p |             | to +     | -55°C<br>125°C<br>50 pF | to +       | -40°C<br>85°C<br>50 pF | Units   | Fig.  |
|                  | tris                          | entail# b         | Min        | Тур                   | Max         | Min      | Max                     | Min        | Max                    |         |       |
| f <sub>max</sub> | Maximum Clock<br>Frequency    | 3.3<br>5.0        | 90<br>100  | 100<br>125            | 8.0         | 65<br>90 | VA                      | 70<br>100  | up Time, H             | MHz     | et    |
| t <sub>PLH</sub> | Propagation Delay             | 3.3<br>5.0        | 2.0        | 9.0<br>6.0            | 11.5<br>8.5 | 1.0      | 14.0<br>10.5            | 1.5        | 12.5<br>9.5            | loi-ins | 2-3,4 |
| tPHL             | Propagation Delay<br>CP to Qn | 3.3<br>5.0        | 2.0<br>1.5 | 8.5<br>6.0            | 11.0        | 1.0      | 13.0<br>10.0            | 1.5        | 12.0<br>9.0            | ns      | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay MR to Qn    | 3.3<br>5.0        | 2.5<br>1.5 | 9.0<br>7.0            | 11.5<br>9.0 | 1.0      | 13.5<br>11.0            | 2.0<br>1.5 | 12.5<br>10.5           | ns      | 2-3,4 |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

# AC Operating Requirements: See Section 2 for waveforms

|                  | Conditions                                      |                   | atlett 74  | AC              | 54AC  | 74AC   | Indmy |       |
|------------------|---|-------------------|------------|-----------------|---|--|-------|-------|
| Symbol           | Parameter Vo.a = 00V                            | V <sub>CC</sub> * |            | + 25°C<br>50 pF | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig.  |
|                  | 753 00  |                   | Тур        |                 | Guaranteed Min  | imum   |       |       |
| t <sub>s</sub>   | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 3.3<br>5.0        | 2.5<br>2.0 | 6.5<br>5.0      | 7.5<br>5.5  | 7.0<br>5.5   | ns    | 2-7   |
| t <sub>h</sub>   | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 3.3<br>5.0        | 1.0<br>0.5 | 3.0<br>3.0      | 3.0<br>3.0  | 3.0<br>3.0   | ns    | 2-7   |
| t <sub>w</sub>   | MR Pulse Width, LOW                             | 3.3<br>5.0        | 1.0<br>1.0 | 5.5<br>5.0      | 7.0<br>5.0  | 7.0<br>5.0   | ns    | 2-3   |
| t <sub>w</sub>   | CP Pulse Width                                  | 3.3<br>5.0        | 1.0<br>1.0 | 5.5<br>5.0      | 7.0<br>5.0  | 7.0<br>5.0   | ns    | 2-3   |
| t <sub>rec</sub> | Recovery Time<br>MR to CP                       | 3.3<br>5.0        | 0          | 2.5<br>2.0      | 3.0<br>2.0  | 2.5<br>2.0   | ns    | 2-3,7 |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

# AC Electrical Characteristics: See Section 2 for waveforms

|                  |   |                   |     | 74ACT                 |      | 54/  | ACT                     | 74/  | ACT                    |       |             |
|------------------|---|-------------------|-----|-----------------------|------|------|-------------------------|------|------------------------|-------|-------------|
| Symbol           | Parameter                                 | V <sub>CC</sub> * |     | C <sub>L</sub> = +25° |      | to + | −55°C<br>125°C<br>50 pF | to + | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                  |   |                   | Min | Тур                   | Max  | Min  | Max                     | Min  | Max                    |       |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency                | 5.0               | 165 | 200                   |      | 95   |                         | 140  |                        | MHz   |             |
| t <sub>PLH</sub> | Propagation Delay<br>CP to Q <sub>n</sub> | 5.0               | 1.5 | 7.0                   | 10.5 | 1.0  | 12.5                    | 1.5  | 11.5                   | ns    | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay<br>CP to Q <sub>n</sub> | 5.0               | 1.5 | 7.0                   | 10.5 | 1.0  | 13.0                    | 1.5  | 11.5                   | ns    | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay MR to Qn                | 5.0               | 1.5 | 6.5                   | 9.5  | 1.0  | 12.0                    | 1.5  | 11.0                   | ns    | 2-3,4       |

\*Voltage Range 5.0 is 5.0V ±0.5V

| 1000              | OpF   CL = 50 pF                                | (A)   | CL = | ou pr | C <sub>L</sub> = 50 pF | C <sub>L</sub> = 50 pF |       | NO.   |
|-------------------|---|-------|------|-------|------------------------|------------------------|-------|-------|
|                   | Max Min Max                                     | nitte | Тур  | Typ   | Guaranteed Min         | imum                   |       |       |
| ts                | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0   | 0.5  | 1.5   | 00 8.8                 | num Clock<br>ency 5.1  | ns ns | 2-7   |
| t <sub>h</sub> ss | Hold Time, HIGH or LOW                          | 5.0   | 1.0  | 2.0   | 8.2.0                  | 2.0 no.                | ns    | 2-7   |
| tw                | MR Pulse Width, LOW                             | 5.0   | 1.5  | 3.0   | 5.0                    | 3.5                    | ns    | 2-3   |
| t <sub>w</sub>    | CP Pulse Width, HIGH OR LOW                     | 5.0   | 1.5  | 3.0   | 5.0                    | 3.5                    | ns    | 2-3   |
| t <sub>rec</sub>  | Recovery Time MR to CP                          | 5.0   | -1.0 | 0.5   | 1.0                    | 0.5                    | ns    | 2-3,7 |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| S     | symbol | Param                   | eter     | Тур  | Units |      | Conditions             |     |  |
|-------|--------|-------------------------|----------|------|-------|------|------------------------|-----|--|
| pli C | N.     | Input Capa              | acitance | 4.5  | pF    | *35W | $V_{CC} = 5.0V$        | 169 |  |
| OM C  | PD     | Power Diss<br>Capacitan |          | 85.0 | pF    | (1/) | V <sub>CC</sub> = 5.0V |     |  |
|       |        |                         |          |      |       |      |                        |     |  |
|       |        |                         |          |      |       |      |                        |     |  |
|       |        |                         |          |      |       |      |                        |     |  |
|       |        |                         |          |      |       |      |                        |     |  |
|       |        |                         |          |      |       |      |                        |     |  |

#### AC Electrical Characteristics: See Section 2 for waveforms

| Fig.<br>No. |      |     |  |  |  |  |                   |  |
|-------------|------|-----|--|--|--|--|-------------------|--|
|             |      |     |  |  |  |  |                   |  |
|             |      |     |  |  |  |  |                   |  |
|             |      |     |  |  |  |  |                   |  |
|             | 11.5 | 1.5 |  |  |  |  |                   |  |
|             |      |     |  |  |  |  | Propagation Delay |  |

# 54AC/74AC175 • 54ACT/74ACT175 Quad D Flip-Flop

#### **General Description**

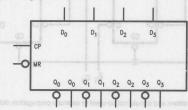
The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

#### **Features**

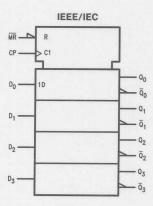
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Asynchronous common reset Asynchronous common reset
- True and complement output
- Outputs source/sink 24 mA
- 'ACT175 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC175: 5962-89552
  - 'ACT175: 5962-89693

Ordering Code: See Section 8

**Logic Symbols** 



TL/F/9936-1



TL/F/9936-2

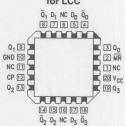
# **Connection Diagrams**

Pin Assignment for DIP, Flatpak and SOIC



TL/F/9936-3

Pin Assignment for LCC



TL/F/9936-4

| Pin Names                         | Description        |
|-----------------------------------|--------------------|
| D <sub>0</sub> -D <sub>3</sub>    | Data Inputs        |
| CP                                | Clock Pulse Input  |
| MR                                | Master Reset Input |
| Q <sub>0</sub> -Q <sub>3</sub>    | True Outputs       |
| $\overline{Q}_0 - \overline{Q}_3$ | Complement Outputs |

#### **Functional Description**

The 'AC/'ACT175 consists of four edge-triggered D flipflops with individual D inputs and Q and  $\overline{\mathbb{Q}}$  outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and  $\overline{\mathbb{Q}}$  outputs to follow. A LOW input on the Master Reset ( $\overline{\mathbb{MR}}$ ) will force all Q outputs LOW and  $\overline{\mathbb{Q}}$  outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

# Truth Table

| Inputs                    | Out                | Outputs          |  |  |  |  |
|---------------------------|--------------------|------------------|--|--|--|--|
| @ t <sub>n</sub> , MR = H | @ t <sub>n+1</sub> |                  |  |  |  |  |
| D <sub>n</sub>            | Qn                 | $\overline{Q}_n$ |  |  |  |  |
| L                         | Leves are          | Н                |  |  |  |  |
| H GGI                     | T-CH U             | DELL             |  |  |  |  |

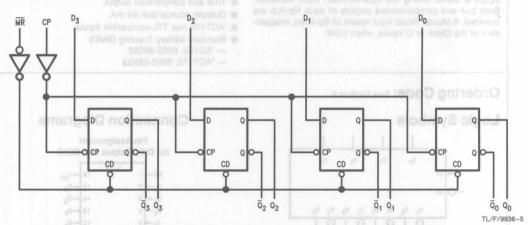
vice is useful for general flip-flop requirements where clock

H = HIGH Voltage Level

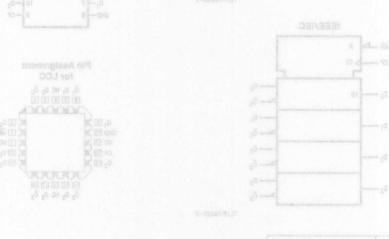
L = LOW Voltage Level

 $t_n = \mbox{Bit Time before Clock Pulse}$   $t_{n+1} = \mbox{Bit Time after Clock Pulse}$ 

#### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ ) -0.5V to +7.0VDC Input Diode Current ( $I_{IK}$ )  $V_I = -0.5V$  -20 mA  $V_I = V_{CC} + 0.5V$  +20 mA

DC Input Voltage ( $V_I$ ) -0.5V to  $V_{CC} + 0.5V$ 

DC Input Voltage (V<sub>I</sub>)  $\sim$  0.5V to V<sub>C</sub> DC Output Diode Current (I<sub>OK</sub>)  $\sim$  0.5V  $\sim$  0.08

 $V_{O} = V_{CC} + 0.5V$  + 20 mA DC Output Voltage ( $V_{O}$ ) - 0.5V to to  $V_{CC} + 0.5V$ 

DC Output Source or Sink Current (I<sub>O</sub>) DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>)  $\pm 50 \text{ mA}$ Storage Temperature (T<sub>STG</sub>)  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Junction Temperature (T<sub>J</sub>)

CDIP

PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating

Conditions
Supply Voltage (V<sub>CC</sub>)

'AC
'ACT

Input Voltage (V<sub>I</sub>)

Output Voltage (V<sub>O</sub>)

Operating Temperature (T<sub>A</sub>)

74AC/ACT

54AC/ACT

-55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices
V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>
V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices V<sub>IN</sub> from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

### **DC Characteristics for 'AC Family Devices**

| 0.1V                        | - 00 V CC -                          | 8.1               | 74                      | AC                   | 8.0   | 54AC                 | 6.8       | 74AC                            | egen               | oV Jugal Vo   |
|-----------------------------|--------------------------------------|-------------------|-------------------------|----------------------|-------|----------------------|-----------|---------------------------------|--------------------|---|
| Symbol Symbol               | Parameter                            | V <sub>CC</sub>   | T <sub>A</sub> =        | + 25°C               | -55   | T <sub>A</sub> =     | 125°C     | T <sub>A</sub> = -40°C to +85°C | Units              | Conditions  |
|                             | $A = NI A_{e}$                       | 65                | Тур                     |                      | nr o  | Guara                | nteed L   | imits                           |                    |   |
| -24 HIV                     | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 4.70  | 2.1<br>3.15<br>3.85  | 4.86      | 2.1<br>3.15<br>3.85             | n Low Le           | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |
| V <sub>IL</sub><br>HiV 10 J | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.50  | 0.9<br>1.35<br>1.65  | 0.36      | 0.9<br>1.35<br>1.65             | ٧                  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| VOH                         | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 0.f±  | 2.9<br>4.4<br>5.4    | 1.0±      | 2.9<br>4.4<br>5.4               | n logut<br>Current | $I_{OUT} = -50 \mu\text{A}$   |
| - 2.1V                      | ooV = IV Am                          | 3.0               |                         | 2.56                 | 1.6   | 2.4                  |           | 9.0 a.a<br>2.46                 | 11                 | $V_{IN} = V_{IL} \text{ or } V_{IH}$<br>- 12 mA   |
| .65V Max                    | mA V <sub>OLD</sub> = 1              | 4.5<br>5.5        |                         | 3.86<br>4.86         | 50    | 3.7<br>4.7           |           | 3.76<br>4.76                    | m LVnam<br>Jurrent | I <sub>OH</sub> -24 mA -24 mA   |
| Vol                         | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 160.0 | 0.1<br>0.1<br>0.1    | 0.8       | 0.1<br>0.1<br>0.1               |                    | I <sub>OUT</sub> = 50 μA  |
|                             |                                      | 3.0<br>4.5<br>5.5 |                         | 0.36<br>0.36<br>0.36 |       | 0.50<br>0.50<br>0.50 | 0.5000.00 | 0,44<br>0.44<br>0.44            | 25°C is idi.<br>V  | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}O_L$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ |
| I <sub>IN</sub>             | Maximum Input<br>Leakage Current     | 5.5               |                         | ±0.1                 |       | ±1.0                 |           | ±1.0                            | μΑ                 | $V_I = V_{CC}$ , GND  |

-20 mA

±50 mA

175°C

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued) and an amunical Action of the Continued of the Continu

|           |                                     |                     | 74               | AC                   | 54AC                              | 74AC                            | tire bis | please contact               |  |
|-----------|-------------------------------------|---------------------|------------------|----------------------|-----------------------------------|---------------------------------|----------|------------------------------|--|
| Symbol    | VO.S Parameter                      | V <sub>CC</sub> (V) | T <sub>A</sub> = | + 25°C               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units    | Conditions                   |  |
| DOV of VO |                                     |                     | Тур              | gatioV tugr          | Guaranteed Li                     | mits                            | gi) Inen | DC Input Blode Cu            |  |
| IOLD      | †Minimum Dynamic                    | 5.5                 | (gV) egi         | itteV tughs          | 50 05 +                           | 75                              | mA       | V <sub>OLD</sub> = 1.65V Max |  |
| IOHD      | Output Current                      | 5.5                 | ilus iegme<br>T  | peravag i<br>ZAAG/AC | -50 + 50V                         | of Va.0 -75                     | mA       | V <sub>OHD</sub> = 3.85V Min |  |
| 128 501   | Maximum Quiescent<br>Supply Current | 5.5                 | T<br>put Edge I  | 8.0                  | 160.0                             | 80.0                            | μΑ       | $V_{IN} = V_{CC}$ or GND     |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# **DC Characteristics for 'ACT Family Devices**

|                     |  |                        | 744              | CT           | 54ACT                       | MT A    | 74ACT                           | (LT) en                    | Junction Temperate<br>CDIP   |  |
|---------------------|--|------------------------|------------------|--------------|-----------------------------|---------|---------------------------------|----------------------------|--|--|
| Symbol              | Parameter  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to + |         | T <sub>A</sub> = -40°C to +85°C | Units                      | Conditions   |  |
|                     |  |                        | Тур              |              | Guarar                      | nteed L | imits                           | adetab eri?<br>modeya ari: | to the device may occur. I'tl<br>exception, to ensure that th                  |  |
| V <sub>IH</sub>     | Minimum High Level Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   | 2.0<br>2.0                  |         | 2.0<br>2.0                      | input load<br>to Vuits     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>     | Maximum Low Level Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8                         | ylim    | 0.8<br>0.8                      | V                          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| Voh                 | Minimum High Level Output Voltage  | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                  | 25°C    | 4.4<br>5.4                      | V                          | I <sub>OUT</sub> = -50 μA  |  |
|                     | = тиоУ   | 4.5<br>5.5             | elim             | 3.86<br>4.86 | 3.70<br>4.70                | 1.5     | 3.76<br>4.76                    | ve.J <b>V</b> igit         | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$        |  |
| V <sub>OL</sub>     | Maximum Low Level Output Voltage   | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1   | 0.1<br>0.1                  | 38.8    | 0.1<br>0.1                      | ٧                          | I <sub>OUT</sub> = 50 μA   |  |
| 0.1V<br>- 0.1V      | and the second of the second o | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                | 1.35    | 0.44<br>0.44                    | Sge<br>Low Let             | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$ |  |
| I <sub>IN</sub>     | Maximum Input<br>Leakage Current   | 5.5                    |                  | ±0.1         | NA ±1.0                     | 4.4     | 9A.A ± 1.0 4                    | μА                         | $V_{I} = V_{CC}$ , GND   |  |
| ICCT                | Maximum<br>I <sub>CC</sub> /Input  | 5.5                    | 0.6              |              | 1.6                         | 25.5    | 1.5                             | mA                         | $V_{\rm I} = V_{\rm CC} - 2.1V$  |  |
| I <sub>OLD</sub> 9- | †Minimum Dynamic   | 5.5                    |                  |              | 7.8 50                      | 3.86    | 758.4                           | mA                         | V <sub>OLD</sub> = 1.65V Max   |  |
| Iонр                | Output Current   | 5.5                    |                  |              | -50                         | 4.86    | -75                             | mA                         | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc An Od           | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 1.0                         | 0.1     | 200.0 0.8 le                    | μA                         | V <sub>IN</sub> = V <sub>CC</sub> or GND                                       |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| Symbol           | Parameter   | V <sub>CC</sub> * | 125°C      | T <sub>A</sub> = +2<br>C <sub>L</sub> = 50 |                 | to-            | + 125°C<br>= 50 pF | 1000       | +85°C<br>= 50 pF | Units | Fig.<br>No.       |
|------------------|---|-------------------|------------|--|-----------------|----------------|--------------------|------------|------------------|-------|-------------------|
|                  | xeM rr  | NI.               | Min        | Тур  | Max             | Min            | Max                | Min        | Max              |       |                   |
| f <sub>max</sub> | Maximum Clock<br>Frequency                            | 3.3<br>5.0        | 149<br>187 | 214<br>244                                 |                 | 95<br>95       | 178                | 139<br>187 | mum Clock        | MHz   | *esm <sup>†</sup> |
| t <sub>PLH</sub> | Propagation Delay CP to $Q_n$ or $\overline{Q}_n$     | 3.3<br>5.0        | 2.0        | 9.5  | 12.0            | 1.0            | 15.0<br>11.5       | 2.0        | 13.5<br>9.5      | ns    | 2-3,4             |
| t <sub>PHL</sub> | Propagation Delay CP to $Q_n$ or $\overline{Q}_n$     | 3.3<br>5.0        | 2.5        | 8.5<br>6.0                                 | 13.0            | 1.0            | 14.5<br>10.5       | 2.0        | 14.5<br>10.5     | ns    | 2-3,4             |
| t <sub>PLH</sub> | Propagation Delay                                     | 3.3<br>5.0        | 3.0        | 7.5<br>5.5                                 | 12.5<br>8.0 9.0 | 1.0            | 13.5<br>10.5       | 2.5        | 13.5<br>10.0     | ns    | 2-3,4             |
| t <sub>PHL</sub> | Propagation Delay $\overline{MR}$ to $\overline{Q}_n$ | 3.3<br>5.0        | 3.0<br>2.0 | 8.5<br>6.0                                 | 11.0<br>8.5     | 1.0<br>a a 1.0 | 15.0<br>11.0       | 2.5        | 12.5<br>9.0      | ns    | 2-3,4             |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

# AC Operating Requirements: See Section 2 for waveforms and particular and particu

|                  | ZAACT                            | TOANS                 | 74   | AC             | 54AC  | 74AC   |        |             |
|------------------|----------------------------------|-----------------------|--|----------------|---|--|--------|-------------|
| Symbol           | Parameter                        | V <sub>CC</sub> * (V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |                | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units  | Fig.<br>No. |
|                  | equesio(8                        | l beemsted            | Тур  | Guaranteed Min |   | imum   |        |             |
| t <sub>s</sub>   | Setup Time, HIGH or LOW Dn to CP | 3.3<br>5.0            | 2.0  | 4.5<br>3.0     | 5.0<br>3.5  | 4.5<br>3.0   | ns     | 2-7         |
| t <sub>h</sub>   | Hold Time, HIGH or LOW           | 3.3<br>5.0            | 1.0  | 1.0            | 2.0   | 1.0  | olo ns | 2-7         |
| t <sub>w</sub>   | CP Pulse Width<br>HIGH or LOW    | 3.3<br>5.0            | 2.5<br>2.0                                       | 4.5<br>3.5     | 6.0<br>5.0  | 4.5<br>3.5   | ns     | 2-3         |
| tw               | MR Pulse Width, LOW              | 3.3<br>5.0            | 2.5  | 4.5<br>3.5     | 5.5<br>5.0  | 5.0<br>3.5   | ns     | 2-3         |
| t <sub>rec</sub> | Recovery Time<br>MR to CP        | 3.3<br>5.0            | -2.0<br>-1.0                                     | 0              | 1.5<br>1.5  | of RM (omit year<br>one was                                  | ns     | 2-3,7       |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

# AC Electrical Characteristics: See Section 2 for waveforms 2018 19 19 19 19 19 19 20

|                  | THAC  |                   | DAR  | 74ACT  |         | AAT 5   | 4ACT            | 74/  | ACT  |       |       |
|------------------|---|-------------------|--|--------|---------|---|-----------------|--|------|-------|-------|
| Symbol           | Parameter of                                      | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |        |         | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |                 | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.  |
|                  | xsM n   | 14                | Min  | Тур    | Max     | Min   | Max             | Min  | Max  |       |       |
| f <sub>max</sub> | Maximum Clock<br>Frequency                        | 5.0               | 175  | 20 236 |         | 95  | 187             | 145  |      | MHz   | xem?  |
| t <sub>PLH</sub> | Propagation Delay                                 | 5.0               | 2.0  | 0.6.0  | 0.81    | 0.7 1.0   | 0.S<br>a. (11.5 | 1.5  | 11.0 | 19 ns | 2-3,4 |
| tpHL             | Propagation Delay CP to $Q_n$ or $\overline{Q}_n$ | 5.0               | 2.0  | 7.0    | 3.811.0 | 0.8 1.0   | 8.112.5         | 1,5  | 12.0 | ns    | 2-3,4 |
| tpLH             | Propagation Delay                                 | 5.0               | 2.0  | 6.0    | 0.8 9.5 | 3.6 1.0   | 0.211.5         | 1.5  | 10.5 | ns    | 2-3,4 |
| tpHL             | Propagation Delay MR to Qn                        | 5.0               | 2.0  | 5.5    | 3.8 9.5 | 1.0   | 0.911.0         | 1.5  | 10.5 | ns    | 2-3,4 |

\*Voltage Range 5.0 is 5.0V ±0.5V

# AC Operating Requirements: See Section 2 for waveforms 3811941941 upon graits 1990 OA

|  |                           | ZAAC                    |                   | 74A  | CT         | 54ACT   | 74ACT  |                |             |
|--|---------------------------|-------------------------|-------------------|--|------------|---|--|----------------|-------------|
| Symbol                                   | Parameter                 |                         | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 \text{ pF}$ | Units          | Fig.<br>No. |
|  | mominiki                  |                         | seamens E         | Typ Guaranteed Mini                              |            |   | imum   |                |             |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | 1993                      | p Time 3.5<br>c CP      | 0.8<br>35.0       | 3.0<br>3.0                                       | 2.0<br>2.5 | 3.5<br>3.5  | 2.0<br>2.5   | nuta2<br>of ns | 2-7         |
| th                                       | Hold<br>D <sub>n</sub> to | Time, HIGH or LOW       | 5.0               | 1.0 0  | 1.0        | 1.5   | Turne, HIGH or LO  | of ns          | 2-7         |
| t <sub>w</sub>                           | 1                         | Pulse Width<br>H or LOW | 5.0               | 4.0  | 3.0        | 5.0   | 3.5/01/10  | 10 ns          | 2-3         |
| tw                                       | ™R                        | Pulse Width, LOW        | 5.0               | 4.0  | 3.0        | 5.0   | 4.0  | ns             | 2-3         |
| t <sub>rec</sub>                         | Rec                       | overy Time, MR to CP    | 5.0               | 0 0  | 0          | 1.5   | 0  | ns             | 2-3,7       |

\*Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions      |
|-----------------|----------------------------------|------|-------|-----------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 45.0 | pF    | $V_{CC} = 5.0V$ |



# 54AC/74AC191 Up/Down Counter with Preset and Ripple Clock

#### **General Description**

The 'AC191 is a reversible modulo 16 binary counter. It features synchronous counting and asynchronous presetting. The preset feature allows the 'AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

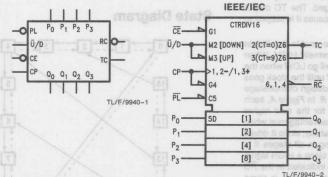
#### **Features**

- High speed—133 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable batalini ena segnado etala lametni ,WO.I
- Outputs source/sink 24 mA

Ordering Code: See Section 8

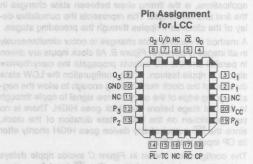
**Logic Symbols** 

#### wood travel and the Connection Diagrams



|      |            | /  |                  |
|------|------------|----|------------------|
| P1-  | 10 0000 T  | 16 | -V <sub>CC</sub> |
| Q1-  | 2          | 15 | -Po              |
| Q0-  | The WOJ    | 14 | — CP             |
| CE-  | 4 nutset a | 13 | - RC             |
| Ū/D- | 5 botso    | 12 | -TC              |
| Q2-  | 6 88 098   | 11 | -PL              |
| Q3-  | 7          | 10 | -P <sub>2</sub>  |
| GND- | 8          | 9  | -P <sub>3</sub>  |

| Pin Names                      | Description                      |
|--------------------------------|----------------------------------|
| CE                             | Count Enable Input               |
| CP                             | Clock Pulse Input                |
| P <sub>0</sub> -P <sub>3</sub> | Parallel Data Inputs             |
| PL                             | Asynchronous Parallel Load Input |
| Ū/D                            | Up/Down Count Control Input      |
| Q <sub>0</sub> -Q <sub>3</sub> | Flip-Flop Outputs                |
| RC                             | Ripple Clock Output              |
| TC                             | Terminal Count Output            |



TL/F/9940-4

#### **Functional Description**

The 'AC191 is a synchronous up/down counter. The 'AC191 is organized as a 4-bit binary counter. It contains four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ( $\overline{\text{PL}}$ ) input is LOW, information present on the Parallel Load inputs ( $P_0-P_3$ ) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the  $\overline{\text{CE}}$  input inhibits counting. When  $\overline{\text{CE}}$  is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the  $\overline{\text{U}}/\text{D}$  input signal, as indicated in the Mode Select Table.  $\overline{\text{CE}}$  and  $\overline{\text{U}}/\text{D}$  can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 15 in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until  $\overline{\rm U}/{\rm D}$  is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (RC) output. The RC output is normally HIGH. When CE is LOW and TC is HIGH, RC output wil go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each RC output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on CE inhibits the RC output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure B. All clock inputs are driven in parallel and the  $\overline{\rm RC}$  outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the  $\overline{\rm RC}$  output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure C avoids ripple delays and their associated restrictions. The  $\overline{\text{CE}}$  input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures A and B doesn't apply, because the TC output of a given stage is not affected by its own  $\overline{\text{CE}}$ .

#### Mode Select Table

|    | In    | puts | Mode |                  |  |
|----|-------|------|------|------------------|--|
| PL | CE    | Ū/D  | СР   | MOGE             |  |
| Н  | L     | E    | 1    | Count Up         |  |
| Н  | ist T | BHEE | 5    | Count Down       |  |
| L  | X     | X    | X    | Preset (Asyn.)   |  |
| Н  | Н     | X    | X    | No Change (Hold) |  |

#### **RC** Truth Table

|         | beau ed of 191 Inputs swota eurise t |           |           |           |  |  |  |
|---------|--------------------------------------|-----------|-----------|-----------|--|--|--|
| PL      | CE                                   | TC*       | СР        | RC        |  |  |  |
| und abi | delitten gn                          | InemHamil | 0.8505.00 | 10 As-T-  |  |  |  |
| Н       | H                                    | X         | X         | H CONTROL |  |  |  |
| Н       | X                                    | L         | X         | Н         |  |  |  |
| L       | X                                    | X         | X         | Н         |  |  |  |

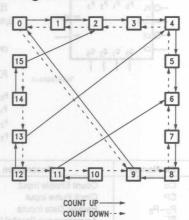
\*TC is generated internally H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Transition

#### **State Diagram**



TL/F/9940-5

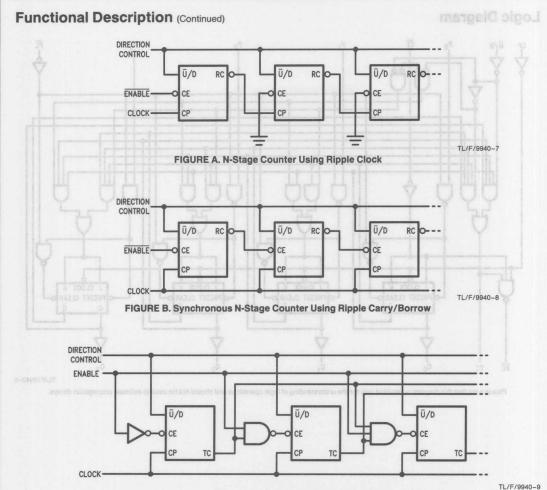
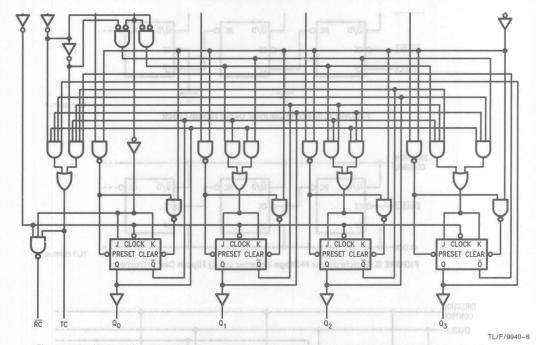


FIGURE C. Synchronous N-Stage Counter with Parallel Gated Carry/Borrow



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>) DC Input Diode Current (I<sub>IK</sub>)

-20 mA

±50 mA

 $V_1 = -0.5V$  $V_1 = V_{CC} + 0.5V$ DC Input Voltage (V<sub>I</sub>)

+20 mA -0.5V to V<sub>CC</sub> + 0.5V

-0.5V to to V<sub>CC</sub> + 0.5V

-65°C to +150°C

175°C 0°887 - 01 140°C

DC Output Diode Current (IOK)

-20 mA  $V_0 = -0.5V$  $V_O = V_{CC} + 0.5V$ + 20 mA

DC Output Voltage (VO) DC Output Source

or Sink Current (IO)

DC V<sub>CC</sub> or Ground Current per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>)

Storage Temperature (TSTG) Junction Temperature (T<sub>J</sub>)

CDIP CDIP DOBA - AT

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating Conditions

Supply Voltage (VCC) Input Voltage (V<sub>I</sub>)

2.0V to 6.0V OV to VCC OV to VCC

Output Voltage (VO) Operating Temperature (T<sub>A</sub>)

74AC/ACT -40°C to +85°C -55°C to +125°C 54AC/ACT

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices Medical Medical Management

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt) - 0.5 sources real manuscript 'ACT Devices of seed and of beetlessand one VO.S is got bits and safety

VIN from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V AC Electrical Characteristics: see section 2 to Am 02 to a

## DC Characteristics for 'AC Family Devices

|                 | 0.51 6.                              |                          | 74                   | AC                     | 0.11        | 54AC                             | C.I        | 74AC                            | -        | ni<br>-Caralita | Propag                                |   |
|-----------------|--------------------------------------|--------------------------|----------------------|------------------------|-------------|----------------------------------|------------|---------------------------------|----------|-----------------|---------------------------------------|---|
| Symbol          | Parameter                            | arameter V <sub>CC</sub> |                      | T <sub>A</sub> = +25°C |             | T <sub>A</sub> = -55°C to +125°C |            | T <sub>A</sub> = -40°C to +85°C |          | Units           | Conditions                            |   |
| 2-3,4           | an 14.0                              | r l                      | Тур                  | 0.1                    | 12.0        | Guaranteed Lin                   | mits       | 5.0                             |          | 2               | CPtol                                 | HJSk  |
| VIH             | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5        | 2.25<br>2.75         | 2.1<br>3.15<br>3.85    | 17.8        | 2.1<br>3.15<br>3.85              | 4.0<br>2.5 | 2.1<br>3.15<br>3.85             | Am       | ation De<br>G V | V <sub>OUT</sub> or V <sub>CC</sub>   | = 0.1V<br>- 0.1V                            |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5        | 1.5<br>2.25<br>2.75  | 0.9<br>1.35<br>1.65    | 9.5         | 0.9<br>1.35<br>1.65              | 2.0        | 0.9<br>1.35<br>1.65             | yes      | o Volta         | V <sub>OUT</sub> = or V <sub>CC</sub> | = 0.1V<br>- 0.1V                            |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5        | 2,99<br>4.49<br>5.49 | 2.9<br>4.4<br>5.4      | 12.0        | 2.9<br>4.4<br>5.4                | 2.5        | 2.9<br>4.4<br>5.4               | ki       | ation De        | l <sub>OUT</sub> =                    | -50 μΑ                                      |
|                 | 5 12.5 ns                            | 0.0                      | 8.8                  | 0.1                    | 0.8         | 5.0                              | 8.1        | 5.0                             | yn)      | aG mails        | *V <sub>IN</sub> =                    | V <sub>IL</sub> or V <sub>IH</sub>          |
|                 | 0 14.5 ns                            | 3.0<br>4.5<br>5.5        | 14.5                 | 2.56<br>3.86<br>4.86   | 12.5        | 2.4<br>3.7<br>4.7                | 2.5        | 2.46<br>3.76<br>4.76            | lay      | ation De<br>No. | Гон                                   | -12 mA<br>-24 mA<br>-24 mA                  |
| V <sub>OL</sub> | Maximum Low Level                    | 3.0                      | 0.002                | 0.1                    | 8.5         | 0.1                              | 1.8        | 0.1                             | - EVI    | TO              | I <sub>OUT</sub> =                    | 50 μΑ                                       |
|                 | Output Voltage                       | 4.5<br>5.5               | 0.001<br>0.001       | 0.1                    | 8.11<br>8.8 | 0.1<br>0.1                       | 2.0        | 0.1                             | yel      | ation De        | Propag<br>U/D to                      | Hidy  |
|                 | 6 12.6 ns                            | 3.0                      | 13.5                 | 0.36                   | 11.0        | 0.50                             | 2.0        | 0.44                            | lay      | 01              | of GNU                                | V <sub>IL</sub> or V <sub>IH</sub><br>12 mA |
| 2-3,6           | 0 15.5 ns                            | 4.5<br>5.5               | 16.5                 | 0.36                   | 8.81        | 0.50<br>0.50                     | 2.5        | 0.44                            | VS!      | ed notin        | loL                                   | 24 mA<br>24 mA                              |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                      |                      | ±0.1                   |             | ±1.0                             |            | ±1.0                            | VI<br>VI | μА              | V <sub>I</sub> = V <sub>I</sub>       | CC, GND                                     |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued) and a mumix of studeed A

|           |                                     |                        | 74                     | AC            | 54AC                              | 74AC                            | ace spe<br>the Na        | please contact                           |  |
|-----------|-------------------------------------|------------------------|------------------------|---------------|-----------------------------------|---------------------------------|--------------------------|--|--|
| Symbol Vo | / Parameter                         | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                    | Conditions                               |  |
| DOV of VO |                                     | (AT) m                 | Тур                    | Typ Guarantee |                                   | mits                            | iner (I <sub>III</sub> ) | DC Input Diode Ou                        |  |
| IOLD      | †Minimum Dynamic                    | 5.5                    |                        | PARCIAC       | 50 03 4                           | 75                              | mA                       | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD      | Output Current                      | 5.5                    | noisti is              | OANGAR        | -50 + 50                          | / of V8.0-75                    | mA (                     | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc       | Maximum Quiescent<br>Supply Current | 5.5                    | 18<br>0% to 7          | 8.0           | 160.0                             | 80.0                            | μΑ                       | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

#### AC Electrical Characteristics: See Section 2 for waveforms

|                          |   |                       |  | 74AC        |              | 54  | AC                                | 74  | AC                             | manua T an                 | Junet                |
|--------------------------|---|-----------------------|--|-------------|--------------|---|-----------------------------------|---|--------------------------------|----------------------------|----------------------|
| Symbol                   | Parameter   | V <sub>CC</sub> * (V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             |              | $T_A = -55^{\circ}C$ to $+125^{\circ}C$ $C_L = 50 \text{ pF}$ |                                   | $T_{A} = -40^{\circ}C$ to +85°C $C_{L} = 50 \text{ pF}$ |                                | Units                      | Fig.<br>No.          |
|                          |   |                       | Min  | Тур         | Max          | Min   | Max                               | Min   | Max                            | emce may b<br>on, to cosum | b stit of<br>ligeoxe |
| f <sub>max</sub>         | Maximum Count<br>Frequency                            | 3.3<br>5.0            | 70<br>90   | 105<br>133  | bne          | 55<br>80  | lational does<br>is specification | 0.0   | Virgud foadin<br>Michaella out | MHz                        | tempor<br>operati    |
| t <sub>PLH</sub>         | Propagation Delay<br>CP to Q <sub>n</sub>             | 3.3<br>5.0            | 2.0  | 8.5<br>6.0  | 15.0<br>11.0 | 1.0   | 16.5<br>12.0                      | 1.5<br>1.5  | 16.0<br>12.0                   | ns                         | 2-3,4                |
| t <sub>PHL</sub>         | Propagation Delay<br>CP to Q <sub>n</sub>             | 3.3<br>5.0            | 2.5<br>1.5                                       | 8.5<br>6.0  | 14.5<br>10.5 | 1.0<br>1.0  | 16.0<br>12.0                      | 2.0   | 16.0<br>11.5                   | ns                         | 2-3,4                |
| t <sub>PLH</sub>         | Propagation Delay<br>CP to TC                         | 3.3<br>5.0            | 3.5<br>2.5                                       | 10.5<br>7.5 | 18.0<br>12.0 | 1.0   | 19.5<br>14.0                      | 2.5<br>1.5  | 20.0<br>14.0                   | ns                         | 2-3,4                |
| t <sub>PHL</sub> V1.0    | Propagation Delay<br>CP to TC                         | 3.3<br>5.0            | 4.0<br>2.5                                       | 10.5<br>7.5 | 17.5<br>12.5 | 1.0   | 19.0<br>14.5                      | 3.0<br>2.0  | 19.0<br>13.5                   | ns                         | 2-3,4                |
| t <sub>PLH</sub><br>V1.0 | Propagation Delay CP to RC                            | 3.3<br>5.0            | 2.5<br>2.0                                       | 7.5<br>5.5  | 12.0<br>9.5  | 1.0   | 14.0<br>10.5                      | 2.0   | 13.5<br>10.5                   | ns                         | 2-3,4                |
| t <sub>PHL</sub> 1.0     | Propagation Delay<br>CP to RC                         | 3.3<br>5.0            | 2.5<br>1.5                                       | 7.0<br>5.0  | 11.5<br>8.5  | 1.0   | 12.5<br>9.5                       | 2.0<br>1.0  | 12.5<br>9.5                    | ns                         | 2-3,4                |
| tpLH                     | Propagation Delay<br>CE to RC                         | 3.3<br>5.0            | 2.5<br>1.5                                       | 7.0<br>5.0  | 12.0<br>8.5  | 0.31.0<br>1.0   | 14.0<br>10.0                      | 1.5<br>1.0  | 13.5<br>9.5                    | ns                         | 2-3,4                |
| t <sub>PHL</sub>         | Propagation Delay CE to RC                            | 3.3<br>5.0            | 2.0<br>1.5                                       | 6.5<br>5.0  | 11.0<br>8.0  | 1.0   | 12.5<br>9.5                       | 1.5<br>1.0  | 12.5<br>9.0                    | ns                         | 2-3,4                |
| t <sub>PLH</sub>         | Propagation Delay U/D to RC                           | 3.3<br>5.0            | 2.5<br>1.5                                       | 6.5<br>5.0  | 12.5<br>9.0  | 1.0   | 14.5<br>11.0                      | 2.0<br>1.0  | 14.5<br>10.0                   | ns                         | 2-3,4                |
| tPHL<br>Aµ 08            | Propagation Delay U/D to RC                           | 3.3<br>5.0            | 2.5<br>1.5                                       | 7.0<br>5.0  | 12.0<br>8.5  | 1.0   | 15.0<br>11.0                      | 2.0<br>1.0  | 13.5<br>10.0                   | ns                         | 2-3,4                |
| t <sub>PLH</sub>         | Propagation Delay U/D to TC                           | 3.3<br>5.0            | 2.0<br>1.5                                       | 7.0<br>5.0  | 11.5<br>8.5  | 1.0   | 14.0<br>13.5                      | 1.5<br>1.0  | 13.5<br>9.5                    | ns                         | 2-3,4                |
| tpHL                     | Propagation Delay U/D to TC                           | 3.3<br>5.0            | 2.0<br>1.5                                       | 6.5<br>5.0  | 11.0<br>8.5  | 1.0   | 13.5<br>10.0                      | 1.5<br>0.8 1.0  | 12.5<br>9.5                    | ns                         | 2-3,4                |
| <sup>t</sup> PLH         | Propagation Delay<br>P <sub>n</sub> to Q <sub>n</sub> | 3.3<br>5.0            | 2.5  | 8.0<br>5.5  | 13.5<br>9.5  | 1.0<br>1.0  | 16.5<br>11.5                      | 2.0<br>1.0  | 15.5<br>10.5                   | ns                         | 2-3,4                |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

| r. |   |   |   |
|----|---|---|---|
|    |   |   |   |
|    |   | 3 |   |
|    |   |   |   |
|    | 4 | 4 | 4 |

| Symbol               | Parameter   | (V)        |            | $A = +25$ $C_L = 50 p$ |              | to +       | 125°C<br>50 pF | - FE 10. 1 | 85°C<br>50 pF | Units | No.   |     |
|----------------------|---|------------|------------|------------------------|--------------|------------|----------------|------------|---------------|-------|-------|-----|
|                      | atuc  |            | Out        | Min                    | Тур          | Max        | Min            | Max        | Min           | Max   | al Bu | 100 |
| t <sub>PHL</sub>     | Propagation Delay<br>P <sub>n</sub> to Q <sub>n</sub> | 3.3<br>5.0 | 2.5<br>1.5 | 7.5<br>5.5             | 13.0<br>9.5  | 1.0<br>1.0 | 15.5<br>10.5   | 1.5<br>1.0 | 14.5<br>10.5  | ns    | 2-3,4 |     |
| t <sub>PLH</sub> 191 | Propagation Delay                                     | 3.3<br>5.0 | 3.5<br>2.0 | 9.5<br>5.5             | 14.5<br>9.5  | 1.0<br>1.0 | 18.0<br>12.5   | 2.5<br>1.0 | 17.5<br>10.5  | ns    | 2-3,4 |     |
| t <sub>PHL</sub>     | Propagation Delay                                     | 3.3<br>5.0 | 3.0<br>2.0 | 8.0<br>6.0             | 13.5<br>10.0 | 1.0<br>1.0 | 15.5<br>11.5   | 2.0<br>1.5 | 15.5<br>11.0  | ns    | 2-3,4 |     |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

# AC Operating Requirements: See Section 2 for waveforms

|                  |                                   |                   | 74.                               | AC              | 54AC  | 74AC   | W. F. | E277 12 |
|------------------|-----------------------------------|-------------------|-----------------------------------|-----------------|---|--|---|---------|
| Symbol           | Parameter                         | V <sub>CC</sub> * | T <sub>A</sub> = C <sub>L</sub> = | + 25°C<br>50 pF | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units                                     | Fig.    |
|                  | Pin Assignment<br>for LCC and PCC |                   | Тур                               | Flatpak a       | Guaranteed Min  | imum   | 1.5 St                                    |         |
| ts               | Setup Time, HIGH or LOW           | 3.3<br>5.0        | 1.0<br>0.5                        | 3.0<br>2.0      | 4.0   | 3.0<br>2.5   | ns  | 2-7     |
| th               | Hold Time, HIGH or LOW            | 3.3<br>5.0        | -1.5<br>-0.5                      | 0.5<br>1.0      | 1.5   | 1.0  | ns  | 2-7     |
| ts               | Setup Time, LOW  CE to CP         | 3.3<br>5.0        | 3.0<br>1.5                        | 6.0<br>4.0      | 9.0<br>6.0  | 7.0<br>4.5   | ns  | 2-7     |
| th               | Hold Time, LOW  CE to CP          | 3.3<br>5.0        | -4.0<br>-2.5                      | -0.5<br>0       | 0<br>0.5  | -0.5<br>0  | ns  | 2-7     |
| ts               | Setup Time, HIGH or LOW U/D to CP | 3.3<br>5.0        | 4.0<br>2.5                        | 8.0<br>5.5      | 10.5<br>7.5   | 9.0<br>6.5   | ns  | 2-7     |
| th               | Hold Time, HIGH or LOW U/D to CP  | 3.3<br>5.0        | -5.0<br>-3.0                      | 0               | 0 1.0   | 0 0.5  | ns  | 2-7     |
| t <sub>w</sub>   | PL Pulse Width, LOW               | 3.3<br>5.0        | 2.0<br>1.0                        | 3.5<br>1.0      | 5.0<br>5.0  | 4.0<br>1.0   | ns  | 2-3     |
| t <sub>w</sub>   | CP Pulse Width, LOW               | 3.3<br>5.0        | 2.0                               | 3.5<br>3.0      | 6.0<br>6.0  | 4.0<br>4.0   | ns  | 2-3     |
| t <sub>rec</sub> | Recovery Time PL to CP            | 3.3<br>5.0        | -0.5<br>-1.0                      | 0               | 1.5   | O DETATO TRE   | ns  | 2-3,7   |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

# Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions      |
|-----------------|-------------------------------|------|-------|-----------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 75.0 | pF    | $V_{CC} = 5.0V$ |



# 54AC/74AC240 • 54ACT/74ACT240 Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

#### **Features**

■ Inverting TRI-STATE outputs drive bus lines or buffer memory address registers

ROKETTY &

Symbol

- Outputs source/sink 24 mA
- 'ACT240 has TTL-compatible inputs

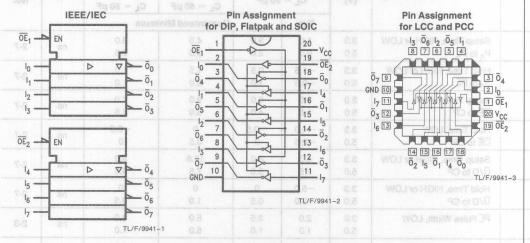
AC Electrical Characteristics: see Section 2 for waveforms (Continued

- Standard Military Drawing (SMD)
  - 'AC240: 5962-87550
  - 'ACT240: 5962-87759

Ordering Code: See Section 8

#### Logic Symbol

#### **Connection Diagrams**



#### 

#### **Truth Tables**

| Inpu            | its ea            | Outputs               |
|-----------------|-------------------|-----------------------|
| OE <sub>1</sub> | o.al <sub>n</sub> | (Pins 12, 14, 16, 18) |
| L               | L                 | VEDE HER MED A        |
| L               | Н                 | V8.0 ± V0.8 st 0.8 s  |
| Н               | X                 | Z                     |

| H | Inpu            | its     | Outpute                      |     |
|---|-----------------|---------|------------------------------|-----|
|   | OE <sub>2</sub> | In      | Outputs<br>(Pins 3, 5, 7, 9) |     |
|   | J87             | Tonsque | H Capacitatu                 | gq. |
| - | L               | Н       |                              |     |
|   | Н               | X       | Z                            |     |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|  | -0.5V to +7.0V                            |
|--|---|
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$ | -20 mA                                    |
| $V_I = V_{CC} + 0.5V$<br>DC Input Voltage ( $V_I$ )  | +20 mA<br>-0.5V to V <sub>CC</sub> + 0.5V |
| DC Output Diode Current ( $I_{OK}$<br>$V_O = -0.5V$  | -20 mA                                    |
| $V_0 = V_{CC} + 0.5V$                                | + 20 mA                                   |
| DC Output Voltage (V <sub>O</sub> )                  | $-0.5$ V to to $V_{CC} + 0.5$ V           |
| or Sink Current (I <sub>O</sub> )                    | ±50 mA                                    |
| DC V <sub>CC</sub> or Ground Current                 |   |

per Output Pin (ICC or IGND) ±50 mA -65°C to +150°C Storage Temperature (T<sub>STG</sub>) Junction Temperature (TJ) CDIP

PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT        | 2.0V to 6.0V<br>4.5V to 5.5V      |
|---|-----------------------------------|
| Input Voltage (V <sub>I</sub> )                   | 0V to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )                  | BTATE-IST mumber 0V to VCC        |
| Operating Temperature (T)<br>74AC/ACT<br>54AC/ACT | -40°C to +85°C<br>-55°C to +125°C |
| Minimum Input Edge Rate                           | (ΔV/Δt) Inemuo lugruO             |

VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

125 mV/ns

## DC Characteristics for 'AC Family Devices

|                             |                                      | 2.0                    | 74                      | AC                  | 0.8           | 54AC                            | 74AC                          | egal             | lay Jugal  |
|-----------------------------|--------------------------------------|------------------------|-------------------------|---------------------|---------------|---------------------------------|-------------------------------|------------------|--|
| Symbol                      | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C              | B.0<br>B.0_58 | T <sub>A</sub> = 5°C to + 125°C | T <sub>A</sub> = -40°C to +85 | °C Units         | Conditions   |
|                             | - = Tuol y                           | 6,6                    | Тур                     | Guaranteed Lie      |               | imits                           | High Leval                    | VOH Minimum      |  |
| VIH<br>HIV TO JI<br>- Z4 mA | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85 | 9.70          | 2.1<br>3.15<br>3.85             | 2.1<br>3.15<br>3.85           | V                | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$                  |
| V <sub>IL</sub> Au 0        | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65 | 0.5           | 0.9<br>1.35<br>1.65             | 0.9<br>1.35<br>1.65           | level value      | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V |
| Voh                         | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4   | 0.80          | 2.9<br>4.4<br>5.4               | 2.9<br>4.4<br>5.4             | V                | $I_{OUT} = -50 \mu\text{A}$                          |
| CMD.                        |                                      | 3.0                    |                         | 2.56                | lt ±          | 2.4                             | 2.46                          | Input<br>Current | $V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ mA}$ |
| Vir<br>S GND                | V = V   Aμ   VO = V <sub>0</sub>     | 4.5<br>5.5             |                         | 3.86<br>4.86        | DF ±          | 3.7<br>4.7                      | 3.76<br>4.76                  | TFV-STATE        | J <sub>OH</sub> −24 mA<br>−24 mA                     |
| V <sub>OL</sub> S —         | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1   | 8.1           | 0.1<br>0.1<br>0.1               | 0.1<br>0.1                    | V                | I <sub>OUT</sub> = 50 μA <sub>OO</sub>               |
| new Vae.                    |                                      | 3.0                    |                         | 0.36                | 02 -          | 0.50                            | 0.44                          | urent            | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA           |
| 0                           | VIN = VO<br>Or GND                   | 4.5<br>5.5             |                         | 0.36<br>0.36        | loar          | 0.50<br>0.50                    | 0.44<br>0.44                  | OV scient        | l <sub>OL</sub> 24 mA 24 mA                          |
| I <sub>IN</sub>             | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                |               | ± 1.0                           | ± 1.0                         | μА               | $V_I = V_{CC}$ , GND                                 |

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued) with A mumber of students of the Continued of the Cont

|                  | Vo.s. Parameter                      |                        | 74AC                     |                         | 54AC                             | 74AC                            | tice spir               | 1f Military/Asros  |  |
|------------------|--------------------------------------|------------------------|--------------------------|-------------------------|----------------------------------|---------------------------------|-------------------------|--|--|
| Symbol           |                                      | V <sub>CC</sub><br>(V) | T <sub>A</sub> =         | + 25°C                  | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                   | Conditions   |  |
| ta Vac           |                                      |                        | Тур                      | ngut Voltag             | Guaranteed Lir                   | nits                            | nent (I <sub>II</sub> ) | DC Input Diode Cu  |  |
| lozoV of         | Maximum TRI-STATE<br>Leakage Current | 5.5                    | (oV) eg<br>amperati<br>T | to ± 0.5                | ±10.0                            | or Va.0 ±5.0                    | μА                      | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I} = V_{CC}$ , GND<br>$V_{O} = V_{CC}$ , GND |  |
| I <sub>OLD</sub> | †Minimum Dynamic                     | 5.5                    | energia la co            | URNUMPO<br>at resentati | 50                               | 75                              | mA                      | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub> | Output Current                       | 5.5                    | 89                       | 'AC Devic               | -50                              | -75                             | mA                      | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc              | Maximum Quiescent<br>Supply Current  | 5.5                    |                          | 8.0                     | 160.0                            | 80.0                            | μА                      | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{|N}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

# **DC Characteristics for 'ACT Family Devices**

|                  |                                      |                        | 74               | ACT          | 54ACT                            | 74ACT                           | agnitist ma    | Work 1: Abnotuse maximum   |  |
|------------------|--------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|----------------|--|--|
| Symbol           | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units          | Conditions   |  |
|                  |                                      |                        | Тур              |              | Guaranteed Li                    | mits                            |                | The state of the s |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5              | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8<br>0.8                       | 0.8<br>0.8                      | V              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V              | $I_{OUT} = -50 \mu\text{A}$  |  |
| V1.0             | - 30 V xo V                          | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V              | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1          | 0.1<br>0.1                       | 0.1<br>0.1                      | V              | Ι <sub>ΟUT</sub> = 50 μΑ   |  |
| -50 µA           | = Tuol V                             | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | valle<br>Valle | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$  |  |
| IN/10 Ji         | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | ±1.0                             | ±1.0                            | μΑ             | $V_I = V_{CC}$ , GND   |  |
| loz              | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                  | ±0.5         | ±10.0                            | ±5.0                            | μА             | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |
| Ісст             | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |              | 1.6                              | 1.5 Inv                         | mA             | $V_{I} = V_{CC} - 2.1V$  |  |
| I <sub>OLD</sub> | †Minimum Dynamic                     | 5.5                    |                  |              | 50                               | 75                              | mA             | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub> | Output Current                       | 5.5                    |                  |              | -50                              | -75                             | mA             | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc AS           | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 160.0                            | 80.0                            | μА             | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for waveforms

|                     |                                     |                          |  | 74AC       |             | 54         | IAC                     | 74   | AC          | na2 i |             |
|---------------------|-------------------------------------|--------------------------|--|------------|-------------|------------|-------------------------|--|-------------|-------|-------------|
| Symbol              | Parameter                           | V <sub>CC</sub> *<br>(V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |             | to +       | −55°C<br>125°C<br>50 pF | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ |             | Units | Fig.<br>No. |
|                     |                                     | uO 4                     | Min  | Тур        | Max         | Min        | Max                     | Min  | Max         | 18 18 | 100         |
| t <sub>PLH</sub>    | Propagation Delay<br>Data to Output | 3.3<br>5.0               | 1.5<br>1.5                                       | 6.0<br>4.5 | 8.0<br>6.5  | 1.0<br>1.0 | 11.0<br>8.5             | 1.0  | 9.0<br>7.0  | ns    | 2-3,4       |
| t <sub>PHL</sub> 10 | Propagation Delay  Data to Output   | 3.3<br>5.0               | 1.5<br>1.5                                       | 5.5<br>4.5 | 8.0<br>6.0  | 1.0        | 10.5                    | 1.0  | 8.5<br>6.5  | ns    | 2-3,4       |
| t <sub>PZH</sub>    | Output Enable Time                  | 3.3<br>5.0               | 1.5<br>1.5                                       | 6.0<br>5.0 | 10.5<br>7.0 | 1.0        | 11.5<br>9.0             | 1.0  | 11.0<br>8.0 | ns    | 2-5         |
| t <sub>PZL</sub>    | Output Enable Time                  | 3.3<br>5.0               | 1.5<br>1.5                                       | 7.0<br>5.5 | 10.0        | 1.0<br>1.0 | 13.0<br>10.5            | 1.0<br>1.0   | 11.0<br>8.5 | ns    | 2-6         |
| t <sub>PHZ</sub>    | Output Disable Time                 | 3.3<br>5.0               | 1.5<br>1.5                                       | 7.0<br>6.5 | 10.0<br>9.0 | 1.0<br>1.0 | 12.5<br>10.5            | 1.0  | 10.5<br>9.5 | ns    | 2-5         |
| t <sub>PLZ</sub>    | Output Disable Time                 | 3.3<br>5.0               | 1.5<br>1.5                                       | 7.5<br>6.5 | 10.5<br>9.0 | 1.0<br>1.0 | 13.5<br>11.0            | 1.0<br>1.0   | 11.5<br>9.5 | ns    | 2-6         |

\*Voltage Range 3.3 is 3.3V ±0.3V \*Voltage Range 5.0 is 5.0V ±0.5V

# AC Electrical Characteristics: See Section 2 for waveforms

|                  | Parameter                           | V <sub>CC</sub> * (V) |  | 74ACT |      | 54   | ACT  | 74/  | ACT  |                      |       |
|------------------|-------------------------------------|-----------------------|--|-------|------|--|------|--|------|----------------------|-------|
| Symbol           |                                     |                       | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | $T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$ |      | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |      | Units                | Fig.  |
|                  |                                     |                       | Min  | Тур   | Max  | Min  | Max  | Min  | Max  | anno di la constanti |       |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 5.0                   | 1.5  | 6.0   | 8.5  | 1.0  | 9.5  | 1.5  | 9.5  | ns                   | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay Data to Output    | 5.0                   | 1.5  | 5.5   | 7.5  | 1.0  | 9.0  | 1.5  | 8.5  | ns                   | 2-3,4 |
| t <sub>PZH</sub> | Output Enable Time                  | 5.0                   | 1.5  | 7.0   | 8.5  | 1.0  | 10.0 | 1.0  | 9.5  | ns                   | 2-5   |
| t <sub>PZL</sub> | Output Enable Time                  | 5.0                   | 2.0  | 7.0   | 9.5  | 1.0  | 11.5 | 1.5  | 10.5 | ns                   | 2-6   |
| t <sub>PHZ</sub> | Output Disable Time                 | 5.0                   | 2.0  | 8.0   | 9.5  | 1.0  | 11.0 | 2.0  | 10.5 | ns                   | 2-5   |
| t <sub>PLZ</sub> | Output Disable Time                 | 5.0                   | 2.5  | 6.5   | 10.0 | 1.0  | 11.5 | 2.0  | 10.5 | ns                   | 2-6   |

\*Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol | Parameter         | Тур  | Units | Conditions             |  |
|--------|-------------------|------|-------|------------------------|--|
| CIN    | Input Capacitance | 4.5  | pF    | $V_{CC} = 5.0V$        |  |
| CPD    | Power Dissipation | 45.0 |       | V <sub>CC</sub> = 5.0V |  |
| -      | Capacitance       | 45.0 | pF    |                        |  |

# 54AC/74AC241 • 54ACT/74ACT241 Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

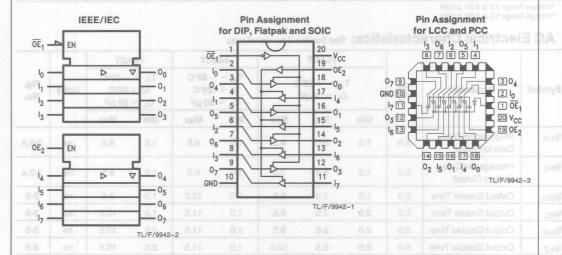
#### **Features**

- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- 'ACT241 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC241: 5962-87551
  - 'ACT241: 5962-89847

Ordering Code: See Section 8

**Logic Symbol** 

#### **Connection Diagrams**



| Pin<br>Names               | Description                                 |
|----------------------------|---|
| ŌĒ₁,                       | TRI-STATE Output Enable Input               |
| OE <sub>2</sub>            | TRI-STATE Output Enable Input (Active HIGH) |
| $l_0 - l_7$<br>$O_0 - O_7$ | Inputs Outputs                              |

#### **Truth Tables**

| Inputs          |                | Outputs               |  |  |  |  |  |
|-----------------|----------------|-----------------------|--|--|--|--|--|
| OE <sub>1</sub> | I <sub>n</sub> | (Pins 12, 14, 16, 18) |  |  |  |  |  |
| L               | L              | L L                   |  |  |  |  |  |
| Lan             | Heoms          | DEGEO HIGH            |  |  |  |  |  |
| H               | X              | S Power Dissin        |  |  |  |  |  |

| Inpu            | its  | Outputs          |  |  |  |  |
|-----------------|--|------------------|--|--|--|--|
| OE <sub>2</sub> | Inputs   I | (Pins 3, 5, 7, 9 |  |  |  |  |
| Н               | L  | L                |  |  |  |  |
| Н               | Н  | Н                |  |  |  |  |
| L               | X  | Z                |  |  |  |  |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

| Supply Voltage (V <sub>CC</sub> )  | -0.5          | V to +7.0V                     | 'ACT  | 4.5V to 5.5V   |
|--|---------------|--------------------------------|---|--|
| DC Input Diode Current (I <sub>IK</sub> )  | etimi         |                                | Input Voltage (V <sub>I</sub> )                                 | 0V to V <sub>CC</sub>  |
| $V_{l} = -0.5V$ $V_{l} = V_{CC} + 0.5V$ DC Input Voltage (V <sub>l</sub> )                 | -0.5V to V    | -20 mA<br>+20 mA<br>(CC + 0.5V | Output Voltage (V <sub>O</sub> ) Operating Temperature (Taylor) | -40°C to +85°C   |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$                                      |               | -20 mA                         | 54AC/ACT Minimum Input Edge Rate                                | -55°C to +125°C  |
| $V_O = V_{CC} + 0.5V$ DC Output Voltage ( $V_O$ )  | -0.5V to to V | + 20 mA                        | 'AC Devices V <sub>IN</sub> from 30% to 70%                     | OHD Output Current   |
| DC Output Source<br>or Sink Current (I <sub>O</sub> )                                      |               | ± 50 mA                        | V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V<br>Minimum Input Edge Rate   | 125 mV/ns  |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) |               | ±50 mA                         | 'ACT Devices<br>V <sub>IN</sub> from 0.8V to 2.0V               | *All outputs loaded; thresholds on Input as: **All swimum test duration 2.0 ms, one output |
| Storage Temperature (T <sub>STG</sub> ) Junction Temperature (T <sub>J</sub> )             | -65°C         | to +150°C                      |   | of beelmanding one VOLD to go 125 mV/ns of terminable of OMES to CAMB to got               |
| CDIP<br>PDIP   |               | 175°C<br>140°C                 | or 'ACT Family De   | DC Characteristics for   |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# **DC Characteristics for 'AC Family Devices**

|                    | - 00V10                              | 0.8                 | 74                   | AC                  | 0.8                              | 54AC                | 0.8                             | 6.1                    | 74AC                | 1          | egah     | Input Vo                              |  |
|--------------------|--------------------------------------|---------------------|----------------------|---------------------|----------------------------------|---------------------|---------------------------------|------------------------|---------------------|------------|----------|---------------------------------------|--|
| Symbol             | Parameter                            | V <sub>CC</sub> (V) | T <sub>A</sub> =     | + 25°C              | T <sub>A</sub> = -55°C to +125°C |                     | T <sub>A</sub> = -40°C to +85°C |                        | 85°C                | Units      | Con      | ditions                               |  |
| 50 µA              | - = Tuo! y                           | 1.1                 | Тур                  |                     | 5.5                              | Guara               | nteed L                         | imits                  | 4,5                 | lav        | High Le  | Minimun                               | ноУ  |
| L or VIH<br>—24 mA | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75  | 2.1<br>3.15<br>3.85 | 3.70                             | 2.1<br>3.15<br>3.85 | 8.6<br>8.86                     | ep.c                   | 2.1<br>3.15<br>3.85 |            | V        | V <sub>OUT</sub> = or V <sub>CC</sub> |  |
| V <sub>IL</sub>    | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75  | 0.9<br>1.35<br>1.65 | 01,4<br>1:0<br>1:0               | 0.9<br>1.35<br>1.65 | 1.0                             | 0.001                  | 0.9<br>1.35<br>1.65 | lev        | n Loy Le | V <sub>OUT</sub> = or V <sub>CC</sub> | 0.1V<br>- 0.1VoV                             |
| Voh<br>Am AS       | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49 | 2.9<br>4.4<br>5.4   | 0.60                             | 2.9<br>4.4<br>5.4   | 0.36                            |                        | 2.9<br>4.4<br>5.4   |            | ٧        | I <sub>OUT</sub> =                    | -50 μΑ                                       |
|                    | Jua VI = VOC                         | 3.0                 |                      | 2.56                | 0.† ±                            | 2.4                 | 1.0主                            |                        | 2.46                |            |          | *V <sub>IN</sub> =                    | V <sub>IL</sub> or V <sub>IH</sub><br>-12 mA |
|                    | $\mu A = V_{ij}$ $V_0 = V_{ij}$      | 4.5<br>5.5          |                      | 3.86<br>4.86        | ±10.0                            | 3.7<br>4.7          |                                 |                        | 3.76<br>4.76        |            |          | Іон М                                 | -24 mA<br>-24 mA                             |
| V <sub>OL</sub>    | Maximum Low Level Output Voltage     | 3.0<br>4.5          | 0.002<br>0.001       | 0.1<br>0.1          | 8.1                              | 0.1                 |                                 | 8.0                    | 0.1<br>0.1          |            | V        | TUOUT IF                              | 50 μΑ  |
|                    | = guoV Am                            | 5.5                 | 0.001                | 0.1                 | 68                               | 0.1                 |                                 |                        | 0.1                 | -          | en Dynen | uminiM1                               | cuol   |
|                    | = <sub>QHQ</sub> V Am                | 3.0                 |                      | 0.36                | -80                              | 0.50                |                                 |                        | 0.44                |            | inanu    | *V <sub>IN</sub> =                    | V <sub>IL</sub> or V <sub>IH</sub><br>12 mA  |
|                    | μΑ V <sub>IN</sub> = V <sub>O</sub>  | 4.5<br>5.5          |                      | 0.36<br>0.36        | 160.0                            | 0.50<br>0.50        |                                 |                        | 0.44                | ins        |          | loL M                                 | 24 mA<br>24 mA                               |
| I <sub>IN</sub>    | Maximum Input<br>Leakage Current     | 5.5                 |                      | ±0.1                |                                  | ±1.0                | nethny to                       | diso rille<br>and a te | ±1.0                | es Jugai i | μΑ       | $V_1 = V_0$                           | C, GND                                       |

 $<sup>\</sup>ensuremath{^{*}\text{All}}$  outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'AC Family Devices (Continued) and a mumber of the continued and a mumber of the continued and th

|                      | Parameter                            |                        | 74.                       | AC        | 54AC                              | 74AC                            | 102 006               | 11 Military/Aerosp   |  |
|----------------------|--------------------------------------|------------------------|---------------------------|-----------|-----------------------------------|---------------------------------|-----------------------|--|--|
| Symbol<br>Va.a of    |                                      | V <sub>CC</sub><br>(V) | T <sub>A</sub> =          | + 25°C    | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                 | Conditions   |  |
|                      |                                      |                        | Тур                       | estloV ju | Guaranteed L                      | imits                           | rent (I <sub>IK</sub> | DC Input Diode Cu  |  |
| loz <sup>V</sup> orl | Maximum TRI-STATE<br>Leakage Current | 5.5                    | age (Vo)<br>emperar<br>71 | ±0.5      | ±10.0                             | ±5.0                            | μА                    | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND |  |
| lold                 | †Minimum Dynamic                     | 5.5                    | inhall bio                | RA NJAR   | 50 108 -                          | 75                              | mA                    | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub>     | Output Current                       | 5.5                    | 890                       | NC Devi   | -50 02+                           | -75                             | mA                    | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc.                 | Maximum Quiescent<br>Supply Current  | 5.5                    | 30% to 8                  | 8.0       | 160.0                             | 80.0                            | μА                    | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{\text{IN}}$  and  $I_{\text{CC}} @ 3.0V$  are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\text{CC}}$ .

#### **DC Characteristics for 'ACT Family Devices**

|                      |                                      |                        | 744              | ACT          |                                   | 54ACT        | nsb doirt | 74ACT                          | era egmist m | Note 1: Absolute maxim   |  |
|----------------------|--------------------------------------|------------------------|------------------|--------------|-----------------------------------|--------------|-----------|--------------------------------|--------------|--|--|
| Symbol               | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to + 125°C |              |           | T <sub>A</sub> = -40°C to +85° |              | Conditions   |  |
|                      |                                      |                        | Тур              |              |                                   | Guara        | nteed L   | imits                          |              |  |  |
| V <sub>IH</sub>      | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   | DAVA                              | 2.0          | may<br>c  | 2.0<br>2.0                     | V            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>      | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5              | 0.8          | TA =                              | 0.8          | 25°C      | 0.8<br>0.8                     | V            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>      | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | Guan                              | 4.4<br>5.4   | 1.0       | 4.4<br>5.4                     | V            | $I_{OUT} = -50 \mu\text{A}$  |  |
| V1.0 -               | 7.94566                              | 4.5<br>5.5             |                  | 3.86<br>4.86 | 8.88<br>8.88                      | 3.70<br>4.70 | 3.15      | 3.76<br>4.76                   | eps<br>V     | $^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub> /1.0 | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1   | 1.38                              | 0.1          | 1.36      | 8.25 0.1 A<br>8.35 0.1 B       | Vege         | I <sub>OUT</sub> = 50 μA   |  |
| -60 µA               | = Tuol V                             | 4.5<br>5.5             |                  | 0.36<br>0.36 | 2.9<br>4,4<br>5,4                 | 0.50<br>0.50 |           | 0.44                           |              | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |  |
| VIL or VIII          | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | 2.4                               | ±1.0         | 2.58      | ±1.0                           | μΑ           | $V_I = V_{CC}$ , GND   |  |
| loz                  | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                  | ±0.5         | 3.7<br>4.7                        | ±10.0        | 3.86      | ±5.0                           | μΑ           | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |
| ICCT                 | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |              | 0.1                               | 1.6          | 0.1       | \$00.0<br>1.5,4                | mA           | $V_I = V_{CC} - 2.1V$  |  |
| IOLD                 | †Minimum Dynamic                     | 5.5                    |                  |              | 1.0                               | 50           | 1.0       | 75                             | mA           | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub>     | Output Current                       | 5.5                    |                  |              | na.o                              | -50          | aen       | -75                            | mA           | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc AS<br>Am AS      | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 0.50                              | 160.0        | 0.36      | 80.0                           | μА           | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

lenoHel/KK

# AC Electrical Characteristics: See Section 2 for waveforms

|                  |                                     | E. 176            |            | 74AC   |              | 54         | AC   | 74         | AC                     | ma2 i |             |
|------------------|-------------------------------------|-------------------|------------|--|--------------|------------|--|------------|------------------------|-------|-------------|
| Symbol           | Parameter                           | V <sub>CC</sub> * |            | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |            | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                  | phints                              | E163 (            | Min        | Тур  | Max          | Min        | Max  | Min        | Max                    | A le  | inn         |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 1.5<br>1.5 | 6.0<br>5.0                                       | 9.0<br>7.0   | 1.0<br>1.0 | 12.0<br>9.5  | 1.5<br>1.0 | 10.0<br>7.5            | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 1.5<br>1.5 | 6.0<br>4.5                                       | 9.0<br>7.0   | 1.0        | 11.5<br>9.0  | 1.0<br>1.0 | 10.5<br>7.5            | ns    | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time                  | 3.3<br>5.0        | 1.5        | 6.5<br>5.5                                       | 12.5         | 1.0        | 13.0   | 1.0        | 13.0<br>9.5            | ns    | 2-5         |
| t <sub>PZL</sub> | Output Enable Time                  | 3.3<br>5.0        | 1.5<br>1.5 | 7.0<br>5.5                                       | 12.0<br>9.0  | 1.0<br>1.0 | 13.0<br>10.0   | 1.5<br>1.0 | 13.0<br>9.5            | ns    | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 2.0<br>1.5 | 8.0<br>6.5                                       | 12.0<br>10.0 | 1.0<br>1.0 | 13.0<br>11.5   | 2.0        | 12.5<br>10.5           | ns    | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 1.5<br>1.5 | 7.0<br>6.0                                       | 12.5<br>10.0 | 1.0<br>1.0 | 13.0<br>11.5   | 1.0<br>1.0 | 13.5<br>10.5           | ns    | 2-6         |

\*Voltage Range 3.3 is 3.3V ±3.3V Voltage Range 5.0 is 5.0V ±0.5V

#### AC Electrical Characteristics: See Section 2 for waveforms

| Symbol           | 1 60 % 90 %                         |                   |     | 74ACT                 |      | 54/  | ACT  | 74/  | ACT  | 913 PSA  | 1.00   |
|------------------|-------------------------------------|-------------------|-----|-----------------------|------|--|------|--|------|--|--------|
|                  | Parameter                           | V <sub>CC</sub> * |     | A = +25°<br>CL = 50 p |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |      | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ |      | Units  | Fig.   |
|                  |                                     | - E Dr            | Min | Тур                   | Max  | Min  | Max  | Min  | Max  | and the same of th |        |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 5.0               | 1.5 | 6.5                   | 9.0  | 1.0  | 10.0 | 1.5  | 10.0 | ns   | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>Data to Output | 5.0               | 1.5 | 7.0                   | 9.0  | 1.0  | 10.0 | 1.5  | 10.0 | ns   | 2-3, 4 |
| tpzH             | Output Enable Time                  | 5.0               | 1.5 | 6.0                   | 9.0  | 1.0  | 11.5 | 1.0  | 10.0 | ns   | 2-5    |
| t <sub>PZL</sub> | Output Enable Time                  | 5.0               | 1.5 | 7.0                   | 10.0 | 1.0  | 12.5 | 1.5  | 11.0 | ns   | 2-6    |
| t <sub>PHZ</sub> | Output Disable Time                 | 5.0               | 1.5 | 8.0                   | 10.5 | 1.0  | 12.5 | 1.5  | 11.5 | ns   | 2-5    |
| t <sub>PLZ</sub> | Output Disable Time                 | 5.0               | 2.0 | 7.0                   | 10.5 | 1.0  | 12.5 | 1.5  | 11.5 | ns   | 2-6    |

\*Voltage Range 5.0 is 5.0V ±0.5V

### Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN (81 ,81     | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 45.0 | pF    | V <sub>CC</sub> = 5.0V |

4



# 54AC/74AC244 • 54ACT/74ACT244 Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

#### **Features**

■ TRI-STATE outputs drive bus lines or buffer memory address registers

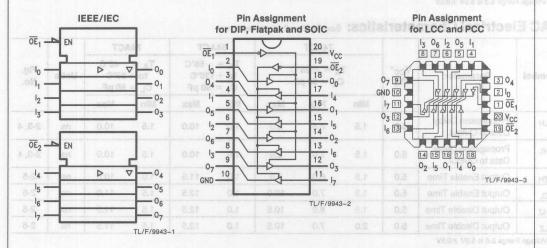
Symbol

- Outputs source/sink 24 mA
- 'ACT244 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC244: 5962-87552
  - 'ACT244: 5962-87760

Ordering Code: See Section 8

### **Logic Symbol**

#### **Connection Diagrams**



#### **Truth Tables**

| Pin Names                          | Description  |
|------------------------------------|--|
| $\overline{OE}_1, \overline{OE}_2$ | TRI-STATE Output Enable Inputs   |
| 10-17                              | Inputs VA a service of the service o |
| 00-07                              | Outputs  |

| Input           | ts     | Outputs               |     |
|-----------------|--------|-----------------------|-----|
| OE <sub>1</sub> | Inegra | (Pins 12, 14, 16, 18) |     |
| b.8s            | Lnobs  | op L Power Dissip     | i i |
| L               | H      | ronanosqsO H          |     |
| Н               | X      | Z                     |     |

| Inpu            | its | Outputs           |
|-----------------|-----|-------------------|
| OE <sub>2</sub> | In  | (Pins 3, 5, 7, 9) |
| L               | L   | L                 |
| L               | Н   | Н                 |
| Н               | X   | Z                 |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>) DC Input Diode Current (IIK)  $V_1 = -0.5V$ -20 mA  $V_1 = V_{CC} + 0.5V$ +20 mA DC Input Voltage (V<sub>I</sub>) -0.5V to V<sub>CC</sub> + 0.5V

DC Output Diode Current (IOK) -20 mA  $V_0 = -0.5V$  $V_0 = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (Vo) -0.5V to to V<sub>CC</sub> + 0.5V DC Output Source

or Sink Current (IO) DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) -65°C to +150°C Storage Temperature (TSTG)

Junction Temperature (T,J) CDIP

PDIP 140°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply.

#### Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>) 'AC - -

2.0V to 6.0V 4.5V to 5.5V 'ACT OV to Vcc Input Voltage (VI) Output Voltage (Vo) OV to VCC

Operating Temperature (TA)

74AC/ACT -40°C to +85°C 54AC/ACT -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

VIN from 30% to 70% of VCC

125 mV/ns V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices VIN from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V

temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## DC Characteristics for 'AC Family Devices

| W 4 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 |                                      | 33.65                  |                      | 10/1/10               | L. Made                           | 53.4    | - (- L) - (-)        |                             | RETURNAL STATE                  | N. 184 STEEL STATE OF THE STATE |  |
|---|--------------------------------------|------------------------|----------------------|-----------------------|-----------------------------------|---------|----------------------|-----------------------------|---------------------------------|--|--|
| 0.1V                                    | - 00 V VCC                           | 2.0                    | 74                   | AC 0.S                | 54AC                              | 1.6     | 5.5                  | 74AC                        | eg                              | Input Volta  |  |
| Symbol                                  | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =     | + 25°C                | T <sub>A</sub> = -55°C to + 125°C |         | -40°                 | T <sub>A</sub> = C to +85°C | Units                           | Conditions   |  |
| - 50 jsA -                              |                                      | 4,4                    | Тур                  | Typ Guaranteed Limits |                                   |         |                      |                             | ligh Level                      | V <sub>OH</sub> Minimum I  |  |
| VIH<br>HIV TO JI'<br>Am AS —            | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75  | 2.1<br>3.15<br>3.85   | 2.1<br>3.15<br>3.85               | 84.8    | 4.5                  | 2.1<br>3.15<br>3.85         | V                               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>                         | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75  | 0.9<br>1.35<br>1.65   | 0.9<br>1.35<br>1.65               | 0.001   | 4.5                  | 0.9<br>1.35<br>1.65         | eve. <b>V</b> .vo.              | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| Voh 10 m<br>Am AS<br>Am AS              | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49 | 2.9<br>4.4<br>5.4     | 2.9<br>4.4<br>5.4                 |         | 4.6                  | 2.9<br>4.4<br>5.4           | ٧                               | $I_{OUT} = -50 \mu\text{A}$  |  |
|   | OV = IV AH                           | 0.1±                   |                      | 0.1±                  | 1.0±                              |         | s.s                  | triemuO agair               | nput Leal                       | *VIN = VIL or VIH  |  |
|   | $V = V_{IV}$ $V = V_{IV}$            | 3.0<br>4.5<br>5.5      |                      | 2.56<br>3.86<br>4.86  | 2.4<br>3.7<br>4.7                 |         | 8.6                  | 2.46<br>3.76<br>4.76        | ATS-IRI                         | -12 mA<br>I <sub>OH</sub> -24 mA<br>-24 mA   |  |
| VOL                                     | Maximum Low Level                    | 3.0                    | 0.002                | 0.1                   | 0.1                               | 8.0     | 8,8                  | 0.1                         |                                 | $I_{OUT} = 50 \mu A$   |  |
|   | Output Voltage                       | 4.5<br>5.5             | 0.001                | 0.1                   | 0.1<br>0.1                        |         | 8.8                  | 0.1                         | V<br>Dynamic                    | muminiM† 0.10  |  |
|   |                                      | -75                    |                      | -90                   |                                   |         | 6.5                  |                             | 71301                           | *VIN = VIL or VIH  |  |
| 200                                     | AA Or GND                            | 3.0<br>4.5<br>5.5      |                      | 0.36<br>0.36<br>0.36  | 0.50<br>0.50<br>0.50              | abnu tu | B,a                  | 0.44<br>0.44<br>0.44        | Sufescent<br>FenV<br>renolds on | 12 mA<br>1 <sub>OL</sub> 24 mA<br>24 mA  |  |
| I <sub>IN</sub>                         | Maximum Input<br>Leakage Current     | 5.5                    |                      | ±0.1                  | ±1.0                              |         | at a time<br>0.25°C. | ±1.0 of leading             | μΑ                              | $V_{I} = V_{CC}$ , GND   |  |

±50 mA

±50 mA

175°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol<br>Va.a of     | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C   |             |              |                          | Units     | Conditions  |  |
|-----------------------|-------------------------------------|------------------------|--------------------------|-------------|--------------|--------------------------|-----------|---|--|
|                       |                                     |                        | Тур                      | stioV jugn  | Guaranteed L | imits                    | rent (lps | DC Input Diode Curr   |  |
| loz <sup>oV</sup> ol  | Maximum TRI-STATE® Current          | 5.5                    | oV) egel<br>negmaT<br>TC | ±0.5        | ± 10.0       | o <sub>3 V3.0</sub> ±5.0 | μА        | $\begin{aligned} &V_{l}\left(\text{OE}\right) = V_{lL}, V_{lH} \\ &V_{l} = V_{CC}, V_{GND} \\ &V_{O} = V_{CC}, GND \end{aligned}$ |  |
| I <sub>OLD</sub>      | †Minimum Dynamic                    | 5.5                    | on a Relat               | t coursists | 50 03-       | 75                       | mA        | V <sub>OLD</sub> = 1.65V Max  |  |
| IOHD                  | Output Current                      | 5.5                    | 890                      | (AC Day     | -50          | -75                      | mA        | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc <sub>1</sub> \Var | Maximum Quiescent<br>Supply Current | 5.5                    | 30% to<br>3V, 4.8V       | 8.0         | 160.0        | 80.0                     | μА        | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## **DC Characteristics for 'ACT Family Devices**

|                        |                                      |                        | 74             | ACT          | 54ACT                            | 74ACT           | dan mun      | Note 1: Ansolute made   |  |
|------------------------|--------------------------------------|------------------------|----------------|--------------|----------------------------------|-----------------|--------------|---|--|
| Symbol                 | Parameter                            | V <sub>CC</sub><br>(V) |                |              | T <sub>A</sub> = -55°C to +125°C |                 | Units        | Conditions  |  |
|                        |                                      |                        | Тур            |              | Guaranteed Li                    | imits           |              |   |  |
| V <sub>IH</sub>        | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5            | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0      | ٧            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub>        | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5     | 0.8          | 0.8                              | 0.8             | V            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>        | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4      | ٧            | $I_{OUT} = -50 \mu\text{A}$   |  |
|                        | 11000                                | 4.5<br>5.5             |                | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76    | egati        | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$              |  |
| V <sub>OL</sub>        | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001 | 0.1          | 0.1                              | 0.1             | ٧            | I <sub>OUT</sub> = 50 μA  |  |
| 50 µA                  | 2.8 lour = -<br>4.4 V                | 4.5<br>5.5             |                | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44    | high<br>over | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{IOL}$ $^{24 \text{ mA}}$ $^{24 \text{ mA}}$ |  |
| I <sub>IN</sub> V 10 ] | Maximum Input Leakage Current        | 5.5                    |                | ±0.1         | ±1.0                             | ±1.0            | μΑ           | $V_I = V_{CC}$ , GND  |  |
| loz                    | Maximum TRI-STATE®                   | 5.5                    |                | ±0.5         | ± 10.0                           | ±5.0            | μА           | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| ICCT                   | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6            | 1.0          | 1.6                              | 0.0 01.5 (eve.) | mA           | $V_I = V_{CC} - 2.1V$   |  |
| I <sub>OLD</sub>       | †Minimum Dynamic                     | 5.5                    |                | 1.0          | 50                               | 75              | mA           | V <sub>OLD</sub> = 1.65V Max  |  |
| IOHD                   | Output Current                       | 5.5                    |                |              | -50                              | -75             | mA           | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc St<br>Am AS        | Maximum Quiescent Supply Current     | 5.5                    |                | 8.0          | 160.0                            | 80.0            | μΑ           | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol           | Parameter                           | V <sub>CC</sub> * |            |            |             |            | to + 125°C<br>C <sub>L</sub> = 50 pF |            | 85°C<br>50 pF | Units   | Fig.<br>No. |
|------------------|-------------------------------------|-------------------|------------|------------|-------------|------------|--------------------------------------|------------|---------------|---------|-------------|
|                  |                                     |                   | Min        | Тур        | Max         | Min        | Max                                  | Min        | Max           | le ls   | toO         |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 2.0<br>1.5 | 6.5<br>5.0 | 9.0<br>7.0  | 1.0        | 12.5<br>9.5                          | 1.5<br>1.0 | 10.0<br>7.5   | ns      | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 2.0        | 6.5<br>5.0 | 9.0<br>7.0  | 1.0<br>1.0 | 12.0<br>9.0                          | 2.0<br>1.0 | 10.0<br>7.5   | ns      | 2-3,4       |
| t <sub>PZH</sub> | Output Enable Time                  | 3.3<br>5.0        | 2.0        | 6.0        | 10.5<br>7.0 | 1.0        | 11.5<br>9.0                          | 1.5<br>1.5 | 11.0          | ns      | 2-5         |
| t <sub>PZL</sub> | Output Enable Time                  | 3.3<br>5.0        | 2.5<br>1.5 | 7.5<br>5.5 | 10.0<br>8.0 | 1.0<br>1.0 | 13.0<br>10.5                         | 2.0<br>1.5 | 11.0<br>8.5   | ns      | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 3.0<br>2.5 | 7.0<br>6.5 | 10.0        | 1.0<br>1.0 | 12.5<br>10.5                         | 1.5<br>1.0 | 10.5<br>9.5   | of ahoo | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 2.5<br>2.0 | 7.5<br>6.5 | 10.5<br>9.0 | 1.0<br>1.0 | 13.0<br>11.0                         | 2.5<br>2.0 | 11.5<br>9.5   | ns      | 2-6         |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

#### AC Electrical Characteristics: See Section 2 for waveforms

| Symbol           | n Assignment                        | R.                | 74ACT  |     | 54ACT  T <sub>A</sub> = -55°C  to + 125°C  C <sub>L</sub> = 50 pF |     | $74ACT$ $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 \text{ pF}$ |        | Units | Fig.    |       |
|------------------|-------------------------------------|-------------------|--|-----|---|-----|--|--------|-------|---------|-------|
|                  | Parameter                           | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |     |   |     |  |        |       |         |       |
|                  |                                     |                   | Min  | Тур | Max   | Min | Max  | Min    | Max   | S 18 08 |       |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 5.0               | 2.0  | 6.5 | 9.0   | 1.0 | 10.0   | 1.5    | 10.0  | ns      | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay Data to Output    | 5.0               | 2.0  | 7.0 | 9.0   | 1.0 | 10.0   | 1.5    | 10.0  | ns      | 2-3,4 |
| t <sub>PZH</sub> | Output Enable Time                  | 5.0               | 1.5  | 6.0 | 8.5   | 1.0 | 9.5  | 1.0    | 9.5   | ns      | 2-5   |
| t <sub>PZL</sub> | Output Enable Time                  | 5.0               | 2.0  | 7.0 | 9.5   | 1.0 | 11.0   | 1.5 TA | 10.5  | ns      | 2-6   |
| t <sub>PHZ</sub> | Output Disable Time                 | 5.0               | 2.0  | 7.0 | 9.5   | 1.0 | 11.0   | 1.5    | 10.5  | ns      | 2-5   |
| tpLZ             | Output Disable Time                 | 5.0               | 2.5  | 7.5 | 10.0  | 1.0 | 11.5   | 2.0    | 10.5  | ns      | 2-6   |

#### Capacitance

| C <sub>PD</sub> Power Dissipation 45.0 pF V <sub>CC</sub> = 5.0V | Symbol | Parameter         | Тур  | Units | Conditions             |
|--|--------|-------------------|------|-------|------------------------|
| Capacitance 45.0 pF  | CIN    | Input Capacitance | 4.5  | pF    | $V_{CC} = 5.0V$        |
|  | CPD    |                   | 45.0 | pF    | V <sub>CC</sub> = 5.0V |
|  | 14161  | Capacitance       | 45.0 | pF    | A eu                   |



# 54AC/74AC245 • 54ACT/74ACT245 Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

#### **General Description**

The 'AC/'ACT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

#### **Features**

- Noninverting buffers
- Bidirectional data path
- A and B outputs source/sink 24 mA

AC Electrical Characteristics: See Section 2 for waveforms

- 'ACT245 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC245: 5962-87758
  - 'ACT245: 5962-87663

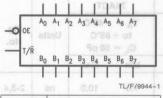
Ordering Code: See Section 8

#### **Logic Symbols**

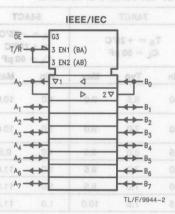
## Connection Diagrams

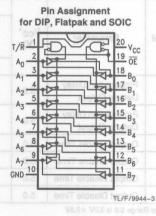
Symbol

Symbol



| Pin<br>Names                   | Description                                  |
|--------------------------------|--|
| ŌĒ                             | Output Enable Input                          |
| T/R                            | Transmit/Receive Input                       |
| A <sub>0</sub> -A <sub>7</sub> | Side A TRI-STATE                             |
| 2-5                            | Inputs or TRI-STATE Outputs                  |
| B <sub>0</sub> -B <sub>7</sub> | Side B TRI-STATE Inputs or TRI-STATE Outputs |



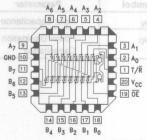


#### **Truth Table**

| Inp | outs | Outputs             |  |  |  |  |  |
|-----|------|---------------------|--|--|--|--|--|
| OE  | T/R  | Vo a =              |  |  |  |  |  |
| L   | L    | Bus B Data to Bus A |  |  |  |  |  |
| L   | Н    | Bus A Data to Bus B |  |  |  |  |  |
| Н   | X    | HIGH-Z State        |  |  |  |  |  |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial

# Pin Assignment for LCC and PCC



TL/F/9944-4

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )                     | -0.5V to $+7.0V$               |
|---|--------------------------------|
| DC Input Diode Current (IIK)                          |                                |
| $V_{I} = -0.5V$                                       | -20 mA                         |
| $V_I = V_{CC} + 0.5V$                                 | + 20 mA                        |
| DC Input Voltage (V <sub>I</sub> )                    | $-0.5$ V to $V_{CC}$ + $0.5$ V |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$ | -20 mA                         |

+20 mA  $V_O = V_{CC} + 0.5V$ DC Output Voltage (Vo) -0.5V to to  $V_{CC} + 0.5$ V

DC Output Source ±50 mA or Sink Current (Io)

DC V<sub>CC</sub> or Ground Current per Output Pin (ICC or IGND) Storage Temperature (TSTG) -65°C to +150°C

Junction Temperature (T<sub>.I</sub>) CDIP PDIP

140°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recom-

#### Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>) 2.0V to 6.0V 'AC 4.5V to 5.5V 'ACT OV to Vcc Input Voltage (V<sub>I</sub>) Output Voltage (VO) omanyo muminin OV to VCC Operating Temperature (TA) 74AC/ACT -40°C to +85°C 100000 - 55°C to + 125°C 54AC/ACT Minimum Input Edge Rate (ΔV/Δt)

'AC Devices VIN from 30% to 70% of VCC

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

VIN from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

mend operation of FACTTM circuits outside databook specifications.

#### DC Characteristics for 'AC Family Devices

|                                | - 30V 10                                  | 0.8               | 74                      | AC OS                | 54AC                        |       | 8.8  | 74AC                          | -60                  | Input Volti  |
|--------------------------------|---|-------------------|-------------------------|----------------------|-----------------------------|-------|------|-------------------------------|----------------------|--|
| Symbol                         | Parameter                                 | V <sub>CC</sub>   | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to + | 125°C | -40  | T <sub>A</sub> = 0°C to +85°C | Units                | Conditions   |
|                                | - = TUO! V                                | 4,4               | Тур                     |                      | Guaranteed Limi             |       | nits | nits                          |                      | Minimum HoV  |
| VIH<br>HIV 10 J                | Minimum High Level<br>Input Voltage       | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85         |       | 4.8  | 2.1<br>3.15<br>3.85           | V                    | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                           |
| V <sub>IL</sub> A <sub>A</sub> | Maximum Low Level<br>Input Voltage        | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65         |       | 4.5  | 0.9<br>1.35<br>1.65           | LowLev               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                           |
| V <sub>OH</sub>                | Minimum High Level<br>Output Voltage      | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4           |       | 4.5  | 2.9<br>4.4<br>5.4             | ٧                    | $I_{OUT} = -50 \mu\text{A}$                                      |
|                                | pA V <sub>I</sub> = V <sub>CC</sub>       | 0.11              |                         | 0.1±                 | T:0±                        |       | 8.5  | akage Current                 | Input Le             | *VIN = VIL or VIH  |
|                                | $V_1 = V_{QQ}$                            | 3.0<br>4.5        |                         | 2.56<br>3.86         | 2.4<br>3.7                  |       | 5,5  | 2.46<br>3.76                  | V                    | 12 mA  |
| 65V Max                        | t = quoV Am                               | 5.5               |                         | 4.86                 | 4.7                         |       | 5.5  | 4.76                          | Emacy C              | -24 mA   |
| VOLVAR                         | Maximum Low Level<br>Output Voltage       | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1           |       | 5.5  | 0.1<br>0.1<br>0.1             | vent<br>V<br>Quiasge | $I_{OUT} = 50 \mu A_{OHO}$                                       |
|                                | ФИЗ 10 ГОЧ<br>= (30) IV<br>= VOV<br>= VOV | 3.0<br>4.5<br>5.5 |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50        |       | 8.5  | 0.44<br>0.44<br>0.44          | OM                   | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA |
| I <sub>IN</sub>                | Maximum Input<br>Leakage Current          | 5.5               |                         | ±0.1                 | ±1.0                        |       |      | ±1.0 ue sno                   | μА                   | $V_I = V_{CC}$ , GND   |

±50 mA

175°C

†Maximum test duration 2.0 ms, one output loaded at a time.

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

| Symbol / Parameter |                                     | (V) | $T_A =$                        | + 25°C            | -55°C to +125°C     | -40°C to +85°C      | VV | Supply Voltage (Vo   |  |
|--------------------|-------------------------------------|-----|--------------------------------|-------------------|---------------------|---------------------|----|--|--|
| ooV of             |                                     |     | Тур                            | Guaranteed Limits |                     |                     |    | DC Input Diode Ou  |  |
| IOLD               | †Minimum Dynamic                    | 5.5 | (OV) ab                        | AthoV tugtu(      | 50                  | 75                  | mA | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD               | Output Current                      | 5.5 | nuisneqme                      | perating Te       | +50 + 00V           | et Va.0 -75         | mA | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc°881            | Maximum Quiescent<br>Supply Current | 5.5 |                                | 8.0               | 160.0               | 80.0                | μΑ | V <sub>IN</sub> = V <sub>CC</sub> or GND                                       |  |
| lozt<br>en\Vm      | Maximum I/O<br>Leakage Current      | 5.5 | 98<br>(0% to 70<br>V, 4.5V, 5. | ±0.6              | V2.0 + 00V<br>±11.0 | of of V2.0—<br>±6.0 | μA | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### DC Characteristics for 'ACT Family Devices

|                           | Parameter                            |                     |                        | 74                     | ACT           | 54ACT                             | 74ACT                           | ter mun   | Note it Absolute makin   |  |
|---------------------------|--------------------------------------|---------------------|------------------------|------------------------|---------------|-----------------------------------|---------------------------------|-----------|--|--|
| Symbol                    |                                      |                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions   |  |
|                           |                                      |                     |                        | Тур                    |               | Guaranteed L                      | imits                           | NUC - 1-1 | mend operation of FAI  |  |
| V <sub>IH</sub>           | Minimum High Level<br>Input Voltage  | 2440                | 4.5<br>5.5             | 1.5<br>1.5             | 2.0           | 2.0                               | 2.0<br>2.0                      | V         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>           | Maximum Low Level Input Voltage      | = A7                | 4.5<br>5.5             | 1.5<br>1.5             | 0.8           | 0.8                               | 0.8                             | V         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>           | Minimum High Level<br>Output Voltage |                     | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4    | 4.4<br>5.4                        | 4.4<br>5.4                      | V         | $I_{OUT} = -50 \mu\text{A}$  |  |
|                           | TUOV<br>- 20V 10 V                   | 2.1<br>3.15<br>3.85 | 4.5<br>5.5             |                        | 3.86<br>4.86  | 3.70<br>4.70                      | 3.76<br>4.76                    | age<br>V  | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| V <sub>OL</sub>           | Maximum Low Level Output Voltage     | 1.35                | 4.5<br>5.5             | 0.001<br>0.001         | 0.1<br>0.1    | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧         | I <sub>OUT</sub> = 50 μA   |  |
|                           | ruol V                               | 2.9                 | 4.5<br>5.5             |                        | 0.36<br>0.36  | 0.50<br>0.50                      | 0.44<br>0.44                    | High L    | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| IIN                       | Maximum Input Leakage                | Current             | 5.5                    |                        | ±0.1          | ±1.0                              | ±1.0                            | μΑ        | $V_I = V_{CC}$ , GND   |  |
| ICCT ST-                  | Maximum<br>I <sub>CC</sub> /Input    | 2.46                | 5.5                    | 0.6                    | 2.4<br>3.7    | 1.6                               | 1.5                             | mA        | $V_I = V_{CC} - 2.1V$  |  |
| lold                      | †Minimum Dynamic                     | 4.76                | 5.5                    |                        | 4.7           | 50                                | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD                      | Output Current                       | 7.0                 | 5.5                    |                        | 0.1           | -50                               | 10.0 -75 leve                   | mA        | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc                       | Maximum Quiescent<br>Supply Current  | 1.0                 | 5.5                    |                        | 8.0           | 160.0                             | 80.0                            | μА        | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |
| 12 TSOI<br>24 mA<br>24 mA | Maximum I/O<br>Leakage Current       | 0.44                | 5.5                    |                        | 08.0<br>0±0.6 | \$8.0<br>±11.0                    | ±6.0                            | μΑ        | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|  | 1 |  |
|--|---|--|

Select in

| Symbol Parameter | Parameter                              | V <sub>CC</sub> * |            |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |            | Units        | Fig.<br>No. |       |
|------------------|--|-------------------|------------|------------|--|------------|--|------------|--------------|-------------|-------|
|                  |  | 4110              | Min        | Тур        | Max  | Min        | Max  | Min        | Max          | furn        | 31-8  |
| t <sub>PLH</sub> | Propagation Delay An to Bn or Bn to An | 3.3<br>5.0        | 1.5<br>1.5 | 5.0<br>3.5 | 8.5<br>6.5   | 1.0<br>1.0 | 11.5<br>8.5  | 1.0<br>1.0 | 9.0<br>7.0   | ns          | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay An to Bn or Bn to An | 3.3<br>5.0        | 1.5        | 5.0<br>3.5 | 8.5<br>6.0   | 1.0<br>1.0 | 10.0<br>7.5  | 1.0<br>1.0 | 9.0<br>7.0   | ns          | 2-3,4 |
| t <sub>PZH</sub> | Output Enable Time                     | 3.3<br>5.0        | 2.5        | 7.0<br>5.0 | 11.5   | 1.0<br>1.0 | 13.5<br>10.0   | 2.0        | 12.5<br>9.0  | ns          | 2-5   |
| t <sub>PZL</sub> | Output Enable Time                     | 3.3<br>5.0        | 2.5<br>1.5 | 7.5<br>5.5 | 12.0<br>9.0  | 1.0<br>1.0 | 14.5<br>10.5   | 2.0<br>1.0 | 13.5<br>9.5  | ns          | 2-6   |
| t <sub>PHZ</sub> | Output Disable Time                    | 3.3<br>5.0        | 2.0<br>1.5 | 6.5<br>5.5 | 12.0<br>9.0  | 1.0        | 13.5<br>10.5   | 1.0        | 12.5<br>10.0 | ns          | 2-5   |
| t <sub>PLZ</sub> | Output Disable Time                    | 3.3<br>5.0        | 2.0<br>1.5 | 7.0<br>5.5 | 11.5<br>9.0  | 1.0<br>1.0 | 14.0<br>10.5   | 1.5<br>1.0 | 13.0<br>10.0 | ns          | 2-6   |

<sup>\*</sup>Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for waveforms

| Symbol           | Parameter   | HC 701    |                   | 74ACT  | XAM  | 54/ | ACT   | 74/ | ACT   |    | and . |      |
|------------------|---|-----------|-------------------|--|------|-----|---|-----|---|----|-------|------|
|                  |   | Parameter | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |      |     | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ |     | $T_A = -40^{\circ}C$<br>to +85°C<br>$C_L = 50 \text{ pF}$ |    | Units | Fig. |
|                  |   | T.        | Min               | Тур  | Max  | Min | Max   | Min | Max   | 2  | 30 0- |      |
| t <sub>PLH</sub> | Propagation Delay An to Bn or Bn to An  | 5.0       | 1.5               | 4.0  | 7.5  | 1.0 | 9.0   | 1.5 | 8.0   | ns | 2-3,4 |      |
| t <sub>PHL</sub> | Propagation Delay<br>A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub> | 5.0       | 1.5               | 4.0  | 8.0  | 1.0 | 10.0  | 1.0 | 9.0   | ns | 2-3,4 |      |
| t <sub>PZH</sub> | Output Enable Time  | 5.0       | 1.5               | 5.0  | 10.0 | 1.0 | 12.0  | 1.5 | 11.0  | ns | 2-5   |      |
| t <sub>PZL</sub> | Output Enable Time  | 5.0       | 1.5               | 5.5  | 10.0 | 1.0 | 13.0  | 1.5 | 12.0  | ns | 2-6   |      |
| t <sub>PHZ</sub> | Output Disable Time   | 5.0       | 1.5               | 5.5  | 10.0 | 1.0 | 12.0  | 1.0 | 11.0  | ns | 2-5   |      |
| t <sub>PLZ</sub> | Output Disable Time   | 5.0       | 2.0               | 5.0  | 10.0 | 1.0 | 12.0  | 1.5 | 11.0  | ns | 2-6   |      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

#### Capacitance

| Symbol           | Parameter                        | Тур  | Units | Conditions      |
|------------------|----------------------------------|------|-------|-----------------|
| C <sub>IN</sub>  | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$ |
| C <sub>1/O</sub> | Input/Output<br>Capacitance      | 15.0 | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub>  | Power Dissipation<br>Capacitance | 45.0 | pF    | $V_{CC} = 5.0V$ |



# 54AC/74AC251 • 54ACT/74ACT251 8-Input Multiplexer with TRI-STATE® Output

#### **General Description**

The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

#### **Features**

- Multifunctional capability
- On-chip select logic decoding
- Inverting and noninverting TRI-STATE outputs

AC Electrical Cinaracteristics: See Section 2 for

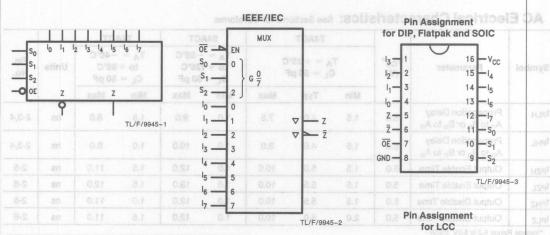
Symbol

- Outputs source/sink 24 mA
- 'ACT251 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC251: 5962-87692
  - 'ACT251: 5962-89599

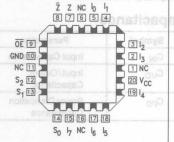
## Ordering Code: See Section 8

#### **Logic Symbols**

#### **Connection Diagrams**



| Pin Names  | Description  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|
| S <sub>0</sub> -S <sub>2</sub><br><del>OE</del><br>I <sub>0</sub> -I <sub>7</sub><br>Z<br><del>Z</del> | Select Inputs TRI-STATE Output Enable Input Multiplexer Inputs TRI-STATE Multiplexer Output Complementary TRI-STATE Multiplexer Output |  |  |  |  |  |  |



TL/F/9945-4

#### **Functional Description**

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs,  $S_0$ ,  $S_1$ ,  $S_2$ . Both true and complementary outputs are provided. The Output Enable input ( $\overline{OE}$ ) is active LOW. When it is activated, the logic function provided at the output is:

$$\begin{split} Z &= \overline{\mathsf{OE}} \bullet (\mathsf{I}_0 \bullet \overline{\mathsf{S}}_0 \bullet \overline{\mathsf{S}}_1 \bullet \overline{\mathsf{S}}_2 + \mathsf{I}_1 \bullet \mathsf{S}_0 \bullet \overline{\mathsf{S}}_1 \bullet \overline{\mathsf{S}}_2 + \\ & \mathsf{I}_2 \bullet \overline{\mathsf{S}}_0 \bullet \mathsf{S}_1 \bullet \overline{\mathsf{S}}_2 + \mathsf{I}_3 \bullet \mathsf{S}_0 \bullet \overline{\mathsf{S}}_1 \bullet \overline{\mathsf{S}}_2 + \\ & \mathsf{I}_4 \bullet \overline{\mathsf{S}}_0 \bullet \overline{\mathsf{S}}_1 \bullet \mathsf{S}_2 + \mathsf{I}_5 \bullet \mathsf{S}_0 \bullet \overline{\mathsf{S}}_1 \bullet \mathsf{S}_2 + \\ & \mathsf{I}_6 \bullet \overline{\mathsf{S}}_0 \bullet \mathsf{S}_1 \bullet \mathsf{S}_2 + \mathsf{I}_7 \bullet \mathsf{S}_0 \bullet \mathsf{S}_1 \bullet \mathsf{S}_2) \end{split}$$

When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

#### Truth Table its? mumixaM stuloedA

| police Sales | Inp            | uts            |                | Out               | puts |
|--------------|----------------|----------------|----------------|-------------------|------|
| OE           | S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> | ofu <b>Z</b> nisi | O\Z  |
| VO. H OF V   | X              | X              | X              | Z Z               | Z    |
| L            | L              | L              | (Si) finem     | To                | 10   |
| Ames +       | L              | L              | Н              | a.o. 1            | 11   |
|              | L              | Н              | L              | Ī <sub>2</sub>    | 12   |
| V8.0 + 50    | m Lan          | Н              | H              | Ī <sub>3</sub>    | 13   |
| Am Qs —      | Н              | LO             | Oi) Maure      | Ī <sub>4</sub>    | 14   |
| Am (S.+      | Н              | L              | H v            | Ī <sub>5</sub>    | 15   |
| L            | H Ve           | Н              | L              | Ī <sub>6</sub>    | 16   |
| Anna La Dal  | H Ve           | Н              | How            | Ī <sub>7</sub>    | 17   |

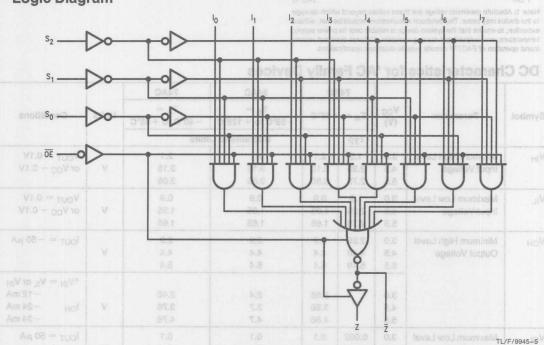
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| 3.0 | 0.36 | 0.50 | 0.44 | V | 0.1 | 24 mA | 12 mA | 13 mA

PDIP

#### Absolute Maximum Ratings (Note 1)

Supply Voltage (V<sub>CC</sub>)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| DC Input Diode Current (I <sub>IK</sub> ) |                              |
|---|------------------------------|
| $V_1 = -0.5V$                             | -20 mA                       |
| $V_I = V_{CC} + 0.5V$                     | + 20 mA                      |
| DC Input Voltage (V <sub>I</sub> )        | $-0.5$ V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK)             |                              |
| $V_{O} = -0.5V$                           | -20 mA                       |
| $V_O = V_{CC} + 0.5V$                     | + 20 mA                      |
|   |                              |

DC Output Voltage ( $V_O$ ) -0.5V to to  $V_{CC}+0.5V$  DC Output Source or Sink Current ( $I_O$ )  $\pm$  50 mA DC  $V_{CC}$  or Ground Current

per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ Junction Temperature ( $T_{J}$ ) CDIP  $175^{\circ}\text{C}$ 

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating and Solved and Conditions

| Supply Voltage (V <sub>CC</sub> )                  |                       |
|--|-----------------------|
| 'AC THE BUT MORE SO IN THE RELIGIO                 | 2.00 10 0.00          |
| ACI  | 4.5V to 5.5V          |
| Input Voltage (V <sub>I</sub> )                    | 0V to Vcc             |
| Output Voltage (V <sub>O</sub> )                   | 0V to V <sub>CC</sub> |
| Operating Temperature (T <sub>A</sub> )            |                       |
| 74AC/ACT   | -40°C to +85°C        |
| 54AC/ACT   | -55°C to +125°C       |
| Minimum Input Edge Rate (ΔV/Δt) 'AC Devices        |                       |
| V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> |                       |
| V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V                 | 125 mV/ns             |
| Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices       |                       |
| V <sub>IN</sub> from 0.8V to 2.0V                  |                       |
| Vcc @ 4.5V, 5.5V                                   | 125 mV/ns             |

#### **DC Characteristics for 'AC Family Devices**

| 144             |                                  |                 | 74                     | AC   | 54AC                             | 74AC                            |       |                           |
|-----------------|----------------------------------|-----------------|------------------------|------|----------------------------------|---------------------------------|-------|---------------------------|
| Symbol          | Parameter                        | V <sub>CC</sub> | T <sub>A</sub> = +25°C |      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                |
|                 |                                  |                 | Тур                    |      | Guaranteed L                     | imits                           |       |                           |
| VIH             | Minimum High Level               | 3.0             | 1.5                    | 2.1  | 2.1                              | 2.1                             |       | V <sub>OUT</sub> = 0.1V   |
|                 | Input Voltage                    | 4.5             | 2.25                   | 3.15 | 3.15                             | 3.15                            | V     | or V <sub>CC</sub> - 0.1V |
|                 | UUU                              | 5.5             | 2.75                   | 3.85 | 3.85                             | 3.85                            |       |                           |
| V <sub>IL</sub> | Maximum Low Level                | 3.0             | 1.5                    | 0.9  | 0.9                              | 0.9                             |       | V <sub>OUT</sub> = 0.1V   |
|                 | Input Voltage                    | 4.5             | 2.25                   | 1.35 | 1.35                             | 1.35                            | V     | or V <sub>CC</sub> - 0.1V |
|                 |                                  | 5.5             | 2.75                   | 1.65 | 1.65                             | 1.65                            |       |                           |
| V <sub>OH</sub> | Minimum High Level               | 3.0             | 2.99                   | 2.9  | 2.9                              | 2.9                             |       | $I_{OUT} = -50 \mu A$     |
| 011             | Output Voltage                   | 4.5             | 4.49                   | 4.4  | 4.4                              | 4.4                             | V     |                           |
|                 |                                  | 5.5             | 5.49                   | 5.4  | 5.4                              | 5.4                             |       |                           |
|                 |                                  |                 | 8                      |      |                                  |                                 |       | *VIN = VIL or VIH         |
|                 |                                  | 3.0             | 772                    | 2.56 | 2.4                              | 2.46                            |       | -12 mA                    |
|                 |                                  | 4.5             | Y                      | 3.86 | 3.7                              | 3.76                            | V     | I <sub>OH</sub> -24 mA    |
|                 |                                  | 5.5             |                        | 4.86 | 4.7                              | 4.76                            |       | -24 mA                    |
| VOL             | Maximum Low Level                | 3.0             | 0.002                  | 0.1  | 0.1                              | 0.1                             |       | $I_{OUT} = 50 \mu A$      |
|                 | Output Voltage                   | 4.5             | 0.001                  | 0.1  | 0.1                              | 0.1                             | V     | Please note:              |
|                 |                                  | 5.5             | 0.001                  | 0.1  | 0.1                              | 0.1                             |       |                           |
|                 |                                  | 1               |                        |      |                                  |                                 |       | *VIN = VIL or VIH         |
|                 |                                  | 3.0             |                        | 0.36 | 0.50                             | 0.44                            |       | 12 mA                     |
|                 |                                  | 4.5             |                        | 0.36 | 0.50                             | 0.44                            | V     | IOL 24 mA                 |
|                 |                                  | 5.5             |                        | 0.36 | 0.50                             | 0.44                            |       | 24 mA                     |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current | 5.5             |                        | ±0.1 | ±1.0                             | ±1.0                            | μΑ    | $V_I = V_{CC}$ , GND      |

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### 4

## DC Characteristics for 'AC Family Devices (Continued) Indiana (Continued)

|              |            | Parameter                     |                        | 0A7                    | 4AC        | 54AC                              | 74A      | 0                               | 100 |  |
|--------------|------------|-------------------------------|------------------------|------------------------|------------|-----------------------------------|----------|---------------------------------|-----|--|
| Symbol       | elin U     |                               | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |            | T <sub>A</sub> = -55°C to + 125°C |          | T <sub>A</sub> = -40°C to +85°C |     | Conditions   |
|              | Ct = 50 pF | 7                             | Тур                    | 13                     | Guaranteed | Limits                            |          |                                 |     |  |
| loz<br>4,8-9 | Max        | imum TRI-STATE®<br>ent        | 5.5                    | 3                      | ±0.5       | 0.01 ± 17.5                       | a.r ±5.0 |                                 | μА  | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , $V_{GND}$<br>$V_{O}$ = $V_{CC}$ , GND |
| IOLD         | †Mir       | nimum Dynamic                 | 5.5                    | 1                      | 1.0        | 50                                | 75       | 8                               | mA  | V <sub>OLD</sub> = 1.65V Max   |
| IOHD         | Outp       | out Current                   | 5.5                    |                        | 0.1        | -50                               | -75      |                                 | mA  | V <sub>OHD</sub> = 3.85V Min   |
| Icc          |            | imum Quiescent<br>ply Current | 5.5                    |                        | 8.0        | 160.0                             | 80.0     | 2                               | μА  | V <sub>IN</sub> = V <sub>CC</sub> or GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{IN}$  and  $I_{CC} @ 3.0V$  are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

#### DC Characteristics for 'ACT Family Devices

|                    | Parameter                          |                 | 74           | ACT          | 54ACT                            | 74ACT                           | sable Tim     | tenz Output Di   |
|--------------------|------------------------------------|-----------------|--------------|--------------|----------------------------------|---------------------------------|---------------|--|
| Symbol             |                                    | V <sub>CC</sub> |              | =<br>25°C    | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units         | Conditions   |
|                    | 8.5                                | 3.5             | Тур          | 0.0          | Guaranteed L                     | imits                           | VC 0+ US      | East Remail enadov!  |
| V <sub>IH</sub>    | Minimum High Leve<br>Input Voltage | 4.5<br>5.5      | 1.5<br>1.5   | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | V             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>    | Maximum Low Level<br>Input Voltage |                 | 1.5<br>1.5   | 0.8          | 0.8<br>0.8                       | 0.8                             | ٧             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub>    | Minimum High Level Output Voltage  | 4.5<br>5.5      | 4.49<br>5.49 | 4.4<br>5.4   | 5.4                              | 4.4<br>5.4                      | V             | $I_{OUT} = -50 \mu\text{A}$  |
|                    | Risk est                           | 4.5<br>5.5      | M<br>M       | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | valeV na      | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| V <sub>OL</sub>    | Maximum Low Level Output Voltage   | el 4.5<br>5.5   | 0.001        | 0.1          | 0.1<br>0.1 <sub>a</sub>          | 0.1<br>0.1                      | Z<br>on Velay | I <sub>OUT</sub> = 50 μA   |
|                    | an 0,81                            | 4.5             |              | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | on Delay      | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub> SS | Maximum Input<br>Leakage Current   | 5.5             | 17           | ±0.1         | ±1.0                             | ± 1.0                           | μΑ            | $V_I = V_{CC}$ , GND   |
| loz                | Maximum TRI-STA<br>Current         | TE® 5.5         | ř            | ±0.5         | ±10.0                            | ±5.0                            | μΑ            | $V_{I} = V_{IL}, V_{IH}$<br>$V_{O} = V_{CC}, GND$  |
| ГССТ               | Maximum I <sub>CC</sub> /Input     | 5.5             | 0.6          | 0.1          | 1.6                              | 1.5                             | mA            | $V_{\rm I} = V_{\rm CC} - 2.1V$  |
| lold               | †Minimum Dynamic                   | 5.5             | 7            | 1.0          | 50 0.8                           | 75                              | mA            | V <sub>OLD</sub> = 1.65V Max   |
| IOHD               | Output Current                     | 5.5             |              |              | -50                              | -75                             | mA            | V <sub>OHD</sub> = 3.85V Min   |
| lcc                | Maximum Quiescer<br>Supply Current | 5.5             |              | 8.0          | 160.0                            | 80.0                            | μА            | V <sub>IN</sub> = V <sub>CC</sub> or GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics: See Section 2 for waveforms

| Symbol               |  | CAM               |  | 74AC        |              | OA 54   | AC           | 74   | AC           |             |             |
|----------------------|--|-------------------|--|-------------|--------------|---|--------------|--|--------------|-------------|-------------|
|                      | Parameter                                      | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             |              | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |              | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ |              | Units       | Fig.<br>No. |
|                      | - (30) V                                       |                   | Min  | Тур         | Max          | Min   | Max          | Min  | Max          | Score L. A. |             |
| t <sub>PLH</sub>     | Propagation Delay $S_n$ to Z or $\overline{Z}$ | 3.3<br>5.0        | 1.5<br>1.5                                       | 11.5<br>8.5 | 17.5<br>12.5 | 1.0   | 21.0<br>15.5 | 1.5<br>1.5   | 19.0<br>13.5 | ns          | 2-3,4       |
| t <sub>PHL</sub> van | Propagation Delay $S_n$ to Z or $\overline{Z}$ | 3.3<br>5.0        | 1.5<br>1.5                                       | 11.0        | 17.5<br>12.5 | 1.0   | 21.0<br>15.5 | 1.5<br>1.5   | 19.0<br>13.5 | ns          | 2-3,4       |
| tPLH                 | Propagation Delay $I_n$ to Z or $\overline{Z}$ | 3.3<br>5.0        | 1.5<br>1.5                                       | 10.0<br>7.0 | 14.0<br>10.0 | 1.0   | 17.0<br>12.0 | 1.5<br>1.5   | 15.5<br>11.0 | ns          | 2-3,4       |
| t <sub>PHL</sub>     | Propagation Delay $I_n$ to Z or $\overline{Z}$ | 3.3<br>5.0        | 1.5<br>1.5                                       | 9.0<br>6.5  | 14.0<br>10.0 | 1.0<br>1.0  | 16.5<br>12.0 | 1.5<br>1.5   | 15.5<br>11.0 | ns          | 2-3,4       |
| t <sub>PZH</sub>     | Output Enable Time                             | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.5<br>5.5  | 11.0         | 1.0   | 13.0<br>10.0 | 1.5<br>1.5   | 12.0<br>9.0  | ns          | 2-5         |
| t <sub>PZL</sub>     | Output Enable Time                             | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.5<br>5.5  | 11.0         | 1.0   | 13.0<br>10.0 | 1.5<br>1.5   | 12.0<br>9.0  | ns          | 2-6         |
| t <sub>PHZ</sub>     | Output Disable Time                            | 3.3<br>5.0        | 1.5<br>1.5                                       | 8.5<br>7.0  | 11.5<br>9.5  | 3.5<br>2.5  | 14.0<br>11.0 | 1.5<br>1.5   | 13.0<br>10.0 | ns          | 2-5         |
| t <sub>PLZ</sub>     | Output Disable Time                            | 3.3<br>5.0        | 1.5  | 7.0<br>5.5  | 11.0         | 4.0<br>3.0  | 13.0<br>10.0 | 1.5<br>1.5   | 12.0<br>8.5  | ns          | 2-6         |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

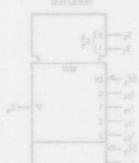
#### AC Electrical Characteristics: See Section 2 for waveforms

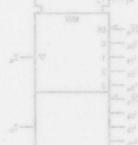
|                  | - 00V 10                                       | 8,0               |     | 74ACT                                      | 8.0 544 | 54ACT  T <sub>A</sub> = -55°C  to +125°C  C <sub>L</sub> = 50 pF |       | $74ACT$ $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 \text{ pF}$ |   | Fig.  |
|------------------|--|-------------------|-----|--|---------|--|-------|--|---|-------|
| Symbol           | Parameter                                      | V <sub>CC</sub> * |     | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ | to +1   |  |       |  |   |       |
|                  | A = MA.  | 87.8              | Min | Тур Мах                                    | Min     | Max  | Min   | Max  |   |       |
| tpLH             | Propagation Delay $S_n$ to Z or $\overline{Z}$ | 5.0               | 2.5 | 7.0 15.5                                   | 1.0     | 18.5   | 2.0   | 17.0   | ns  | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay $S_n$ to Z or $\overline{Z}$ | 5.0               | 2.5 | 7.5 16.5                                   | 1.0     | 19.5   | 2.5   | 18.5   | ns  | 2-3,4 |
| tpLH             | Propagation Delay $I_n$ to Z or $\overline{Z}$ | 5.0               | 2.5 | 5.5 12.0                                   | 1.0     | 14.0   | 2.0   | 13.0   | ns  | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay $I_n$ to Z or $\overline{Z}$ | 5.0               | 2.5 | 6.5 12.5                                   | 1.0     | 15.0   | 2.5   | 14.0   | ns  | 2-3,4 |
| <sup>t</sup> PZH | Output Enable Time                             | 5.0               | 1.5 | 5.0 8.5                                    | 1.0     | 10.0   | 1.5 A | 9.0  | ns  | 2-5   |
| t <sub>PZL</sub> | Output Enable Time                             | 5.0               | 1.5 | 4.5 8.5                                    | 1.0     | 10.0   | 1.5   | 9.5  | ns  | 2-6   |
| t <sub>PHZ</sub> | Output Disable Time                            | 5.0               | 2.0 | 6.0 00 12.0                                | 1.0     | 13.5   | 2.0   | 13.0   | ns  | 2-5   |
| t <sub>PLZ</sub> | Output Disable Time                            | 5.0               | 1.5 | 4.5 8.5                                    | 1.0     | 9.5  | 1.5   | 9.0  | ns  | 2-6   |
| *1/-l4 F         | 2  | 0.08              |     | 0.001                                      | 0.8     | 0.6  | 11,10 | MILESPENDENCE LANGE  | DATE OF THE PARTY | 100   |

\*Voltage Range 5.0 is 5.0V ±0.5V

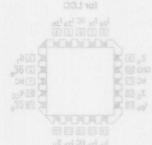
| 103             |                                  | 7.0    | ΡI      | VCC - 5.0V      | _            |
|-----------------|----------------------------------|--------|---------|-----------------|--------------|
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 70.0   | OA pF\\ | $V_{CC} = 5.0V$ | 54AC/74AC    |
|                 | E® Outputs                       | AT2-IA | T ridiw | Multiplexer     | Dual 4-Input |













# 54AC/74AC253 • 54ACT/74ACT253 Dual 4-Input Multiplexer with TRI-STATE® Outputs

#### **General Description**

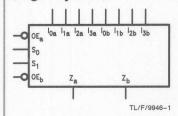
The 'AC/'ACT253 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable  $(\overline{OE})$  inputs, allowing the outputs to interface directly with bus oriented systems.

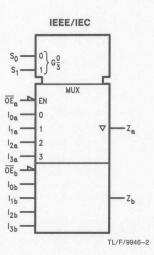
#### **Features**

- Multifunction capability
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT253 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC253: 5962-87693
  - 'ACT253: 5962-87761

#### Ordering Code: See Section 8

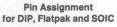
#### **Logic Symbols**

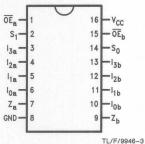




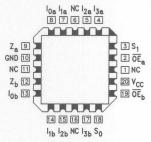
| Pin Names                        | Description                |  |  |  |  |  |
|----------------------------------|----------------------------|--|--|--|--|--|
| I <sub>0a</sub> -I <sub>3a</sub> | Side A Data Inputs         |  |  |  |  |  |
| I <sub>0b</sub> -I <sub>3b</sub> | Side B Data Inputs         |  |  |  |  |  |
| S <sub>0</sub> , S <sub>1</sub>  | Common Select Inputs       |  |  |  |  |  |
| ŌĒa                              | Side A Output Enable Input |  |  |  |  |  |
| ŌĒb                              | Side B Output Enable Input |  |  |  |  |  |
| $Z_a, Z_b$                       | TRI-STATE Outputs          |  |  |  |  |  |

#### **Connection Diagrams**





# Pin Assignment for LCC



TL/F/9946-4

#### Functional Description

The 'AC/'ACT253 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S<sub>0</sub>, S<sub>1</sub>). The 4-input multiplexers have individual Output Enable ( $\overline{\text{OE}}_a, \overline{\text{OE}}_b$ ) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$\begin{split} Z_{\mathbf{a}} &= \overline{OE}_{\mathbf{a}} \bullet (I_{0\mathbf{a}} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1\mathbf{a}} \bullet \overline{S}_{1} \bullet S_{0} + \\ & I_{2\mathbf{a}} \bullet S_{1} \bullet \overline{S}_{0} + I_{3\mathbf{a}} \bullet S_{1} \bullet S_{0}) \end{split}$$

$$Z_{\mathbf{b}} &= \overline{OE}_{\mathbf{b}} \bullet (I_{0\mathbf{b}} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1\mathbf{b}} \bullet \overline{S}_{1} \bullet S_{0} + \\ \end{split}$$

12b • S1 • S0 + 13b • S1 • S0)

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

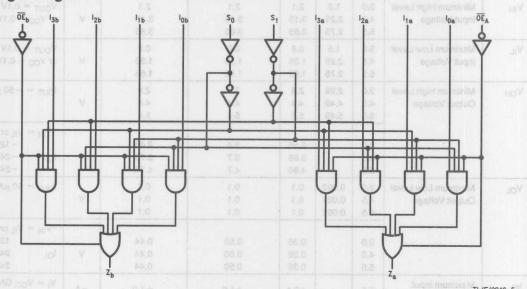
#### **Truth Table**

| Select<br>Inputs |                | .02            | Data | Inputs          | Output<br>Enable | Outputs  |       |
|------------------|----------------|----------------|------|-----------------|------------------|----------|-------|
| S <sub>0</sub>   | S <sub>1</sub> | I <sub>0</sub> | 11   | VI <sub>2</sub> | l <sub>3</sub>   | ŌĒ       | ZAm   |
| an X as          | X              | X              | X    | X               | X                | VOH® 4.8 | ZOTO  |
| L                | L              | L              | X    | X               | X                | L        | L     |
| L                | L              | Н              | X    | X               | X                | L        | HOTE  |
| Н                | L              | X              | L    | X               | X                | L        | F5.0  |
| Н                | L              | X              | Н    | X               | X                | L        | H     |
| L                | Н              | X              | X    | L               | X                | L        | Lalan |
| L                | Н              | X              | Х    | Н               | X                | L        | H     |
| Н                | Н              | X              | X    | X               | L                | L        | L     |
| Н                | Н              | X              | X    | X               | Н                | L        | . Н.  |

Address Inputs So and S1 are common to both sections.

- H = HIGH Voltage Level L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>)

DC Input Diode Current (IIK)  $V_1 = -0.5V$ 

 $V_I = V_{CC} + 0.5V$ DC Input Voltage (V<sub>I</sub>) -0.5V to V<sub>CC</sub> + 0.5V

DC Output Diode Current (IOK)

-20 mA  $V_0 = -0.5V$  $V_O = V_{CC} + 0.5V$ +20 mA DC Output Voltage (VO) -0.5V to to V<sub>CC</sub> + 0.5V

DC Output Source or Sink Current (IO)

±50 mA

DC V<sub>CC</sub> or Ground Current per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>)

±50 mA -65°C to +150°C

Storage Temperature (TSTG) Junction Temperature (T<sub>J</sub>)

175°C CDIP PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>)

'AC Elos eldenel hughe 2.0V to 6.0V 'ACT Input Voltage (V<sub>I</sub>) OV to VCC Output Voltage (Vo)

Operating Temperature (T<sub>A</sub>)

-40°C to +85°C 74AC/ACT 54AC/ACT -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

VIN from 30% to 70% of VCC 125 mV/ns VCC @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices VIN from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

DC Characteristics for 'AC Family Devices

|                        |                                      |                        | 74.                     | AC                   | 54AC                             | 74AC                            | le le    | aJ ageticV HBIH = H  |
|------------------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|----------|--|
| Symbol                 | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units    | Conditions   |
|                        |                                      |                        | Тур                     |                      | Guaranteed L                     | imits                           | P972.050 | nelCoine I   |
| V <sub>IH</sub>        | Minimum High Level                   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | v V      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>        | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | V        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| VoH                    | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V        | $I_{OUT} = -50 \mu\text{A}$  |
|                        |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | V        | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &- 12 \mbox{ mA} \\ I_{OH} &- 24 \mbox{ mA} \\ &- 24 \mbox{ mA} \\ \end{tabular}$ |
| V <sub>OL</sub>        | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V        | Ι <sub>ΟUT</sub> = 50 μΑ   |
|                        |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | V        | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA   |
| I <sub>IN-8488/3</sub> | Maximum Input<br>Leakage Current     | 5.5                    | Lien bluede             | ±0.1                 | ±1.0                             | ±1.0                            | μΑ       | $V_{I} = V_{CC}$ , GND   |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued)

| Symbol | DAST                             |                        | 74                     | AC   |                                   | 54AC         | 74AC                            |       |  |  |
|--------|----------------------------------|------------------------|------------------------|------|-----------------------------------|--------------|---------------------------------|-------|--|--|
|        | Parameter                        | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |      | T <sub>A</sub> = -55°C to + 125°C |              | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                                   |  |
|        | C <sub>L</sub> = 50 pF           | 90                     | Тур                    | 9    |                                   | Guaranteed L | imits                           |       |  |  |
| loz    | Maximum TRI-STATE®               | 3690                   | d n                    | 08   | ralit                             | GyT nil      |                                 |       | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$           |  |
|        | Current axt o.s                  | 5.5                    |                        | ±0.5 | 15.6                              | ±10.0        | ±5.0                            | μА    | $V_I = V_{CC}$ , GND<br>$V_O = V_{CC}$ , GND |  |
| IOLD   | †Minimum Dynamic                 | 5.5                    | 8 6                    |      | 0.81                              | 50           | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max                 |  |
| IOHD   | Output Current                   | 5.5                    | 1 0                    | 1    | 11.0                              | <b>-50</b>   | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min                 |  |
| Icc    | Maximum Quiescent Supply Current | 5.5                    | 1 0                    | 8.0  | 14.5                              | 160.0        | 80.0                            | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND     |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

#### DC Characteristics for 'ACT Family Devices

| Symbol          | 1.0 7.0                             | 0                      | 74                | ACT          | 54ACT                            | 74ACT                           |                        |   |
|-----------------|-------------------------------------|------------------------|-------------------|--------------|----------------------------------|---------------------------------|------------------------|---|
|                 | Parameter 2.7                       | V <sub>CC</sub><br>(V) |                   |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                  | Conditions  |
| 2-6             | 1.0 9.0 ns                          | 8                      | Тур               |              | Guaranteed Li                    | mits                            | eldsaiQ                | tel2 Output   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5        | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | 0.0 V VE.<br>8.0 ± VO. | $V_{OUT} = 0.1V$<br>or $V_{CC} = 0.1V$  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5        | 0.8          | 0.8                              | 0.8<br>0.8                      | V                      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimum High Level Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49      | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V                      | $I_{OUT} = -50 \mu\text{A}$   |
| Fig.            | to + 85°C Units  Cu = 50 pF         | 4.5<br>5.5             | + 128°1<br>= 50 p | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V                      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |
| Vol             | Maximum Low Level Output Voltage    | 4.5<br>5.5             | 0.001<br>0.001    | 0.1          | 0.1<br>0.1                       | 0.1<br>0.1                      | od Ville               | ΙΟυΤ = 50 μΑ  |
| 2-8,4           | en 8.5 8.5                          | 4.5                    | 91                | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | V .                    | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| IN              | Maximum Input<br>Leakage Current    | 5.5                    | 12                | ±0.1         | ±1.0                             | ±1.0                            | μΑ                     | V <sub>I</sub> = V <sub>CC</sub> , GND  |
| loz             | Maximum TRI-STATE® Current          | 5.5                    | 21                | ±0.5         | ±10.0                            | ±5.0                            | μА                     | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |
| ГССТ            | Maximum<br>I <sub>CC</sub> /Input   | 5.5                    | 0.6               | 0.7          | 8 1.6                            | 0.1.5 emil                      | e mA                   | $V_{\rm I} = V_{\rm CC} - 2.1V$   |
| IOLD            | †Minimum Dynamic                    | 5.5                    |                   |              | 50                               | 75                              | mA                     | V <sub>OLD</sub> = 1.65V Max  |
| Iонр            | Output Current 0.8                  | 5.5                    | 8                 |              | -50                              | 0.6 <sub>75</sub> 9011          | mA                     | V <sub>OHD</sub> = 3.85V Min  |
| Icc             | Maximum Quiescent<br>Supply Current | 5.5                    |                   | 8.0          | 160.0                            | 80.0                            | μΑ                     | V <sub>IN</sub> = V <sub>CC</sub> or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: Icc for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{\text{IN}}$  and  $I_{\text{CC}}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\text{CC}}$ .

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# AC Electrical Characteristics: See Section 2 for waveforms

|   |   | CART       |            | 74AC   |              | 54   | AC           | 74   | 4AC          |       |             |
|---|---|------------|------------|--|--------------|--|--------------|--|--------------|-------|-------------|
| Symbol                                      | Parameter 2788  | VCC        |            | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |              | $T_{A} = -40^{\circ}C$ $to +85^{\circ}C$ $C_{L} = 50 \text{ pF}$ |              | Units | Fig.<br>No. |
| N/ (OE) = V <sub>II</sub> , V <sub>IR</sub> |   | Min        | Тур        | Max  | Min          | Max  | Min          | Max  | mixsM        | SC    |             |
| t <sub>PLH</sub>                            | Propagation Delay<br>S <sub>n</sub> to Z <sub>n</sub> | 3.3<br>5.0 | 2.0<br>2.0 | 8.5<br>6.5                                       | 15.5<br>11.0 | 1.0  | 19.5<br>13.5 | 2.0<br>1.5   | 17.5<br>12.5 | ns    | 2-3,4       |
| tPHL<br>niM V88.8                           | Propagation Delay<br>S <sub>n</sub> to Z <sub>n</sub> | 3.3<br>5.0 | 2.5<br>2.0 | 9.5<br>7.0                                       | 16.0<br>11.5 | 1.0  | 20.0<br>15.0 | 2.0<br>1.5   | 18.0<br>13.0 | ns    | 2-3,4       |
| t <sub>PLH</sub> 33                         | Propagation Delay                                     | 3.3<br>5.0 | 1.5<br>1.5 | 7.0<br>5.5                                       | 14.5<br>10.0 | 1.0<br>1.0   | 19.0<br>13.0 | 1.5<br>1.5   | 17.0<br>11.5 | ns    | 2-3,4       |
| t <sub>PHL</sub>                            | Propagation Delay                                     | 3.3<br>5.0 | 2.0<br>1.5 | 7.5<br>5.5                                       | 13.0<br>9.5  | 1.0<br>1.0   | 16.0<br>12.0 | 1.5<br>1.5   | 15.0<br>11.0 | ns ns | 2-3,4       |
| t <sub>PZH</sub>                            | Output Enable Time                                    | 3.3<br>5.0 | 1.5<br>1.5 | 4.5<br>3.5                                       | 8.0<br>6.0   | 1.0<br>1.0   | 9.5<br>7.0   | 1.0  | 8.5<br>6.5   | ns    | 2-5         |
| t <sub>PZL</sub>                            | Output Enable Time                                    | 3.3<br>5.0 | 1.5<br>1.5 | 5.0<br>3.5                                       | 8.0<br>6.0   | 1.0  | 10.0<br>7.5  | 1.0  | 9.0<br>7.0   | ns    | 2-6         |
| t <sub>PHZ</sub>                            | Output Disable Time                                   | 3.3<br>5.0 | 2.0        | 5.5<br>5.0                                       | 9.5<br>8.0   | 1.0  | 11.0<br>9.5  | 1.5<br>1.5   | 10.0         | ns    | 2-5         |
| t <sub>PLZ</sub>                            | Output Disable Time                                   | 3.3<br>5.0 | 1.5<br>1.5 | 5.0<br>4.0                                       | 8.0<br>7.0   | 1.0  | 9.5<br>8.0   | 1.0<br>1.0   | 9.0<br>7.5   | ns    | 2-6         |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

#### AC Electrical Characteristics: See Section 2 for waveforms

|                        | Parameter   | 4,4               |     | 74ACT  |      | 54     | ACT  | 74  | ACT  | uminiN4 | ноУ         |
|------------------------|---|-------------------|-----|--|------|--------|--|-----|--|---------|-------------|
| Symbol                 |   | V <sub>CC</sub> * |     | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |      |        | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |         | Fig.<br>No. |
| Am 52-                 | HO! V   | 4.76              | Min | Тур  | Max  | Min    | Max  | Min | Max  |         |             |
| t <sub>PLH</sub> Aq 03 | Propagation Delay<br>S <sub>n</sub> to Z <sub>n</sub> | 5.0               | 2.0 | 7.0  | 11.5 | 1.0    | 14.5   | 2.0 | 13.0   | ns      | 2-3,4       |
| t <sub>PHL</sub>       | Propagation Delay<br>S <sub>n</sub> to Z <sub>n</sub> | 5.0               | 3.0 | 7.5  | 13.0 | 8.01.0 | 16.0   | 2.5 | 14.5   | ns      | 2-3,4       |
| t <sub>PLH</sub>       | Propagation Delay                                     | 5.0               | 2.5 | 5.5  | 10.0 | 1.0    | 12.0   | 2.0 | 11.0   | ns      | 2-3,4       |
| t <sub>PHL</sub>       | Propagation Delay                                     | 5.0               | 3.5 | 6.5  | 11.0 | 1.0    | 13.5   | 3.0 | 12.5   | ns      | 2-3,4       |
| t <sub>PZH</sub>       | Output Enable Time                                    | 5.0               | 2.0 | 4.5  | 7.5  | 1.0    | 9.5  | 1.5 | 8.5  | ns      | 2-5         |
| tpZL                   | Output Enable Time                                    | 5.0               | 2.0 | 5.0  | 8.0  | 1.0    | 9.5  | 1.5 | 9.0  | ns      | 2-6         |
| t <sub>PHZ</sub>       | Output Disable Time                                   | 5.0               | 3.0 | 6.0  | 9.5  | 1.0    | 11.0   | 2.5 | 10.0   | ns      | 2-5         |
| tPLZ                   | Output Disable Time                                   | 5.0               | 2.5 | 4.5  | 7.5  | 1.0    | 9.0  | 2.0 | 8.5  | ns      | 2-6         |

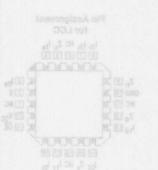
\*Voltage Range 5.0 is 5.0V  $\pm 0.5 \text{V}$ 

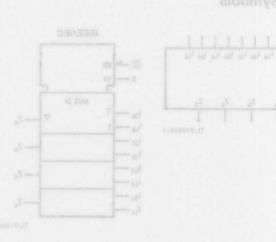
#### Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             | hannime 2       |
|-----------------|----------------------------------|------|-------|------------------------|-----------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        | OUTOOM HOO INSE |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 50.0 | TO pF | V <sub>CC</sub> = 5.0V | AC/74AC         |

M Noninverting TRI-STATE outputs a Outputs source/sink 24 mA a 'ACT257 has TTL-compatible inputs







| Data Inputs from Source 1 |  |  |  |
|---------------------------|--|--|--|
|                           |  |  |  |



# 54AC/74AC257•54ACT/74ACT257 Quad 2-Input Multiplexer with TRI-STATE® Outputs

#### **General Description**

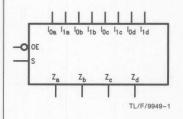
The 'AC/'ACT257 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable (OE) input, allowing the outputs to interface directly with bus-oriented systems.

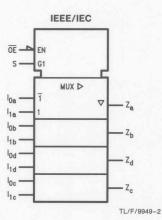
#### **Features**

- Multiplexer expansion by tying outputs together
- Noninverting TRI-STATE outputs
- Outputs source/sink 24 mA
- 'ACT257 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC257: 5962-88703
  - 'ACT257: 5962-89689

#### Ordering Code: See Section 8

#### **Logic Symbols**

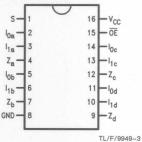




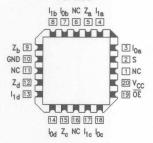
| Pin Names                        | Description                   |  |  |  |
|----------------------------------|-------------------------------|--|--|--|
| S                                | Common Data Select Input      |  |  |  |
| ŌĒ                               | TRI-STATE Output Enable Input |  |  |  |
| loa-lod                          | Data Inputs from Source 0     |  |  |  |
| l <sub>1a</sub> -l <sub>1d</sub> | Data Inputs from Source 1     |  |  |  |
| $Z_a - Z_d$                      | TRI-STATE Multiplexer Outputs |  |  |  |

#### **Connection Diagrams**

#### Pin Assignment for DIP, Flatpak and SOIC



## Pin Assignment for LCC



TL/F/9949-4

#### Functional Description

The 'AC/'ACT257 is guad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the lox inputs are selected and when Select is HIGH, the I<sub>1x</sub> inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \cdot (1_{1a} \cdot S + I_{0a} \cdot \overline{S})$$

$$Z_b = \overline{OE} \bullet (1_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$Z_c = \overline{OE} \cdot (1_{1c} \cdot S + I_{0c} \cdot \overline{S})$$

$$Z_d = \overline{OE} \cdot (1_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enable (OE) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maxi-

mum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

#### **Truth Table**

| Output<br>Enable | Select<br>Input |          | ata<br>puts | Outputs        |  |  |
|------------------|-----------------|----------|-------------|----------------|--|--|
| ŌĒ               | S               | lo.      | 14          |                |  |  |
| Am 0SH           | X               | X        | X           | /a.0 - Z oV    |  |  |
| Am OSL+          | Н               | X        | 0.53        | + ooV E oV     |  |  |
| VecJ+0.5V        | V8.0 H          | X        | (oVHeps     | DO Outhut Volt |  |  |
| Am oaL           | L (ol) 1        | k Claren | Ce X Sin    | OC Outbut Sou  |  |  |
| L                | L               | Hime     | X           | OC VeH or Gro  |  |  |

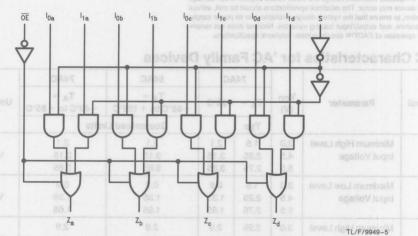
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| Supply Voltage (V <sub>CC</sub> )                     | misto               | -0.5V to 7.0V          | 'ACT              |
|---|---------------------|------------------------|-------------------|
| DC Input Diode Current (I <sub>IK</sub> )             |                     |                        | Input V           |
| $V_{I} = -0.5V$ $V_{I} = V_{CC} + 0.5V$               |                     | -20 mA<br>+20 mA       | Output            |
| DC Input Voltage (V <sub>I</sub> )                    | -0.5V to            | V <sub>CC</sub> +0.5V  | Operat<br>74A0    |
| DC Output Diode Current (IOK)                         |                     |                        | 54A0              |
| $V_0 = -0.5V$   |                     | -20 mA                 | Minimu            |
| $V_O = V_{CC} + 0.5V$                                 |                     | + 20 mA                | 'AC I             |
| DC Output Voltage (V <sub>O</sub> )                   | -0.5V to            | V <sub>CC</sub> + 0.5V | V <sub>IN</sub> f |
| DC Output Source or Sink Current                      | t (I <sub>O</sub> ) | ±50 mA                 | Vcc               |
| DC V <sub>CC</sub> or Ground Current                  |                     |                        | Minimu            |
| Per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) |                     | ±50 mA                 | 'ACT              |
| Storage Temperature (T <sub>STG</sub> )               | -65°                | C to +150°C            | V <sub>IN</sub> f |
| Junction Temperature (T,j)                            |                     |                        | VCC               |
| CDIP  |                     | 175°C                  |                   |
| PDIP  |                     | 140°C                  |                   |
|   |                     |                        |                   |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

| 2.0V to 6.0V<br>4.5V to 5.5V   |
|--|
| 0V to V <sub>CC</sub>  |
| of a column OV to V <sub>CC</sub>  |
| -40°C to +85°C<br>-55°C to +125°C  |
| 30 = 35<br>30 = 35<br>30 = 35<br>125 mV/ns                                   |
| bend fund of set many<br>began find a of benot<br>et eno fud la<br>125 mV/ns |
|  |

#### **DC Characteristics for 'AC Family Devices**

|                 | 2,                                   |                        | 74.                     | AC                   | 54AC                             | 74AC                            |                 |  |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-----------------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units           | Conditions   |  |
|                 |                                      |                        | Тур                     |                      | Guaranteed L                     | imits                           |                 |  |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | ٧               | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | ٧               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VoH             | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | etts e V. serie | $I_{OUT} = -50 \mu\text{A}$  |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | ٧               | $*V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ m/s}$ $I_{OH} - 24 \text{ m/s}$ $-24 \text{ m/s}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | ٧               | I <sub>OUT</sub> = 50 μA   |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | V               | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $12 \text{ mA}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$     |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μΑ              | $V_I = V_{CC}$ , GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| 1            |                                      | 1.1 |      |        | 00 0 10 1 120 0 | 1 10 0 10 1 00 0 |                 |   |
|--------------|--------------------------------------|-----|------|--------|-----------------|------------------|-----------------|---|
|              | CL = 50 pF                           |     | Тур  | 8 = 10 | Guaranteed      | Limits           |                 |   |
| loz          | Maximum TRI-STATE<br>Leakage Current | 5.5 | 8.0  | ±0.5   | ± 10.0          | ±5.0             | μΑ<br>μου Delay | $\begin{aligned} &V_{I}\left(\text{OE}\right) = V_{IL}, V_{IH} \\ &V_{I} = V_{CC}, \text{GND} \\ &V_{O} = V_{CC}, \text{GND} \end{aligned}$ |
| IOLD         | †Minimum Dynamic                     | 5.5 | 8.5  | 0,     | 50              | 75               | mA              | V <sub>OLD</sub> = 1.65V Max  |
| IOHD         | Output Current                       | 5.5 | 14.5 | 0,1    | -50             | -75              | mA              | V <sub>OHD</sub> = 3.85V Min  |
| Icc<br>A.S.S | Maximum Quiescent<br>Supply Current  | 5.5 | 14.5 | 8.0    | 2160.0          | 80.0             | μΑ              | V <sub>IN</sub> = V <sub>CC</sub> or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.
I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### **DC Characteristics for 'ACT Family Devices**

|                 | en 0.07                              | 12                     | 74/            | ACT          | 54ACT                            | 74ACT                           | eldsalC              | IndinO - 2Het   |  |
|-----------------|--------------------------------------|------------------------|----------------|--------------|----------------------------------|---------------------------------|----------------------|---|--|
| Symbol          | Parameter 0.9                        | V <sub>CC</sub><br>(V) | TA =           | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                | Conditions  |  |
|                 | 0.8                                  | -1                     | Тур            | 4814         | e a t va                         | No. 0.12 appears as other?      |                      |   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5     | 2.0<br>2.0   | 2.0<br>2.0                       | 2.0<br>2.0                      | 3.0 VVO.             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| VIL             | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5            | 0.8          | 0.8                              | 0.8<br>0.8                      | ٧                    | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level Output Voltage    | 4.5<br>5.5             | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V                    | $I_{OUT} = -50 \mu\text{A}$   |  |
| 5,5-5           | L = 50 pF<br>7.6 ns                  | 4.5<br>5.5             | 7q 0           | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | eG <b>V</b> oits     | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1<br>0.1                      | eG V <sub>oits</sub> | $I_{OUT} = 50 \mu A$  |  |
| 2,0,4           | an 8,01                              | 4.5<br>5.5             | 0,11           | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44                            | sQ noits             | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{1}V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ |  |
| IIN             | Maximum Input<br>Leakage Current     | 5.5                    | 5.11           | ±0.1         | 8.01±10.5                        | ±1.0                            | μΑ                   | $V_1 = V_{CC}$ , GND  |  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    | 8.6            | ±0.5         | ±10.0                            | ±5.0                            | μΑ                   | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| Ісст            | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6            | 0.1          | 0.0 1.6 8.8                      | 0.1.5 amil                      | mA                   | $V_{\rm I} = V_{\rm CC} - 2.1V$   |  |
| IOLD            | †Minimum Dynamic                     | 5.5                    | 9:0            | 0.4          | 50                               | 75                              | mA                   | V <sub>OLD</sub> = 1.65V Max  |  |
| IOHD            | Output Current                       | 5.5                    |                |              | -50                              | -75                             | mA                   | V <sub>OHD</sub> = 3.85V Min  |  |
| lcc             | Maximum Quiescent<br>Supply Current  | 5.5                    |                | 8.0          | 160.0                            | 80.0                            | μΑ                   | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics: See Section 2 for waveforms

| Symbol            |  | 7480              |            | 74AC                                | 8  | 54A        | C            | 74                     | AC           |              |       |
|-------------------|--|-------------------|------------|-------------------------------------|--|------------|--------------|------------------------|--------------|--------------|-------|
|                   | Parameter                                | V <sub>CC</sub> * |            | A = +25°C<br>C <sub>L</sub> = 50 pF | $T_{A} = -55^{\circ}C$ to +125°C $C_{L} = 50 \text{ pF}$ |            | (v) to +     | −40°C<br>85°C<br>50 pF | Units        | Fig.<br>No.  |       |
| Propagation Delay |  | 3.3<br>5.0        | 1.5<br>1.5 |                                     | 3.5  | 1.0        | 11.0         | 1.0                    | 9.0<br>7.0   | ns           | 2-3,4 |
| t <sub>PHL</sub>  | Propagation Delay                        | 3.3<br>5.0        | 1.5<br>1.5 |                                     | 3.5  | 1.0<br>1.0 | 11.0         | 1.0                    | 9.0<br>7.0   | ns           | 2-3,4 |
| t <sub>PLH</sub>  | Propagation Delay<br>S to Z <sub>n</sub> | 3.3<br>5.0        | 1.5<br>1.5 |                                     | 0.5<br>7.5   | 1.0<br>1.0 | 14.5<br>11.0 | 1.5                    | 11.5<br>8.5  | ns ns        | 2-3,4 |
| t <sub>PHL</sub>  | Propagation Delay<br>S to Z <sub>n</sub> | 3.3<br>5.0        | 1.5<br>1.5 |                                     | 0.5<br>7.5   | 1.00.8     | 14.5<br>11.0 | 1.5                    | 11.5<br>8.5  | ns           | 2-3,4 |
| t <sub>PZH</sub>  | Output Enable Time                       | 3.3<br>5.0        | 1.5<br>1.5 |                                     | 9.5<br>7.5   | 1.0        | 13.0         | 1.0                    | 10.5<br>8.5  | ns ool one i | 2-5   |
| t <sub>PZL</sub>  | Output Enable Time                       | 3.3<br>5.0        | 1.5<br>1.5 |                                     | 9.0  | 1.0        | 11.0<br>9.5  | 1.0<br>1.0             | 10.0<br>9.5  | ns           | 2-6   |
| t <sub>PHZ</sub>  | Output Disable Time                      | 3.3<br>5.0        | 1.5<br>1.5 |                                     | 0.0  | 1.0        | 13.0<br>11.0 | 1.0<br>1.0             | 11.0<br>10.0 | ns           | 2-5   |
| t <sub>PLZ</sub>  | Output Disable Time                      | 3.3<br>5.0        | 1.5        |                                     | 9.0  | 1.0        | 10.5<br>9.5  | 1.0                    | 10.0<br>9.0  | ns           | 2-6   |

\*Voltage Range 3.3 is 3.0V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

#### AC Electrical Characteristics: See Section 2 for waveforms

|  | 100 V 10  | 8.0               |     | 74ACT                  | 54ACT |                         | 74ACT |                        | V Jugni |                      |
|--|---|-------------------|-----|------------------------|-------|-------------------------|-------|------------------------|---------|----------------------|
| Symbol Parameter  Propagation Delay In to Zn |   | V <sub>CC</sub> * |     | A = +25°C<br>L = 50 pF | to +  | -55°C<br>125°C<br>50 pF | to +  | -40°C<br>85°C<br>50 pF | Units   | Fig.<br>No.<br>2-3,4 |
|  |   | 5.0               | 1.5 | 5.0 7.0                | 1.0   | 8.0                     | 31.0  | 7.5                    |         |                      |
| t <sub>PHL</sub>                             | Propagation Delay<br>I <sub>n</sub> to Z <sub>n</sub> | 5.0               | 2.0 | 6.0 7.5                | 1.0   | 9.5                     | 1.5   | 8.5                    | ns      | 2-3,4                |
| tpLH   | Propagation Delay<br>S to Z <sub>n</sub>              | 5.0               | 2.0 | 7.0 9.5                | 1.0   | 11.0                    | 1.5   | 10.5                   | ns      | 2-3,4                |
| t <sub>PHL</sub>                             | Propagation Delay<br>S to Z <sub>n</sub>              | 0.15.0            | 2.5 | 7.0 1 10.5             | 1.0 ± | 11.5                    | 2.0   | 11.5                   | ns      | 2-3,4                |
| t <sub>PZH</sub> V                           | Output Enable Time                                    | 5.0               | 2.0 | 6.0 8.0                | 1.0   | 9.5                     | 1.5   | AT29.0                 | ns      | 2-5                  |
| t <sub>PZL</sub>                             | Output Enable Time                                    | 5.0               | 2.0 | 6.0 8.0                | 1.0   | 9.5                     | 1.5   | 9.0                    | ns      | 2-6                  |
| t <sub>PHZ</sub>                             | Output Disable Time                                   | 5.0               | 2.5 | 6.5 9.0                | 1.0   | 10.5                    | 3.5   | 10.0                   | ns      | 2-5                  |
| tPLZ   | Output Disable Time                                   | 5.0               | 2.0 | 6.0 7.5                | 1.0   | 9.0                     | 1.5   | 8.5                    | ns      | 2-6                  |

1.5

\*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions      |
|-----------------|----------------------------------|------|-------|-----------------|
| CIN             | Input Capacitance                | 4.5  | pF s  | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 50.0 | pF    | $V_{CC} = 5.0V$ |



# 54AC/74AC258 • 54ACT/74ACT258 Quad 2-Input Multiplexer with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable (OE) input, allowing the outputs to interface directly with bus-oriented systems.

#### **Features**

- Multiplexer expansion by tying outputs together
- Inverting TRI-STATE outputs → 2 0 000 =
- Outputs source/sink 24 mA
- 'ACT258 has TTL-compatible inputs
- Standard Military Drawing (SMD)
- 'ACT258: 5962-88704

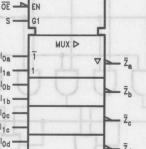
#### Ordering Code: See Section 8

#### **Logic Symbols**

# 1a 0b 1b 0c 1c 0d 1d TL/F/9950-1



loc



IEEE/IEC

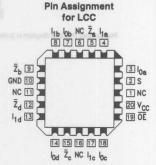


**Connection Diagrams** 

**Pin Assignment** for DIP, Flatpak and SOIC

TL/F/9950-2

| Pin Names                         | Description                      |
|-----------------------------------|----------------------------------|
| S                                 | Common Data Select Input         |
| ŌĒ                                | TRI-STATE Output Enable Input    |
| loa-lod                           | Data Inputs from Source 0        |
| l <sub>1a</sub> -l <sub>1d</sub>  | Data Inputs from Source 1        |
| $\overline{Z}_a - \overline{Z}_d$ | TRI-STATE Inverting Data Outputs |



TL/F/9950-4

#### **Functional Description**

The 'AC/'ACT258 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the  $l_{0x}$  inputs are selected and when Select is HIGH, the  $l_{1x}$  inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/'ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$

$$\overline{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$

$$\overline{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$

$$\overline{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

When the Output Enable input (OE) is HIGH, the outputs are forced to a high impedance state. If the outputs of the TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should

K 01 040

ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

#### Truth Table

| Output<br>Enable | Select<br>Input | 1000 000 32.6  | ata<br>outs | Outputs<br>Z |  |
|------------------|-----------------|----------------|-------------|--------------|--|
| ŌĒ               | S               | I <sub>0</sub> | e Original  |              |  |
| lw 11Helgitiu    | n hig X-S be    | X              | X           | OA Z         |  |
| вооцюв ож        |                 |                | прија, Р    |              |  |
| _                | data Helact     |                |             | betseles     |  |
| _                | oo entini sint  | perDele        | X           | Н            |  |
| agmi dgiri a     | s switched to   | Н              | X           | in inter     |  |

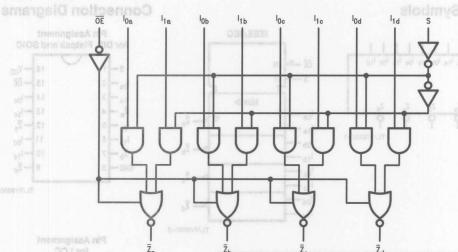
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

#### **Logic Diagram**



TL/F/9950-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for availa     |                              |
|------------------------------------|------------------------------|
| Supply Voltage (V <sub>CC</sub> )  | -0.5V to +7.0V               |
| DC Input Diode Current (IIK)       |                              |
| $V_{I} = -0.5V$                    | -20 mA                       |
| $V_I = V_{CC} + 0.5V$              | + 20 mA                      |
| DC Input Voltage (V <sub>I</sub> ) | $-0.5$ V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK)      |                              |
| $V_0 = -0.5V$                      | -20 mA                       |
| $V_O = V_{CC} + 0.5V$              | + 20 mA                      |
| DC 0. da. d Vallage (V )           | 0 EV/+0+0 V + 0 EV/          |

DC Output Voltage (V<sub>O</sub>) -0.5V to to V<sub>CC</sub> + 0.5V DC Output Source

or Sink Current (I<sub>O</sub>) ±50 mA
DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±50 mA
Storage Temperature (T<sub>STG</sub>) -65°C to +150°C
Junction Temperature (T<sub>,j</sub>)

CDIP 175°C PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT | 2.0V to 6.0V<br>4.5V to 5.5V |
|--|------------------------------|
| Input Voltage (V <sub>I</sub> )            | 0V to V <sub>CC</sub>        |
| Output Voltage (V <sub>O</sub> )           | ATB-IFIT mumbel OV to VCC    |
| Operating Temperature (T <sub>A</sub> )    |                              |
| 74AC/ACT                                   | -40°C to +85°C               |
| 54AC/ACT                                   | -55°C to +125°C              |
| Minimum Input Edge Rate (ΔV                | /Δt)                         |

'AC Devices
V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>

 $V_{CC}$  @ 3.3V 4.5V, 5.5V 125 mV/ns Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

'ACT Devices
V<sub>IN</sub> from 0.8V to 2.0V
V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

#### **DC Characteristics for 'AC Family Devices**

|                           | - ggV 10  | 2.0                    | 74                      | AC 05                | 54AC                                   | 1.5        | 8.6                             | 74AC                 | agi        | Input Voits  |  |
|---------------------------|---|------------------------|-------------------------|----------------------|--|------------|---------------------------------|----------------------|------------|--|--|
| Symbol                    | Parameter   | V <sub>CC</sub><br>(V) |                         |                      | 25°C T <sub>A</sub> = -55°C to + 125°C |            | T <sub>A</sub> = -40°C to +85°C |                      | Units      | Conditions   |  |
|                           | = ruol- v   | 4,4                    | Тур                     | 4.4                  | Guaran                                 | teed L     | imits                           |                      | ligh Leve  | VoH Minimum  |  |
| VIH<br>HIV 10 JI<br>Am AS | Minimum High Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85                    | 98.8       | 6.5                             | 2.1<br>3.15<br>3.85  | V          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$               |  |
| V <sub>IL</sub>           | Maximum Low Level Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65                    | 100.0      | 4,5                             | 0.9<br>1.35<br>1.65  | epsi       | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V |  |
| Voh<br>Am AS<br>Am AS     | Minimum High Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                      |            | 4.5                             | 2.9<br>4.4<br>5.4    | ٧          | $I_{OUT} = -50 \mu\text{A}$                          |  |
|                           | poV = IV Au   | 0.1±                   |                         | 0.13                 | 1,0±                                   |            | 8.5                             | kage Current         | sell Jugri | *VIN = VIL or VIH                                    |  |
|                           | $D_{\Lambda} = D_{\Lambda}$ $D_{\Lambda} = D_{\Lambda}$ $D_{\Lambda} = D_{\Lambda}$ | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                      |            | 3.6                             | 2.46<br>3.76<br>4.76 | V V        | -12 mA<br>I <sub>OH</sub> -24 mA<br>-24 mA           |  |
| JOV Nax                   | Maximum Low Level<br>Output Voltage   | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                      | 8.0        | 8.8                             | 0.1<br>0.1<br>0.1    | Dynamic    | ΙΟυΤ = 50 μΑ   |  |
|                           | = g <sub>H</sub> gV Am  | 97-                    |                         | 08-                  |  |            | 5.6                             |                      | Hasa       | *VIN = VIL or VIH                                    |  |
| 0                         | PA VIN = Vo   | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50                   | mehric tur | 5.5 sith out                    | 0.44<br>0.44<br>0.44 | Viet       | 12 mA<br>I <sub>OL</sub> 24 mA<br>24 mA              |  |
| I <sub>IN</sub>           | Maximum Input<br>Leakage Current  | 5.5                    |                         | ±0.1                 | ±1.0                                   |            | 30 è time<br>1 28°C.            | ±1.0                 | μА         | $V_I = V_{CC}$ , GND                                 |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'AC Family Devices (Continued) THIS THE MEMORIAL AND ADDITIONAL AND THE PROPERTY OF THE

| Symbol     | Parameter                        |                        | 74AC                   |             | 54AC                              | 54AC 74AC                       |                       | H Military/Aerosp  |
|------------|----------------------------------|------------------------|------------------------|-------------|-----------------------------------|---------------------------------|-----------------------|--|
|            |                                  | V <sub>CC</sub><br>(V) |                        | A =<br>25°C | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                 | Conditions   |
|            |                                  |                        | Тур                    | tetloV tu   | Guaranteed L                      | imits                           | rent (i <sub>jK</sub> | DC Input Diode Cu  |
| loz / oi / | Maximum TRI-STATE® Current       | 5.5                    | (V) sgs<br>regme<br>Ti | ±0.5        | ± 10.0                            | ±5.0                            | μА                    | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND |
| IOLD       | †Minimum Dynamic                 | 5.5                    | - 1                    | MACHAE      | 50                                | 75                              | mA                    | V <sub>OLD</sub> = 1.65V Max   |
| IOHD       | Output Current                   | 5.5                    | sec                    | wed OA      | -50                               | -75                             | mA V                  | V <sub>OHD</sub> = 3.85V Min   |
| Icc        | Maximum Quiescent Supply Current | 5.5                    | 30% ti<br>3V 4.5V      | 8.0         | 160.0                             | 80.0                            | μА                    | $V_{IN} = V_{CC}$ or GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## **DC Characteristics for 'ACT Family Devices**

|                  |                                      |              |                        |                         |              | O West                            |                               |                | 1174   |  |
|------------------|--------------------------------------|--------------|------------------------|-------------------------|--------------|-----------------------------------|-------------------------------|----------------|--|--|
|                  | Parameter                            |              |                        | 74                      | ACT          | 54ACT                             | 74ACT                         | e eghillen Mur | Property of Application of the Control of the Contr |  |
| Symbol           |                                      |              | V <sub>CC</sub><br>(V) | T <sub>A</sub> = + 25°C |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85 |                | Conditions   |  |
|                  |                                      |              | Тур                    |                         | Guaranteed   | Limits                            |                               | 10.00          |  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage  | TWAC         | 4.5<br>5.5             | 1.5                     | 2.0          | 2.0<br>2.0                        | 2.0                           | V              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VIL              | Maximum Low Level Input Voltage      | # AT         | 4.5<br>5.5             | 1.5<br>1.5              | 0.8          | 0.8                               | 0.8                           | V              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 1.5          | 4.5<br>5.5             | 4.49<br>5.49            | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                    | V              | $I_{OUT} = -50 \mu\text{A}$  |  |
| VEO              | - 20V 10 V                           |              | 4.5<br>5.5             |                         | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                  | egai<br>V      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 1,36         | 4.5<br>5.5             | 0.001<br>0.001          | 0.1          | 0.1                               | 0.1<br>0.1                    | ٧              | I <sub>OUT</sub> = 50 μA   |  |
| 50 µA            | Tuo <sup>I</sup> V                   |              | 4.5<br>5.5             |                         | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                  | High Leve      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$   |  |
| In               | Maximum Input Leakage                | Current      | 5.5                    |                         | ±0.1         | ±1.0                              | ±1.0                          | μΑ             | $V_I = V_{CC}$ , GND   |  |
| loz              | Maximum TRI-STATE® Current           | 2.48<br>3.76 | 5.5                    |                         | ±0.5         | ± 10.0                            | ±5.0                          | μА             | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |
| Гсст             | Maximum I <sub>CC</sub> /Input       | 0.1          | 5.5                    | 0.6                     | 1.0          | 1.6 0                             | 00.0 1.5                      | mA             | $V_{I} = V_{CC} - 2.1V$  |  |
| lold             | †Minimum Dynamic                     | 0.1          | 5.5                    |                         | 1.0          | 50                                | 75                            | mA             | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub> | Output Current                       |              | 5.5                    |                         |              | -50                               | -75                           | mA             | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc St<br>Am AS  | Maximum Quiescent<br>Supply Current  | 0.44         | 5.5                    |                         | 8.0          | 160.0                             | 80.0                          | μА             | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  |   |                          |            | 74AC                  |             | 54  | 54AC         |  | 74AC         |       |             |
|------------------|---|--------------------------|------------|-----------------------|-------------|---|--------------|--|--------------|-------|-------------|
| Symbol           | Parameter                                   | V <sub>CC</sub> *<br>(V) |            | A = +25°<br>CL = 50 p |             | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |              | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |              | Units | Fig.<br>No. |
|                  |   |                          | Min        | Тур                   | Max         | Min   | Max          | Min  | Max          | Ole   | toO         |
| t <sub>PLH</sub> | Propagation Delay $I_n$ to $\overline{Z}_n$ | 3.3<br>5.0               | 2.0<br>1.5 | 6.0<br>4.5            | 9.5<br>7.5  | 1.0<br>1.0  | 12.0<br>9.5  | 1.5<br>1.0   | 11.0<br>8.5  | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $I_n$ to $\overline{Z}_n$ | 3.3<br>5.0               | 2.0        | 5.0<br>4.0            | 8.5<br>6.5  | 1.0   | 10.5<br>7.5  | 1.5<br>1.0   | 9.5<br>7.0   | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay S to $\overline{Z}_n$     | 3.3                      | 3.0        | 7.5<br>6.0            | 12.0        | 1.0   | 15.0<br>11.5 | 2.5<br>1.5   | 14.0<br>10.5 | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay S to $\overline{Z}_n$     | 3.3<br>5.0               | 2.5<br>1.5 | 7.5<br>5.5            | 11.5<br>9.0 | 1.0   | 14.0<br>10.5 | 2.0<br>1.5   | 13.0<br>10.0 | ns    | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time                          | 3.3<br>5.0               | 2.5<br>1.5 | 6.0<br>4.5            | 9.5<br>7.5  | 1.0   | 11.5<br>9.0  | 2.0  | 10.5         | ns    | 2-5         |
| t <sub>PZL</sub> | Output Enable Time                          | 3.3<br>5.0               | 2.0        | 5.5<br>5.5            | 9.0         | 1.0   | 10.5<br>8.5  | 1.5<br>1.0   | 10.0         | ns    | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                         | 3.3<br>5.0               | 2.5        | 5.5<br>5.5            | 10.0<br>8.5 | 1.0<br>1.0  | 11.5<br>9.5  | 2.0<br>1.5   | 11.0<br>9.0  | ns    | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time                         | 3.3<br>5.0               | 2.0        | 5.5<br>5.0            | 9.0<br>7.0  | 1.0   | 10.5<br>8.5  | 2.0  | 10.0         | ns    | 2-6         |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  | , Flatpak and SOIC                          | for Dil           |     | 74ACT   |      | 54A  | СТ   | 74/  | ACT                    |       |             |
|------------------|---|-------------------|-----|---|------|--|------|------|------------------------|-------|-------------|
| Symbol           | Parameter                                   | V <sub>CC</sub> * |     | T <sub>A</sub> = +25<br>C <sub>L</sub> = 50 p |      | T <sub>A</sub> = -<br>to + 1<br>C <sub>L</sub> = 8 | 25°C | to + | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                  | t0 81                                       | Dg-13             | Min | Тур   | Max  | Min  | Max  | Min  | Max                    |       | 3× 0-       |
| t <sub>PLH</sub> | Propagation Delay $I_n$ to $\overline{Z}_n$ | 5.0               | 2.0 | 6.5   | 8.5  | 1.0  | 10.5 | 1.5  | 9.5                    | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $I_n$ to $\overline{Z}_n$ | 5.0               | 2.0 | 5.5   | 7.5  | 1.0  | 9.0  | 1.5  | 8.0                    | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay S to $\overline{Z}_n$     | 5.0               | 3.0 | 7.5   | 10.5 | 1.0  | 13.0 | 2.0  | 11.5                   | ns    | 2-3, 4      |
| tpHL             | Propagation Delay S to $\overline{Z}_n$     | 5.0               | 1.5 | 7.0   | 9.5  | 1.0  | 12.0 | 1.5  | 11.0                   | ns    | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time                          | 5.0               | 2.0 | 6.5   | 8.5  | 1.0  | 10.5 | 1.5  | 9.5                    | ns    | 2-5         |
| t <sub>PZL</sub> | Output Enable Time                          | 5.0               | 2.0 | 6.5   | 8.5  | 1.0  | 10.0 | 1.5  | 9.5                    | ns    | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                         | 5.0               | 1.5 | 7.0   | 9.0  | 1.0  | 10.5 | 1.0  | 10.0                   | ns    | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time                         | 5.0               | 2.0 | 6.0   | 8.0  | 1.0  | 10.0 | 1.5  | 9.0                    | ns    | 2-6         |

\*Voltage Range 5.0 is 5.0V ±0.5V

#### Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions             |
|-----------------|-------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation Capacitance | 55.0 | pF    | V <sub>CC</sub> = 5.0V |



## 54AC/74AC273 Octal D Flip-Flop

#### **General Description**

The 'AC273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{\text{MR}}$ ) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{MR}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

#### **Features**

■ Ideal buffer for MOS microprocessor or memory

Electrical Characteristics: See Section 2 for waveforms

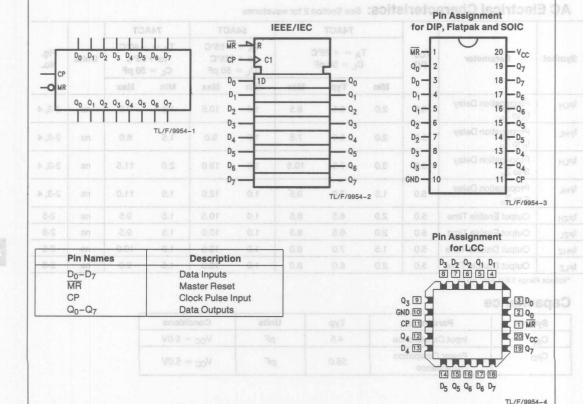
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- See '377 for clock enable version
- See '373 for transparent latch version
- See '374 for TRI-STATE version
- Outputs source/sink 24 mA
- Standard Military Drawing (SMD)
  - 'AC273: 5962-87756

Ordering Code: See Section 8

**Logic Symbols** 

**Connection Diagrams** 

Symbol



| 2.0V to 6.0V  | MR | CP | Dn     | anQ <sub>n</sub> soll be |
|---------------|----|----|--------|--------------------------|
| Reset (Clear) | L  | X  | TOA' X | 0.5 Ye of Va.0           |
| Load '1'      | Н  | 5  | Н      | Am OsH.                  |
| Load '0'      | н  |    | L      | Airc 0S_+                |

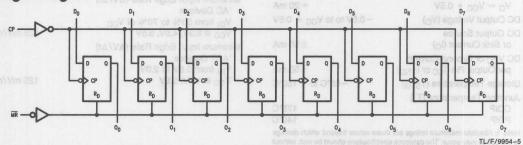
H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

X = Immaterial

✓ = LOW-to-HIGH Transition

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

|  | TA = |  |                   |                         |                                      |     |
|--|---|--|-------------------|-------------------------|--------------------------------------|-----|
|  |   |  |                   |                         |                                      |     |
|  |   |  |                   |                         |                                      |     |
|  |   |  |                   |                         | Maximum Low Level<br>Input Voltage   | JIV |
|  |   |  | 2.9<br>4.4<br>5.4 |                         | Minimum High Lavel<br>Output Voltage |     |
|  |   |  |                   |                         |                                      |     |
|  |   |  |                   | 0.002<br>0.001<br>0.001 |                                      |     |
|  |   |  |                   |                         |                                      |     |
|  |   |  |                   |                         |                                      |     |

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. Supply Voltage ( $V_{\rm CC}$ ) -0.5V to +7.0V

Supply Voltage ( $V_{CC}$ ) = -0.5V to +7.0V DC Input Diode Current ( $I_{IK}$ ) = -0.5V  $V_{I} = V_{CC} + 0.5V$  = 20 mA + 20 mA DC Input Voltage ( $V_{I}$ ) = -0.5V to  $V_{CC} + 0.5V$ 

DC Output Diode Current ( $I_{OK}$ )  $V_O = -0.5V$  $V_O = V_{CC} + 0.5V$ 

DC Output Voltage (V<sub>O</sub>)
DC Output Source

or Sink Current (I<sub>O</sub>)
DC V<sub>CC</sub> or Ground Current
per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>)
Storage Temperature (T<sub>STG</sub>)

Junction Temperature (TJ)
CDIP
PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTT\* circuits outside databook specifications.

#### Recommended Operating

Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 'AC
 2.0V to 6.0V

 'ACT
 4.5 to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

 Output Voltage (V<sub>O</sub>)
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 4.00 to 1.05 °C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

125 mV/ns

#### DC Characteristics for 'AC Family Devices

|                 |                                      |                        | 74                      | AC                   | 54AC                             | 74AC                            |       |  |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |  |
|                 |                                      |                        | Тур                     | yp Guaranteed Limits |                                  |                                 |       |  |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu\text{A}$  |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | ٧     | $\label{eq:VIN} \begin{split} *V_{\text{IN}} &= V_{\text{IL}}  \text{or}  V_{\text{IH}} \\ &- 12  \text{mA} \\ I_{\text{OH}} &- 24  \text{mA} \\ &- 24  \text{mA} \end{split}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | ٧     | I <sub>OUT</sub> = 50 μA   |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $12 \text{ mA}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$  |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μΑ    | $V_{I} = V_{CC}$ , GND   |  |

-20 mA

+20 mA

±50 mA

±50 mA

175°C

140°C

65°C to + 150°C

-0.5V to to VCC + 0.5V

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'AC Family Devices (Continued)

|                  | 97                                  | skillena                             | 74  | AC     | 54AC                              | 74AC                            |       | Symbol                       |
|------------------|-------------------------------------|--------------------------------------|-----|--------|-----------------------------------|---------------------------------|-------|------------------------------|
| Symbol Parameter |                                     | V <sub>CC</sub> (V) T <sub>A</sub> = |     | + 25°C | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions                   |
|                  | 1                                   |                                      | Тур |        | Guaranteed L                      | imits                           | Cap   |                              |
| lold             | †Minimum Dynamic                    | 5.5                                  |     |        | 50                                | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max |
| lohd             | Output Current                      | 5.5                                  |     |        | -50                               | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min |
| lcc              | Maximum Quiescent<br>Supply Current | 5.5                                  |     | 8.0    | 160.0                             | 80.0                            | μА    | $V_{IN} = V_{CC}$ or GND     |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  |                                      |             |  | 74AC       |              | 54  | AC           | 74   | AC           |       |             |
|------------------|--------------------------------------|-------------|--|------------|--------------|---|--------------|--|--------------|-------|-------------|
| Symbol Parameter |                                      | Vcc*<br>(V) | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |            |              | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 pF$ |              | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |              | Units | Fig.<br>No. |
|                  |                                      |             | Min  | Тур        | Max          | Min   | Max          | Min  | Max          |       |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency           | 3.3<br>5.0  | 90<br>140                                  | 125<br>175 |              | 75<br>90  |              | 75<br>125  |              | MHz   |             |
| t <sub>PLH</sub> | Propagation Delay<br>Clock to Output | 3.3<br>5.0  | 4.0<br>3.0                                 | 7.0<br>5.5 | 12.5<br>9.0  | 1.0<br>1.0  | 15.0<br>11.0 | 3.0<br>2.5   | 14.0<br>10.0 | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>Clock to Output | 3.3<br>5.0  | 4.0<br>3.0                                 | 7.0<br>5.0 | 13.0<br>10.0 | 1.0<br>1.0  | 16.0<br>11.5 | 3.5<br>2.5   | 14.5<br>11.0 | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay MR to Output       | 3.3<br>5.0  | 4.0<br>3.0                                 | 7.0<br>5.0 | 13.0<br>10.0 | 1.0<br>1.0  | 16.0<br>11.5 | 3.5<br>2.5   | 14.0<br>10.5 | ns    | 2-3, 4      |

<sup>\*</sup>Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

#### AC Operating Requirements: See Section 2 for waveforms

|                  |                                       |            | 74  | AC         | 54AC   | 74AC   |       |             |
|------------------|---------------------------------------|------------|---|------------|--|--|-------|-------------|
| Symbol           | /mbol Parameter                       |            | $T_A = +25^{\circ}C$<br>$C_L = 50 \text{ pF}$ |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig.<br>No. |
|                  |                                       |            | Тур   |            | Guaranteed Min   | imum   |       |             |
| ts               | Setup Time, HIGH or LOW<br>Data to CP | 3.3<br>5.0 | 3.5<br>2.5                                    | 5.5<br>4.0 | 8.0<br>5.0   | 6.0<br>4.5   | ns    | 2-7         |
| th               | Hold Time, HIGH or LOW<br>Data to CP  | 3.3<br>5.0 | -2.0<br>-1.0                                  | 0          | 0 1.0  | 0<br>1.0   | ns    | 2-7         |
| t <sub>w</sub>   | Clock Pulse Width<br>HIGH or LOW      | 3.3<br>5.0 | 3.5<br>2.5                                    | 5.5<br>4.0 | 6.5<br>5.0   | 6.0<br>4.5   | ns    | 2-3         |
| t <sub>w</sub>   | MR Pulse Width<br>HIGH or LOW         | 3.3<br>5.0 | 2.0<br>1.5                                    | 5.5<br>4.0 | 10.0<br>6.5  | 6.0<br>4.5   | ns    | 2-3         |
| t <sub>rec</sub> | Recovery Time<br>MR to CP             | 3.3<br>5.0 | 1.5<br>1.0                                    | 3.5<br>2.0 | 6.0<br>4.0   | 4.5<br>3.0   | ns    | 2-3, 7      |

<sup>\*</sup>Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

## Capacitance

| Symbol C <sub>IN</sub> | Parameter Input Capacitance |                     | <b>Typ</b> 4.5 | Units | Condition V <sub>CC</sub> = 5 | - |           |  |
|------------------------|-----------------------------|---------------------|----------------|-------|-------------------------------|---|-----------|--|
| C <sub>PD</sub>        | Power                       | Dissipation citance | 50.0           | pF    | V <sub>CC</sub> = 5           |   | Parameter |  |
|                        |                             |                     |                |       |                               |   |           |  |
|                        |                             |                     |                |       |                               |   |           |  |
|                        |                             |                     |                |       |                               |   |           |  |

"All outputs leaded; Unesholds on Ingul associated with output under to

emit a sa bulanol tucturo eno Jam 0.0 material test murrillo

Note: In and Ico @ 3.0V are guaranteed to be less than or equal to the respective limit 6-5.5V Vgg.

#### AC Electrical Characteristics: See Section 2 for wevelonns

|        |  |  | TA =<br>10 + 1<br>C <sub>k</sub> = |            |  |  |
|--------|--|--|------------------------------------|------------|--|--|
|        |  |  |                                    |            |  |  |
|        |  |  |                                    |            |  |  |
|        |  |  |                                    | 7.0<br>5.5 |  |  |
| 2-8, 4 |  |  |                                    |            |  |  |
|        |  |  |                                    |            |  |  |

\*Voltage Flarge 3.3 is 8,3V ± 0.3V Voltage Flarge 5.0 is 5.0V ± 0.5V

#### AC Operating Requirements: See Section 2 for waveforms

|  | $T_A = -40^{\circ}C$ to +85°C $C_L = 50 \text{ pF}$ |  |  |  |
|--|---|--|--|--|
|  |   |  |  |  |
|  |   |  |  |  |
|  |   |  |  |  |
|  |   |  |  |  |
|  | 6.0<br>4.5  |  |  |  |
|  |   |  |  |  |

Voltage Franço 3.3 is 3.3V ±0.3V Voltage Rungo 5.0 is 5.0V ± 0.5V

# 54AC/74AC280 9-Bit Parity Generator/Checker

#### **General Description**

The 'AC280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

#### **Features**

■ 9-bit width for memory applications

#### Ordering Code: See Section 8 **Connection Diagrams Logic Symbols** Pin Assignment Pin Assignment for DIP, SOIC and Flatpak for LCC 12 15 13 Σ<sub>E</sub> NC I<sub>8</sub> NC NC 8 7 6 5 4 13 Σ<sub>0</sub> 9 GND 10 NC 11 I<sub>0</sub> 12 I<sub>1</sub> 13 NC-2 I<sub>6</sub> 1 NC 20 V<sub>CC</sub> E-TL/F/9955-1 $\Sigma_0$ GND -IEEE/IEC 14 15 16 17 18 2k TL/F/9955-2 12 NC 13 NC 14 TL/F/9955-3

| Pin Names | Description        |
|-----------|--------------------|
| 10-18     | Data Inputs        |
| Σο        | Odd Parity Output  |
| ΣΕ        | Even Parity Output |

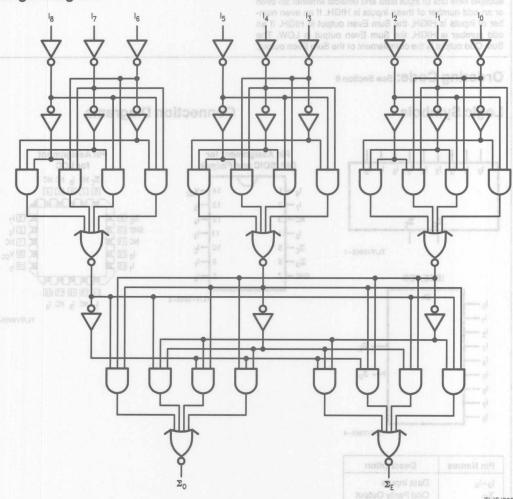
TL/F/9955-4

| I <sub>0</sub> -I <sub>8</sub> | Σ Even | ≥ Uaa |                              |
|--------------------------------|--------|-------|------------------------------|
|                                |        |       | CARRIAGOOG                   |
| 0, 2, 4, 6, 8                  | Н      | L     | ODPOWER POST                 |
| 1, 3, 5, 7, 9                  | L      | H NO  | 9-Bit Parity Generator/Check |

H = HIGH Voltage Level

L = LOW Voltage Level

#### **Logic Diagram**



TL/F/9955-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for a   | availability and specifications. |         |
|---|----------------------------------|---------|
| Supply Voltage (V <sub>CC</sub> )   | -0.5V to +7.0\                   | 1 3     |
| DC Input Diode Current (  | ik) efimili bosins               |         |
| $V_{l} = -0.5V$   | -20 m/                           |         |
| $V_I = V_{CC} + 0.5V$   | + 20 m/                          | 1       |
| DC Input Voltage (V <sub>I</sub> )  | -0.5V to V <sub>CC</sub> + 0.5V  | 1       |
| DC Output Diode Current<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$                       | (lok) -20 m/<br>+20 m/           |         |
| DC Output Voltage (V <sub>O</sub> )   | -0.5V to V <sub>CC</sub> + 0.5   | /       |
| DC Output Source<br>or Sink Current (I <sub>O</sub> )                                   | ±50 m/                           | nii avi |
| DC V <sub>CC</sub> or Ground Curre<br>per Output Pin (I <sub>CC</sub> or I <sub>C</sub> |                                  | Andri   |

PDIP

140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Storage Temperature (T<sub>STG</sub>)
Junction Temperature (T<sub>J</sub>)

CDIP

# Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT |                     | 2.0V to 6.0V<br>4.5V to 5.5V        |
|--|---------------------|-------------------------------------|
| Input Voltage (V <sub>I</sub> )            |                     | 0V to V <sub>CC</sub>               |
| Output Voltage (V <sub>O</sub> )           |                     | olmsmyO mumin 0V to V <sub>CC</sub> |
| Operating Temperatur                       | e (T <sub>A</sub> ) | -40°C to +85°C                      |

74AC/ACT  $-40^{\circ}\text{C to} + 85^{\circ}\text{C}$ 54AC/ACT  $-55^{\circ}\text{C to} + 125^{\circ}\text{C}$ Minimum Input Edge Rate ( $\Delta V/\Delta t$ )

'AC Devices
V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>
V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV

Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) ACT Devices  $V_{IN}$  from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

#### DC Characteristics for 'AC Family Devices

-65°C to +150°C

175°C

| Symbol          |                                      | and a               | 74AC<br>T <sub>A</sub> = +25°C |                      | 54AC                             | 74AC                            |       | 7 200   |
|-----------------|--------------------------------------|---------------------|--------------------------------|----------------------|----------------------------------|---------------------------------|-------|---|
|                 | Parameter                            | V <sub>CC</sub> (V) |                                |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |
|                 | 8                                    | tollibe             | Тур                            | astrus               | Guaranteed Lin                   |                                 |       |   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75            | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage      |                     | 1.5<br>2.25<br>2.75            | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49           | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu A$   |
|                 |                                      | 3.0<br>4.5<br>5.5   |                                | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | V     | $V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ m/s}$ $I_{OH} - 24 \text{ m/s}$ $-24 \text{ m/s}$ |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001        | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V     | I <sub>OUT</sub> = 50 μA  |
|                 |                                      | 3.0<br>4.5<br>5.5   |                                | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | V     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $12 \text{ mA}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$    |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                 |                                | ±0.1                 | ±1.0                             | ±1.0                            | μΑ    | $V_{I} = V_{CC}$ , GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'AC Family Devices (Continued) and a mumb of the local A

| Symbol Vo.s      |                                     | V <sub>CC</sub> (V) | 74AC<br>T <sub>A</sub> = +25°C |            | 54AC                             | 74AC                            | Units      | Conditions                               |  |
|------------------|-------------------------------------|---------------------|--------------------------------|------------|----------------------------------|---------------------------------|------------|--|--|
|                  | Vos Parameter                       |                     |                                |            | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C |            |  |  |
|                  | 70                                  |                     | Тур                            | ensiloV iu | Guaranteed Li                    | mits                            | (hid) iner | DC Input Diode Cur                       |  |
| I <sub>OLD</sub> | †Minimum Dynamic                    | 5.5                 | (oV) e                         | atteV tuqt | 50                               | 75                              | mA         | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD             | Output Current                      | 5.5                 | mperatu                        | erating Te | -50.0 + oo                       | / of va.0-75                    | mA         | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5                 |                                | 8.0        | 160.0                            | 80.0                            | μА         | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note:  $I_{\text{IN}}$  and  $I_{\text{CC}} @ 3.0 \text{V}$  are guaranteed to be less than or equal to the respective limit @ 5.5 V V<sub>CC</sub>.  $I_{\text{CC}}$  for 54AC @ 25°C is identical to 74 AC @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms

| Symbol           | Parameter                             | V <sub>CC</sub> *<br>(V) |  | 74AC        |              | 54  | AC           | 74   | AC           | pulnar o    | de sont             |
|------------------|---------------------------------------|--------------------------|--|-------------|--------------|---|--------------|--|--------------|-------------|---------------------|
|                  |                                       |                          | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             |              | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |              | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |              | Units       | Fig.<br>No.         |
|                  |                                       |                          | Min  | Тур         | Max          | Min   | Max          | Min  | Max          | vice may of | phososs<br>of other |
| t <sub>PLH</sub> | Propagation Delay $I_n$ to $\Sigma_E$ | 3.3<br>5.0               | 5.0<br>3.0                                       | 10.5<br>7.5 | 17.0<br>13.0 | 1.0<br>1.5  | 20.0<br>14.5 | 4.0<br>2.0   | 18.5<br>14.5 | ns          | 2-3, 4              |
| t <sub>PLH</sub> | Propagation Delay $I_n$ to $\Sigma_O$ | 3.3<br>5.0               | 5.0<br>3.0                                       | 12.0<br>8.5 | 17.0<br>13.0 | 1.0<br>1.5  | 20.0<br>14.5 | 4.0<br>2.0   | 18.5<br>14.5 | ns          | 2-3, 4              |

#### Capacitance

| Symbol          |   | Parameter Typ Units |      |    |                        | nditio            | ns                       |  |
|-----------------|---|---------------------|------|----|------------------------|-------------------|--------------------------|--|
| CIN             | Input Capacitance Power Dissipation Capacitance |                     | 4.5  | pF | Vo                     | C = 5.0           | OV                       |  |
| C <sub>PD</sub> |   |                     | 75.0 | pF | V <sub>CC</sub> = 5.0V |                   | Minimum High<br>OV Stage |  |
|                 |   |                     |      |    |                        |                   |                          |  |
|                 |   |                     |      |    |                        |                   |                          |  |
|                 |   |                     |      |    |                        |                   |                          |  |
|                 |   |                     |      |    |                        |                   |                          |  |
|                 |   |                     |      |    |                        | 3,0<br>4,5<br>6,5 |                          |  |
|                 |   |                     |      |    |                        |                   |                          |  |

## 54AC/74AC299 • 54ACT/74ACT299 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

#### **General Description**

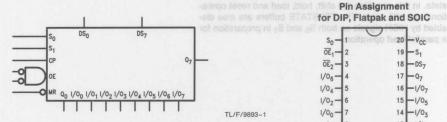
The 'AC/'ACT299 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q0, Q7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

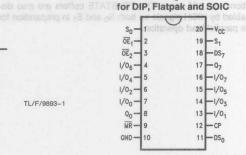
#### **Features**

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT299 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC299: 5962-88754 Sample WOJ A
  - 'ACT299: 5962-88771

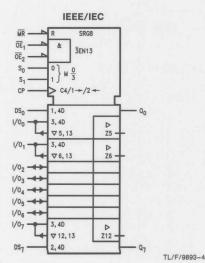
Ordering Code: See Section 8 **Logic Symbols** 

#### **Connection Diagrams**





TL/F/9893-2



for LCC 001/001/021/041/06 87654 MR 9 GND TO 1 S<sub>0</sub>
20 V<sub>CC</sub>
19 S<sub>1</sub> DS<sub>0</sub> 11 CP 12 1/0, 13 14 15 16 17 18 1/031/051/07 Q7 DS7

**Pin Assignment** 

TL/F/9893-3

| Pin Names                             | Description                       |
|---------------------------------------|-----------------------------------|
| CP                                    | Clock Pulse Input                 |
| DS <sub>0</sub>                       | Serial Data Input for Right Shift |
| DS <sub>7</sub>                       | Serial Data Input for Left Shift  |
|                                       | Mode Select Inputs                |
| S <sub>0</sub> , S <sub>1</sub>       | Asynchronous Master Reset         |
| $\overline{OE}_1$ , $\overline{OE}_2$ | TRI-STATE Output Enable Inputs    |
| 1/00-1/07                             | Parallel Data Inputs or           |
|                                       | TRI-STATE Parallel Outputs        |
| Q <sub>0</sub> , Q <sub>7</sub>       | Serial Outputs                    |

#### **Functional Description**

The 'AC/'ACT299 contains eight edge-triggered D-type flipflops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by  $S_0$  and  $S_1$ , as shown in the Truth Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode.  $Q_0$  and  $Q_7$  are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on  $\overline{\text{MR}}$  overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either  $\overline{OE}_1$  or  $\overline{OE}_2$  disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S $_0$  and S $_1$  in preparation for a parallel load operation.

#### **Truth Table**

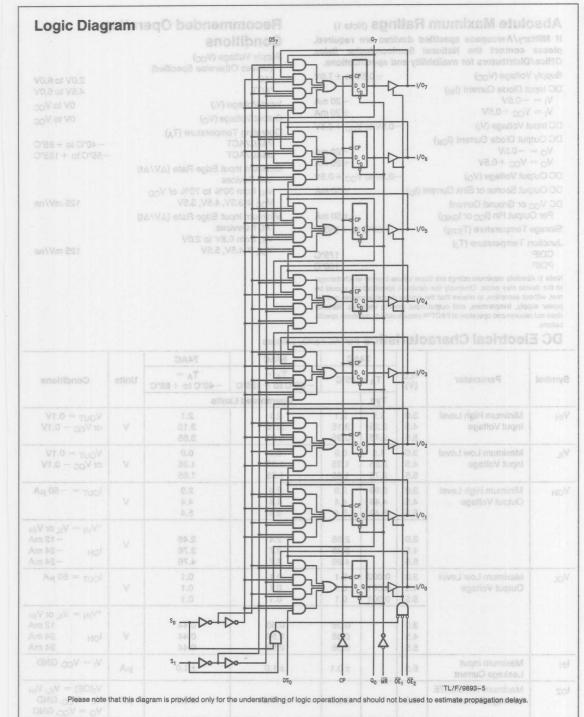
| gen apas                         | Inp            | outs           | winu tid | Response   |
|----------------------------------|----------------|----------------|----------|--|
| MR                               | S <sub>1</sub> | S <sub>0</sub> | CP       | with TRI-STATE® output   |
| ustibles<br>ustibles<br>onal out | X              | X              | X        | Asynchronous Reset;<br>Q <sub>0</sub> -Q <sub>7</sub> = LOW        |
| shH w                            | Н              | Н              | 1        | Parallel Load; I/On → Qn   |
| BO HI                            | 88 <u>E</u> 1  | H              |          | Shift Right; $DS_0 \rightarrow Q_0$ , $Q_0 \rightarrow Q_1$ , etc. |
| Н                                | Н              | L              | ~        | Shift Left, $DS_7 \rightarrow Q_7$ , $Q_7 \rightarrow Q_6$ , etc.  |
| Н                                | L              | L              | X        | Hold   |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

\_\_ = LOW-to-HIGH Transition



4-181

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )                     | -0.5V to $+7.0V$             |
|---|------------------------------|
| DC Input Diode Current (I <sub>IK</sub> )             |                              |
| $V_I = -0.5V$   | -20 mA                       |
| $V_I = V_{CC} + 0.5V$                                 | + 20 mA                      |
| DC Input Voltage (V <sub>I</sub> )                    | $-0.5$ V to $V_{CC} + 0.5$ V |
| DC Output Diode Current (IOK)                         |                              |
| $V_0 = -0.5V$   | -20 mA                       |
| $V_O = V_{CC} + 0.5V$                                 | +20 mA                       |
| DC Output Voltage (V <sub>O</sub> )                   | $-0.5$ V to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (IO)                 | ±50 mA                       |
| DC V <sub>CC</sub> or Ground Current                  |                              |
| Per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                       |
| Storage Temperature (T <sub>STG</sub> )               | -65°C to +150°C              |
| Junction Temperature (T <sub>J</sub> )                |                              |
| CDIP  | 175°C                        |
| DDID  | 140°C                        |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating 10 algo. Conditions

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices

| Supply Voltage (V <sub>CC</sub> ) (Unless Otherwise Specified) 'AC 'ACT   | 2.0V to 6.0V<br>4.5V to 5.0V      |
|---|-----------------------------------|
| Input Voltage (V <sub>I</sub> )   | 0V to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )  | 0V to V <sub>CC</sub>             |
| Operating Temperature (T <sub>A</sub> )<br>74AC/ACT<br>54AC/ACT   | -40°C to +85°C<br>-55°C to +125°C |
| Minimum Input Edge Rate (ΔV/Δt)  'AC Devices  V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V | 125 mV/ns                         |
|   |                                   |

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

#### DC Electrical Characteristics For 'AC Family Devices

|                 |                                      |                        | 74                      | AC                   | 54AC                              | 74AC                            |       |  |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | 25°C                 | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |  |
|                 |                                      |                        | Тур                     |                      | Guaranteed L                      | imits                           |       |  |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | ٧     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu\text{A}$  |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | V     | $\begin{tabular}{ll} *V_{\text{IN}} &= V_{\text{IL}} \text{ or } V_{\text{IH}} \\ &- 12 \text{ mA} \\ &- 24 \text{ mA} \\ &- 24 \text{ mA} \\ \end{tabular}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | V     | Ι <sub>ΟUT</sub> = 50 μΑ   |  |
|                 |                                      | 3.0<br>4.5<br>5.5      | 4                       | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              | 0.44<br>0.44<br>0.44            | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $V_{IOH}$ 24 mA   |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    | American Pro-           | ±0.1                 | ±1.0                              | ±1.0                            | μΑ    | $V_I = V_{CC}$ , GND   |  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    | son historia            | ±0.5                 | ± 10.0                            | fine vine (±5.0 a al marg       | μΑ    | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$   |  |

\*All outputs loaded; threshold on input associated with output under test.

†Maximum test duration 20 ms, one output loaded at a time.

#### 9

| DC Electrical Characteristics For 'AC Family Devices |  |
|--|--|
|--|--|

|        | ZAAC                                | 74AC                           |       | IAC  | 54AC                              | 74AC                            |       |  |  |
|--------|-------------------------------------|--------------------------------|-------|------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol | Parameter                           | V <sub>CC</sub> T <sub>A</sub> |       | 25°C | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |  |
|        | C <sub>L</sub> = 60 pF              |                                | Тур   | - 30 | Guaranteed Li                     |                                 |       |  |  |
| lold   | †Minimum Dynamic                    | 5.5                            | (SVA) | CHAR | 57                                | 86                              | mA    | $V_{OLD} = 1.65V Max$  |  |
| IOHD   | Output Current                      | 5.5                            |       | 07   | -50                               | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                            | 8.88  | 8.0  | 160 <sub>0,21</sub>               | 80                              | μΑ    | V <sub>IN</sub> = V <sub>CC</sub> or GND                                       |  |
| lozt   | Maximum I/O<br>Leakage Current      | 5.5                            | 17.8  | ±0.6 | ±11.0                             | ± 6.0                           | μΑ    | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |

<sup>\*</sup>All outputs loaded; threshold on input associated with output under test.

#### DC Electrical Characteristics For 'ACT Family Devices

|                 | 8.0 17.0 ns                          |                        | 744               | CT           | 54ACT                            | 8.6               | 74ACT                        | ±₽ 10         | O of RM  |  |
|-----------------|--------------------------------------|------------------------|-------------------|--------------|----------------------------------|-------------------|------------------------------|---------------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) |                   |              | T <sub>A</sub> = -55°C to +125°C | -40               | T <sub>A</sub> = °C to +85°C | Units         | Conditions   |  |
|                 | 8.0 19.6                             |                        | Тур               | 0.1          | Guaranteed L                     | imits             |                              | uT elder      | tezu Output B  |  |
| VIH             | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5        | 2.0          | 2.0                              | 4.8               | 2.0                          | V 1           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage      | 3.0<br>4.5             | 1.5               | 0.8          | 0.8                              | 6.0<br>a.a        | 0.8                          | n<br>sable Te | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub> | Minimum High Level                   | 4.5<br>5.5             | 4.49<br>5.49      | 4.4          | 4.4                              | 3.5               | 4.4<br>5.4                   | V             | $I_{OUT} = -50 \mu\text{A}$  |  |
|                 | en a.er o.s                          | 4.5<br>5.5             | 0.0001            | 3.86<br>4.86 | 3.70<br>4.70                     | 3.5               | 3.76<br>4.76                 | TO BY VO.     | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OH</sub> -24 mA<br>-24 mA  |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001    | 0.1<br>0.1   | 0.1<br>0.1                       | atm               | 0.1<br>0.1                   | V             | $I_{OUT} = 50 \mu A$   |  |
|                 | 74AC<br>A = - 40°C                   | 4.5<br>5.5             | 54AC<br>= -63°C   | 0.36<br>0.36 | 0.50<br>0.50                     | 'gaV              | 0.44<br>0.44                 | ٧             | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    | e 50 pf           | ±0.1         | ±1.0                             | (y)               | ±1.0                         | μΑ            | $V_I = V_{CC}$ , GND   |  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    | 9.6               | ±0.5         | ± 10.0                           | 3.3               | ±5.0 10 H                    | μΑ            | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |
| ICCT            | Maximum I <sub>CC</sub> /Input       | 5.5                    | 0.6               |              | 1.6                              | 200               | 1.5                          | mA            | $V_I = V_{CC} - 2.1V$  |  |
| IOLD            | †Minimum Dynamic                     | 5.5                    | 3.3               |              | 50                               | 5.0               | 75                           | mA            | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD            | Output Current                       | 5.5                    | 0,8               |              | -50                              | 8.8               | -75 H                        | mA            | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc             | Maximum Quiescent<br>Supply Current  | 5.5                    | 4.0               | 8.0          | 160                              | 3.3               | 80                           | μΑ            | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |
| lozt<br>V-S     | Maximum I/O<br>Leakage Current       | 5.5                    | 2.0<br>7.5<br>5.0 | ±0.6         | ±11.0                            | 8.8<br>8.6<br>5.0 | ±6.0 1 10 H                  | μΑ            | $V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$   |  |

Note: I<sub>CC</sub> limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| Symbol | Parameter                        | Тур | Units | Conditions      |
|--------|----------------------------------|-----|-------|-----------------|
| CIN    | Input Capacitance                | 4.5 | pF    | $V_{CC} = 5.5V$ |
| CPD    | Power Dissipation<br>Capacitance | 170 | pF    | $V_{CC} = 5.5V$ |

<sup>†</sup>Maximum test duration 20 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

ICC for 54AC @ 25°C is identical to 74AC @ 25°C.

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol           | Parameter  | (V)        | atimi       | C <sub>L</sub> = 50 p | unde-        |            | 50 pF        |            | 50 pF        | Units   | No.     |
|------------------|--|------------|-------------|-----------------------|--------------|------------|--------------|------------|--------------|---------|---------|
|                  | a nav An   | 8.0        | Min         | Тур                   | Max          | Min        | Max          | Min        | Max          | olmis81 | - a wal |
| f <sub>max</sub> | Maximum Input<br>Frequency   | 3.3<br>5.0 | 90<br>130   | 124<br>173            |              | 70<br>80   | i            | 80<br>105  | Dunwint.     | MHz     | CHO     |
| t <sub>PLH</sub> | Propagation Delay<br>CP to Q <sub>0</sub> or Q <sub>7</sub><br>(Shift Left or Right) | 3.3<br>5.0 | 8.5<br>5.5  | 14.0<br>9.5           | 20.5<br>14.0 | 1.0<br>1.0 | 25.5<br>17.5 | 7.0<br>4.5 | 22.0<br>15.0 | ns      | 2-3, 4  |
| tphL             | Propagation Delay<br>CP to Q <sub>0</sub> or Q <sub>7</sub><br>(Shift Left or Right) | 3.3<br>5.0 | 8.5<br>5.5  | 14.5<br>10.0          | 21.5<br>14.5 | 1.0        | 26.5<br>18.0 | 7.0<br>5.0 | 23.0<br>16.0 | ns      | 2-3, 4  |
| t <sub>PLH</sub> | Propagation Delay<br>CP to I/On  | 3.3<br>5.0 | 9.0<br>6.0  | 14.5<br>10.0          | 20.5<br>14.5 | 1.0<br>1.0 | 24.5<br>17.0 | 7.5<br>5.0 | 22.5<br>16.0 | ns      | 2-3, 4  |
| t <sub>PHL</sub> | Propagation Delay<br>CP to I/On  | 3.3<br>5.0 | 10.0<br>6.5 | 16.0<br>11.0          | 23.0<br>16.0 | 1.0        | 26.5<br>18.5 | 8.5<br>6.0 | 24.5<br>17.5 | ns      | 2-3, 4  |
| t <sub>PHL</sub> | Propagation Delay MR to Q <sub>0</sub> or Q <sub>7</sub>                             | 3.3<br>5.0 | 9.0<br>5.5  | 15.5<br>10.5          | 22.5<br>15.5 | 1.0<br>1.0 | 27.0<br>18.5 | 7.5<br>5.0 | 25.0<br>17.0 | ns      | 2-3, 4  |
| t <sub>PHL</sub> | Propagation Delay MR to I/On   | 3.3<br>5.0 | 9.0<br>5.5  | 15.0<br>10.0          | 21.5<br>15.0 | 1.0        | 26.5<br>18.0 | 7.5<br>5.0 | 24.0<br>16.5 | ns      | 2-3, 4  |
| t <sub>PZH</sub> | Output Enable Time   | 3.3<br>5.0 | 7.0<br>4.5  | 12.0<br>8.5           | 18.0<br>12.5 | 1.0        | 22.0<br>15.0 | 6.0        | 19.5<br>13.5 | ns      | 2-5     |
| t <sub>PZL</sub> | Output Enable Time OE to I/On  | 3.3<br>5.0 | 7.0<br>5.0  | 12.5<br>8.0           | 18.0<br>12.5 | 1.0        | 23.5<br>16.0 | 6.0<br>4.0 | 20.5         | ns      | 2-6     |
| t <sub>PHZ</sub> | Output Disable Time OE to I/On   | 3.3<br>5.0 | 6.5<br>3.5  | 13.0<br>9.5           | 18.5<br>14.0 | 1.0        | 22.5<br>17.0 | 5.5<br>3.0 | 19.5<br>15.0 | ns      | 2-5     |
| t <sub>PLZ</sub> | Output Disable Time  | 3.3<br>5.0 | 5.5<br>3.5  | 11.5<br>8.0           | 17.0<br>12.5 | 1.0<br>1.0 | 21.5<br>16.0 | 4.5<br>2.0 | 19.0<br>13.5 | ns      | 2-6     |

<sup>\*</sup>Voltage Range 3.3 is 3.3V  $\pm$ 0.3V. Voltage Range 5.0 is 5.0V  $\pm$ 0.5V.

## 

|                        | - NIA.   |                   | 74           | AC         | 54AC  | 74AC   |         |        |
|------------------------|--|-------------------|--------------|------------|---|--|---------|--------|
| Symbol                 | Parameter  | V <sub>CC</sub> * |              |            | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units   | Fig.   |
|                        | 27   |                   | Тур          |            | Guaranteed Min  | imum   | Leakays |        |
| t <sub>s quality</sub> | Setup Time, HIGH or LOW<br>S <sub>0</sub> or S <sub>1</sub> to CP  | 3.3<br>5.0        | 3.0<br>2.0   | 8.0<br>5.0 | 9.5<br>7.0  | 8.5<br>5.5   | ns      | 2-7    |
| t <sub>h</sub>         | Hold Time, HIGH or LOW<br>S <sub>0</sub> or S <sub>1</sub> to CP   | 3.3<br>5.0        | -3.0<br>-1.5 | 0.5<br>1.0 | 2.0<br>2.5  | 0.5<br>1.0   | ns      | 2-7    |
| ts                     | Setup Time, HIGH or LOW I/On to CP                                 | 3.3<br>5.0        | 2.0          | 5.5<br>3.5 | 6.0<br>4.0  | 6.0<br>4.0   | ns      | 2-7    |
| t <sub>h</sub>         | Hold Time, HIGH or LOW I/On to CP                                  | 3.3<br>5.0        | -2.0<br>-1.0 | 0          | 1.5<br>2.0  | 1.0  | ns      | 2-7    |
| t <sub>s</sub> galo a  | Setup Time, HIGH or LOW DS <sub>0</sub> or DS <sub>7</sub> to CP   | 3.3<br>5.0        | 2.5<br>1.5   | 6.5<br>4.0 | 7.5<br>5.0  | 7.0<br>4.5   | ns      | 2-7    |
| t <sub>h</sub>         | Hold Time, HIGH or LOW<br>DS <sub>0</sub> or DS <sub>7</sub> to CP | 3.3<br>5.0        | -2.0<br>-1.0 | 0<br>1.0   | 1.5<br>1.5  | 0.5<br>1.0   | ns      | 2-7    |
| t <sub>w</sub>         | CP Pulse Width, LOW  | 3.3<br>5.0        | 3.5<br>2.0   | 4.5<br>3.5 | 5.5<br>5.0  | 5.0<br>3.5   | ns      | 2-3    |
| t <sub>w</sub>         | MR Pulse Width, LOW  | 3.3<br>5.0        | 4.0          | 4.5<br>3.5 | 5.5<br>5.0  | 5.0<br>3.5   | ns      | 2-3    |
| t <sub>rec</sub>       | Recovery Time MR to CP   | 3.3<br>5.0        | 0 0.5        | 1.5<br>1.5 | 2.5<br>2.5  | 1.5  | ns      | 2-3, 7 |

<sup>\*</sup>Voltage Range 3.3 is 3.3V ±0.3V \*Voltage Range 5.0 is 5.0V ±0.5V

|                    |  |                          |     | 74ACT  |              | 54/     | ACT   | 74/ | ACT  | PER E |                    |
|--------------------|--|--------------------------|-----|--|--------------|---------|---|-----|--|-------|--------------------|
| Symbol             | Parameter  | V <sub>CC</sub> *<br>(V) |     | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              |         | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |       | Fig.<br>No.        |
|                    |  |                          | Min | Тур  | Max          | Min     | Max   | Min | Max  | Alv   | and do for         |
| f <sub>max</sub>   | Maximum Input<br>Frequency   | 5.0                      | 120 | 170  | on s<br>an b | 70      | eag:  | 110 | vers<br>ebro   | MHz   | l C3+5<br>el trica |
| t <sub>PLH</sub>   | Propagation Delay<br>CP to Q <sub>0</sub> or Q <sub>7</sub><br>(Shift Left or Right) | 5.0                      | 4.0 | 8.5  | 12.5         | 1.0     | 15.5  | 3.0 | 14.0   | ns    | 2-3, 4             |
| t <sub>PHL</sub> . | Propagation Delay<br>CP to Q <sub>0</sub> or Q <sub>7</sub><br>(Shift Left or Right) | 5.0                      | 4.0 | 9.0  | 13.5         | 1.0 Oil | 16.0  | 3.5 | 15.0   | ns    | 2-3, 4             |
| t <sub>PLH</sub>   | Propagation Delay<br>CP to I/On  | 5.0                      | 4.5 | 8.5  | 12.5         | 1.0     | 15.0  | 4.5 | 13.5   | ns    | 2-3, 4             |
| t <sub>PHL</sub>   | Propagation Delay<br>CP to I/On  | 5.0                      | 5.0 | 9.5  | 15.0         | 1.0     | 18.0  | 4.5 | 16.5   | ns    | 2-3, 4             |
| t <sub>PHL</sub>   | Propagation Delay MR to Q <sub>0</sub> or Q <sub>7</sub>                             | 5.0                      | 4.0 | 14.0   | 15.0         | 1.0     | 18.0  | 4.0 | 18.0   | ns    | 2-3, 4             |
| t <sub>PHL</sub>   | Propagation Delay MR to I/On   | 5.0                      | 4.0 | 13.0   | 14.5         | 1.0     | 17.5  | 3.5 | 17.5   | ns    | 2-3, 4             |
| t <sub>PZH</sub>   | Output Enable Time OE to I/On  | 5.0                      | 2.5 | 8.0  | 12.0         | 1.0     | 14.0  | 1.5 | 13.0   | ns    | 2-5                |
| t <sub>PZL</sub>   | Output Enable Time OE to I/On  | 5.0                      | 2.0 | 8.0  | 12.0         | 1.0     | 14.5  | 1.5 | 13.5   | ns    | 2-6                |
| t <sub>PHZ</sub>   | Output Disable Time OE to I/On   | 2.5                      | 2.0 | 8.5  | 12.5         | 1.0     | 14.5  | 2.0 | 13.5   | ns    | 2-5                |
| t <sub>PLZ</sub>   | Output Disable Time OE to I/On   | 2.0                      | 2.5 | 8.0  | 11.5         | 1.0     | 14.0  | 2.0 | 12.5   | ns    | 2-6                |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

#### AC Operating Requirements: See Section 2 for Waveforms

|                  | 01 010  |                   | 744  | СТ  | 54ACT   | 74ACT  | Marie Take |             |
|------------------|---|-------------------|--|-----|---|--|------------|-------------|
| Symbol           | Parameter   | V <sub>CC</sub> * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |     | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units      | Fig.<br>No. |
|                  | Pin Assignment  |                   | Тур  | 1   | Guaranteed Min  | imum   |            |             |
| ts               | Setup Time, HIGH or LOW<br>S <sub>0</sub> or S <sub>1</sub> to CP | 5.0               | 2.0  | 5.0 | 6.5   | 5.5  | ns         | 2-7         |
| th               | Hold Time, HIGH or LOW<br>S <sub>0</sub> or S <sub>1</sub> to CP  | 5.0               | -2.0                                       | 1.0 | 1.5   | 1.0  | ns         | 2-7         |
| ts               | Setup Time, HIGH or LOW   | 5.0               | 1.5  | 4.0 | 4.5   | 4.5  | ns         | 2-7         |
| th               | Hold Time, HIGH or LOW  | 5.0               | -1.0                                       | 1.0 | 1.5   | 0.1 Deed   | ns         | 2-7         |
| ts               | Setup Time, HIGH or LOW DS <sub>0</sub> or DS <sub>7</sub> to CP  | 5.0               | 1.5  | 4.5 | 5.5   | 5.0  | ns         | 2-7         |
| th               | Hold Time, HIGH or LOW DS <sub>0</sub> or DS <sub>7</sub> to CP   | 5.0               | -1.0                                       | 1.0 | 1.5   | m Joe 1.0 boM  | ns         | 2-7         |
| t <sub>w</sub>   | CP Pulse Width<br>HIGH or LOW                                     | 5.0               | 2.0  | 4.0 | atuani 5.0 nel fuo  | 4.5  | ns         | 2-3         |
| t <sub>w</sub>   | MR Pulse Width, LOW   | 5.0               | 2.0  | 3.5 | 5.0   | 3.5  | ns         | 2-3         |
| t <sub>rec</sub> | Recovery Time MR to CP  | 5.0               | 0  | 1.5 | 1.5   | studiu 1.5 ehe8  | ns         | 2-3,7       |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$  0.5V.



### 54ACT/74ACT323 8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

#### **General Description**

The 'ACT323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Qo and Q7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

#### **Features**

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and

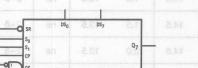
AC Electrical Characteristics: See Section 2 for

Symbol

- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- TTL-compatible inputs

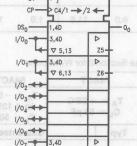
#### Ordering Code: See Section 8

#### **Logic Symbols**



CP 07 1/00 1/01 1/02 1/03 1/04 1/05 1/06 1/07 1,4D 3,4D ▽ 5,13 3,4D ♥ 6,13

1/02



♥ 12,13

2,4D

SRG8

3FN13

SR-

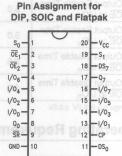
OE2-

TL/F/9787-5

Z12-

| Pin Name                              | Description                         |  |
|---------------------------------------|-------------------------------------|--|
| CP                                    | Clock Pulse Input                   |  |
| DS <sub>0</sub>                       | Serial Data Input for Right Shift   |  |
| DS <sub>7</sub>                       | Serial Data Input for Left Shift    |  |
| S <sub>0</sub> , S <sub>1</sub>       | Mode Select Inputs                  |  |
| SR                                    | Synchronous Reset Input             |  |
| $\overline{OE}_1$ , $\overline{OE}_2$ | TRI-STATE Output Enable Inputs      |  |
| 1/00-1/07                             | Multiplexed Parallel Data Inputs or |  |
| ns 2-3                                | TRI-STATE Parallel Data Outputs     |  |
| Q <sub>0</sub> , Q <sub>7</sub>       | Serial Outputs                      |  |
|                                       |                                     |  |

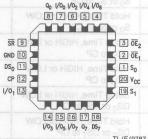
#### **Connection Diagrams**



TL/F/9787-2

DA

Symt.



**Pin Assignment** 

for LCC

TL/F/9787-3

in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode.  $Q_0$  and  $Q_7$  are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \$\overline{SR}\$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP.

A HIGH signal on either  $\overline{OE}_1$  or  $\overline{OE}_2$  disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S $_0$  and S $_1$  in preparation for a parallel load operation.

#### Mode Select Table

| Inputs |                |                |    | Response  |
|--------|----------------|----------------|----|---|
| SR     | S <sub>1</sub> | S <sub>0</sub> | СР | Tiesponse Tiesponse   |
| L      | X              | X              | _  | Synchronous Reset; Q <sub>0</sub> -Q <sub>7</sub> = LOW         |
| Н      | Н              | Н              | _  | Parallel Load; I/O <sub>n</sub> → Q <sub>n</sub>                |
| Н      | L              | Н              | _  | Shift Right; $DS_0 \rightarrow Q_0, Q_0 \rightarrow Q_1$ , etc. |
| Н      | Н              | L              | _  | Shift Left; $DS_7 \rightarrow Q_7, Q_7 \rightarrow Q_6$ , etc.  |
| Н      | L              | L              | X  | Hold  |

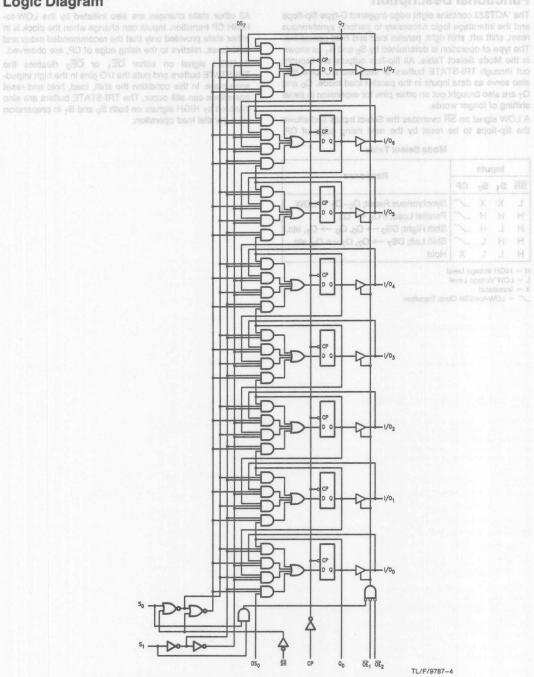
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Clock Transition

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office, Distributors for availabil   | ity and specimentions.       |
|--|------------------------------|
| Supply Voltage (V <sub>CC</sub> )  | -0.5V to $+7.0V$             |
| DC Input Diode Current (I <sub>IK</sub> )  |                              |
| $V_1 = -0.5V$<br>$V_1 = V_{CC} + 0.5V$   | -20 mA<br>+20 mA             |
| DC Input Voltage (V <sub>I</sub> )   | $-0.5V$ to $V_{CC} + 0.5V$   |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$                                      | -20 mA                       |
| $V_O = V_{CC} + 0.5V$  | + 20 mA                      |
| DC Output Voltage (V <sub>O</sub> )  | $-0.5$ V to $V_{CC} + 0.5$ V |
| DC Output Source or Sink Current (I <sub>O</sub> )   | 8.81 0.1 ±50 mA              |
| DC V <sub>CC</sub> or Ground Current Per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | 0.8† ±50 mA                  |
| Storage Temperature (T <sub>STG</sub> )  | -65°C to +150°C              |
| Junction Temperature (T <sub>J</sub> )   |                              |
| a CDIP an O.ST O.S   | 175°C                        |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications,

#### **Recommended Operating** Conditions

| 'AC 'ACT   | Parameter      | 2.0V to 6.0V<br>4.5V to 5.5V |
|--|----------------|------------------------------|
| Input Voltage (V <sub>I</sub> )                  |                | 0V to V <sub>CC</sub>        |
| Output Voltage (V <sub>O</sub> )                 |                | 0V to V <sub>CC</sub>        |
| Operating Temperature (T <sub>A</sub> ) 74AC/ACT | um Input Frequ | -40°C to +85°C               |

-55°C to +125°C 54AC/ACT Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> 125 mV/ns V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V 125 mV/ns V<sub>CC</sub> @ 4.5V, 5.5V

**DC Electrical Characteristics For 'ACT Family Devices** 

|                    | TORFT                                | 1                      | 74               | ACT          | 1339   | 54ACT                            |        | 74ACT                            |                |   |  |
|--------------------|--------------------------------------|------------------------|------------------|--------------|--------|----------------------------------|--------|----------------------------------|----------------|---|--|
| Symbol             | Parameter of                         | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       |        | T <sub>A</sub> =<br>C to + 125°C | -40    | T <sub>A</sub> =<br>0°C to +85°C | Units          | Conditions  |  |
| -027               | CL = 50 9F                           | YA.B                   | Тур              | 1            | +5.0   | Guaranteed L                     | imits  |                                  |                |   |  |
| V <sub>IH</sub>    | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0          |        | 2.0                              |        | 2.0<br>2.0                       | ٧              | $V_{OUT} = 0.1V$<br>or $V_{CC} = 0.1V$  |  |
| V <sub>IL</sub> -S | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5              | 0.8          | 8      | 0.8<br>0.8                       | 5.0    | 0.8                              | V              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>    | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 1      | 4.4<br>5.4                       | 5.0    | 4.4<br>5.4                       | V              | $I_{OUT} = -50 \mu\text{A}$   |  |
|                    | 4.5 ns                               | 4.5<br>5.5             | 4.5              | 3.86<br>4.86 | 1,5.   | 3.70<br>4.70                     | 6.8    | 3.76<br>4.76                     | tme, HI<br>Sov | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OH</sub> -24 mA<br>-24 mA |  |
| V <sub>OL</sub>    | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1   |        | 0.1<br>0.1                       | 5.0    | 0.1<br>0.1                       | E.V.           | $I_{OUT} = 50 \mu A$  |  |
|                    | 2.5 ns                               | 4.5<br>5.5             | 0.8              | 0.36<br>0.36 | 9      | 0.50<br>0.50                     | 5.0    | 0.44<br>0.44                     | Pile Smith     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = -24 \text{ mA}$ $V_{IN} = -24 \text{ mA}$ |  |
| I <sub>IN</sub>    | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         |        | ±1.0                             |        | ±1.0                             | μА             | V <sub>I</sub> = V <sub>CC</sub> , GND  |  |
| loz                | Maximum TRI-STATE<br>Current         | 5.5                    | 50.50            | ±0.5         |        | ±10.0                            | 7.0    | ±5.0                             | μΑ             | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| lozt               | Maximum I/O<br>Leakage Current       | 5.5                    |                  | ±0.6         |        | ±11.0                            |        | ±6.0                             | μΑ             | $V_{I/O} = V_{CC}$ or GND<br>$V_{IN} = V_{IH}$ , $V_{IL}$                                 |  |
| Ісст               | Maximum I <sub>CC</sub> /Input       | 5.5                    | 0.6              | Con          | esinti | 1.6                              |        | 1.5 jemens                       | mA             | $V_I = V_{CC} - 2.1V$   |  |
| I <sub>OLD</sub>   | †Minimum Dynamic Output              | 5.5                    | = 5.0V           | ooV          | Äq     | 50                               |        | 75 acoustic                      | mA             | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub>   | Current                              | 5.5                    | va.e =           | DOV          | Fig    | -50                              | itence | -75 modes                        | mA             | V <sub>OHD</sub> = 3.85V Min  |  |
| ICC                | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          |        | 160                              |        | 80                               | μΑ             | $V_{IN} = V_{CC}$ or GND  |  |

<sup>\*</sup>All outputs loaded: thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms. one output loaded at a time.

Note: ICC for 54ACT is identical to 74ACT @ 25°C.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                  |   | (00V)                    |   | 74ACT | Sales  | 54/   | ACT  | 74   | ACT     | adnos s | please      |
|------------------|---|--------------------------|---|-------|--------|---|------|--|---------|---------|-------------|
| Symbol           | Parameter   | V <sub>CC</sub> *<br>(V) | T <sub>A</sub> = 25°C<br>C <sub>L</sub> = 50 pF |       |        | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |         | Units   | Fig.<br>No. |
|                  | /0  | (oV)                     | Min I   | Тур   | Max    | Min   | Max  | Min  | Max     | -0.5V   | E (V)       |
| f <sub>max</sub> | Maximum Input Frequency                                     | 5.0                      | 120   | 125   | V8:0 - | 95  | -0.5 | 110  | (iV) er | MHz     | ini 20      |
| tpLH             | Propagation Delay<br>CP to Q <sub>0</sub> or Q <sub>7</sub> | 5.0                      | 5.0   | 9.0   | 12.5   | 1.0   | 16.5 | 4.0  | 14.0    | ns      | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>CP to Q <sub>0</sub> or Q <sub>7</sub> | 5.0                      | 5.0   | 9.0   | 13.5   | 1.0   | 17.0 | 4.5  | 15.0    | ns      | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay<br>CP to I/On                             | 5.0                      | 5.0   | 8.5   | 12.5   | 1.0   | 16.5 | 4.5  | 14.5    | ns      | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>CP to I/On                             | 5.0                      | 6.0   | 10.0  | 14.5   | 1.0   | 18.0 | 5.0  | 16.0    | ns      | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time  | 5.0                      | 3.5   | 7.5   | 11.0   | 1.0   | 15.0 | 3.0  | 12.5    | ns      | 2-5         |
| t <sub>PZL</sub> | Output Enable Time  | 5.0                      | 3.5   | 7.5   | 11.5   | 1.0   | 15.5 | 3.0  | 13.0    | ns      | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time   | 5.0                      | 4.0   | 8.5   | 12.5   | 1.0   | 15.5 | 3.0  | 13.5    | ns      | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time   | 5.0                      | 3.0   | 8.0   | 11.5   | 1.0   | 15.0 | 2.5  | 12.5    | ns      | 2-6         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

#### AC Operating Requirements: See Section 2 for Waveforms

|                                    |                    | T  | TOAKS             |                   | 744             | CT            | 54ACT  | 74ACT   |                       | - SIR       |
|------------------------------------|--------------------|--|-------------------|-------------------|-----------------|---------------|--|---|-----------------------|-------------|
| Symbol                             | Parameter          |  | $\tau_A =$        | V <sub>CC</sub> * | TA = CL = VCC = | DATE: \$10 TO | $T_A = -55^{\circ}C$<br>$to + 125^{\circ}C$<br>$C_L = 50 \text{ pF}$<br>$V_{CC} = +5.0V$ | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF<br>V <sub>CC</sub> = +5.0V | Units                 | Fig.<br>No. |
| V1.0                               | # TUOV             | V  | 2.0               |                   | Тур             | 0.3           | Guaranteed Min   | TOWN I VISITED W  | urninilyi<br>W turnil | HIV         |
| ts V1.0                            | Setup 7<br>So or S |  | GH or LOW         | 5.0               | 2.0             | 5.0           | 8.6.0 a.A  | 145.01 Wo.1 m   | amb <b>ns</b> /       | 2-7         |
| t <sub>h</sub> As <sub>1</sub> 03- | Hold Ti            |  | H or LOW          | 5.0               | 4.0             | 1.5           | 84 1.5 2.4   | le1.5 doll n  | ns<br>tugino          | 2-7         |
| ts IIV 10 JIV<br>Am 48 —           |                    | ime, HIC<br>S <sub>0</sub> , DS <sub>7</sub> | H or LOW<br>to CP | 5.0               | 1.0             | 4.0 88        | 4.5  | 4.5   | ns                    | 2-7         |
| th Au 08                           |                    | me, HIGI<br>S <sub>0</sub> , DS <sub>7</sub> | H or LOW<br>to CP | 5.0               | 0.0             | 1.0           | 1.0 2.3  | la1.0 wo.l m  | man ns                | 2-7         |
| t <sub>s</sub> <sub>HV</sub> 10 HV | Setup T            |  | H or LOW          | 5.0               | 1.0             | 2.5           | 3.0  | 2.5   | ns                    | 2-7         |
| th IS-                             | Hold Ti            |  | H or LOW          | 5.0               | 0               | 1.0           | 1.0  | 1.0<br>tugol co   | ns                    | 2-7         |
| t <sub>w</sub>                     | CP Puls<br>HIGH o  | e Width                                      | 0.7.1             | 5.0               | 2.0             | 4.0           | 5.0  | 4.5   | ns                    | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

| Symbol | Parameter                     | Тур | Units | Conditions      |
|--------|-------------------------------|-----|-------|-----------------|
| CIN    | Input Capacitance             | 4.5 | pF    | $V_{CC} = 5.0V$ |
| CPD    | Power Dissipation Capacitance | 170 | pF    | $V_{CC} = 5.0V$ |



### 54ACT/74ACT367 Hex Buffer with TRI-STATE® Outputs

#### **General Description**

The 'ACT367 contains six independent non-inverting buffers with TRI-STATE outputs.

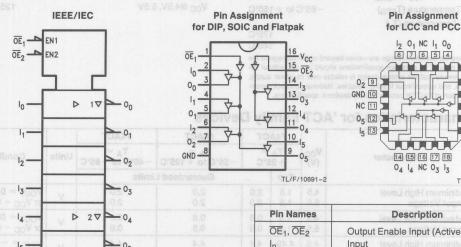
#### **Features**

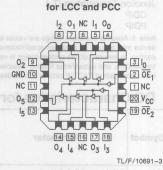
- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs Va.0 + ooV = oV

Ordering Code: See Section 8

#### **Logic Symbol**

# Connection Diagrams





| Pin Names                         | Description                      |
|-----------------------------------|----------------------------------|
| OE <sub>1</sub> , OE <sub>2</sub> | Output Enable Input (Active LOW) |
| AS AABal A                        | Input leve I rigit repminist     |
| 0 0 a a                           | Output spatioV lugtuO            |

#### **Function Table**

| 1.0     |
|---------|
| Outputs |
| 0       |
| ₽H0-    |
| 0.Lm    |
| Z       |
|         |

TL/F/10691-1

L = LOW Voltage Level

H = HIGH Voltage Level

X = Immaterial

Z = High Impedance

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V<sub>CC</sub>) -0.5V to +7.0VDC Input Diode Current (IIK)  $V_1 = -0.5V$ -20 mA +20 mA  $V_I = V_{CC} + 0.5V$ DC Input Voltage (VI) -0.5V to  $V_{CC} + 0.5V$ DC Output Diode Current (IOK)  $V_0 = -0.5V$ -20 mA  $V_O = V_{CC} + 0.5V$ + 20 mA -0.5V to  $V_{CC} + 0.5V$ DC Output Voltage (Vo) DC Output Source or Sink Current (IO) ±50 mA

 DC V<sub>CC</sub> or Ground Current
 ±50 mA

 Storage Temperature (T<sub>STG</sub>)
 −65°C to +150°C

Junction Temperature (T<sub>J</sub>)
CDIP 175°C
PDIP 140°C

Note 1: Absolute maximum ratings are values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>)
'AC
'ACT

2.0V to 6.0V 4.5V to 5.5V

Input Voltage (V<sub>I</sub>)
Output Voltage (V<sub>O</sub>)

0V to V<sub>CC</sub>

Operating Temperature (T<sub>A</sub>)

74AC/ACT 54AC/ACT -40°C to +85°C -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

 $V_{IN}$  from 30% to 70% of  $V_{CC}$   $V_{CC}$  @3.3V, 4.5V, 5.5V

125 mV/ns

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices V<sub>IN</sub> from 0.8V to 2.0V

V<sub>CC</sub> @4.5V, 5.5V

125 mV/ns

#### **DC Characteristics for 'ACT Family Devices**

| Can per          |                                     | -                      | 744                             | СТ           | 54ACT                            | 74ACT                           |                        | James 1  |  |
|------------------|-------------------------------------|------------------------|---------------------------------|--------------|----------------------------------|---------------------------------|------------------------|--|--|
| Symbol           | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> =<br>+ 25°C      |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                  | Conditions   |  |
|                  | 37                                  | 1536                   | Тур                             |              | Guaranteed I                     | Limits                          | NAME OF TAXABLE PARTY. |  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5                      | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧                      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5                      | 0.8          | 0.8<br>0.8                       | 0.8                             | V                      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>  | Minimum High Level Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49                    | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V                      | $I_{OUT} = -50 \mu\text{A}$  |  |
|                  | Sov.                                | 4.5<br>5.5             | toV WQL<br>bV HOIH<br>loufemint | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V                      | $\begin{tabular}{ll} *V_{IN} = V_{IL} \mbox{ or } V_{IH} \\ -24 \mbox{ mA} \\ -24 \mbox{ mA} \end{tabular}$            |  |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage | 4.5<br>5.5             | 0.001<br>0.001                  | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1<br>0.1                      | ٧                      | $I_{OUT} = 50 \mu A$   |  |
|                  |                                     | 4.5<br>5.5             |                                 | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | V                      | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ 24 \mbox{ mA} \\ I_{OL} & 24 \mbox{ mA} \\ \end{tabular}$ |  |
| I <sub>IN</sub>  | Maximum Input Leakage Current       | 5.5                    |                                 | ±0.1         | ±1.0                             | ±1.0                            | μΑ                     | $V_I = V_{CC}$ , GND   |  |
| loz              | Maximum TRI-STATE<br>Current        | 5.5                    |                                 | ±0.5         | ± 10.0                           | ±5.0                            | μА                     | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |
| ICCT             | Maximum<br>I <sub>CC</sub> /Input   | 5.5                    | 0.6                             |              | 1.6                              | 1.5                             | mA                     | $V_I = V_{CC} - 2.1V^{\dagger\dagger}$   |  |
| I <sub>OLD</sub> | †Minimum Dynamic                    | 5.5                    |                                 |              | 50                               | 75                              | mA                     | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub> | Output Current                      | 5.5                    |                                 |              | -50                              | -75                             | mA                     | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5                    |                                 | 8.0          | 160.0                            | 80.0                            | μА                     | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C

<sup>††</sup>May be measured per the JEDEC alternate method.

| Symbol           | Sympol              | Parameter | (V) |     | C <sub>L</sub> = 50 | pF         |             | 125°C<br>50 pF |      | 85°C<br>50 pF | Units  | No. |
|------------------|---------------------|-----------|-----|-----|---------------------|------------|-------------|----------------|------|---------------|--------|-----|
|                  |                     | atuqi     | Min | Тур | Max                 | Min        | Max         | Min            | Max  | evni          | xsh    |     |
| t <sub>PLH</sub> | Propagation Delay   | 5.0       | 1.0 | 6.5 | 9.0                 |            |             | 1.0            | 10.0 | ns            | 2-3, 4 |     |
| t <sub>PHL</sub> | Propagation Delay   | 5.0       | 1.0 | 6.5 | 9.0                 |            |             | 1.0            | 10.0 | ns            | 2-3, 4 |     |
| t <sub>PZH</sub> | Output Enable Time  | 5.0       | 1.0 | 8.0 | 10.5                | ritiw aren | nverting bu | 1.0            | 11.0 | ns            | 2-5    |     |
| tpzL             | Output Enable Time  | 5.0       | 1.0 | 9.5 | 12.0                |            |             | 1.0            | 13.0 | ns            | 2-6    |     |
| t <sub>PHZ</sub> | Output Disable Time | 5.0       | 1.0 | 9.5 | 12.0                |            |             | 1.0            | 13.0 | ns            | 2-5    |     |
| t <sub>PLZ</sub> | Output Disable Time | 5.0       | 1.0 | 8.0 | 10.5                |            |             | 1.0            | 11.5 | ns            | 2-6    |     |

\*Voltage range 5.0 is 5.0V  $\pm$  0.5V.

| Symbol          | Parameter                     | Тур    | Units | Conditions      |
|-----------------|-------------------------------|--------|-------|-----------------|
| CIN             | Input Capacitance             | 4.5    | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 45.0   | pF    | $V_{CC} = 5.0V$ |
| OME S           | NO DE LA COMPANIA             | بالقرر | 17/2  | r) 60           |
|                 |                               |        |       |                 |
|                 |                               |        |       |                 |



# 54ACT/74ACT368 Hex Inverter Buffer with TRI-STATE® Outputs

#### **General Description**

The 'ACT368 contains six independent inverting buffers with TRI-STATE outputs.

#### **Features**

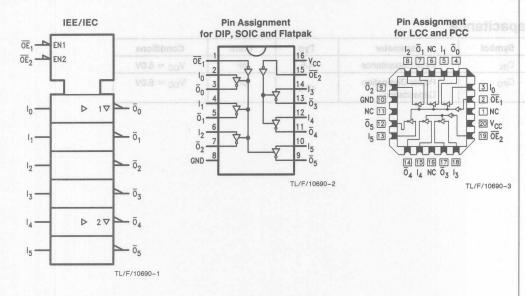
- Outputs source/sink 24 mA
- 'ACT has TTL-compatible inputs

les my2

Ordering Code: See Section 8

#### **Logic Symbols**

#### **Connection Diagrams**



#### **Function Table**

| Inpu         | uts | Output |  |
|--------------|-----|--------|--|
| OE<br>L<br>L | 1   | ō      |  |
| L            | L   | Н      |  |
| L            | Н   | L      |  |
| Н            | X   | Z      |  |

| Pin Names                             | Description                            |
|---------------------------------------|--|
| $\overline{OE}_1$ , $\overline{OE}_2$ | Output Enable Input (Active LOW) Input |
| $\overline{O}_n$                      | Output                                 |

L = LOW Voltage Level

H = HIGH Voltage Level

X = Immaterial

Z = High Impedance

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for available   | ility and specifications.    |
|--|------------------------------|
| Supply Voltage (V <sub>CC</sub> )  | -0.5V to $+7.0$ V            |
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$                                       | −20 mA<br>+20 mA             |
| $V_1 = V_{CC} + 0.5V$  |                              |
| DC Input Voltage (V <sub>I</sub> )   | $-0.5V$ to $V_{CC} + 0.5V$   |
| DC Output Diode Current (IOK)  |                              |
| $V_{O} = -0.5V$<br>$V_{O} = V_{CC} + 0.5V$   | -20 mA<br>+20 mA             |
| DC Output Voltage (V <sub>O</sub> )  | $-0.5$ V to $V_{CC} + 0.5$ V |
| DC Output Source<br>or Sink Current (I <sub>O</sub> )                                      | ±50 mA                       |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                       |
| Storage Temperature (T <sub>STG</sub> )  | -65°C to +150°C              |
| Junction Temperature (T <sub>J</sub> ) CDIP  | 175°C                        |
| PDIP   | 140°C                        |
|  |                              |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating 19913 001 Conditions

| AU   |         | 2.0V to 6.0V<br>4.5V to 5.5V      |
|--|---------|-----------------------------------|
| Input Voltage (V <sub>I</sub> )  |         | 0V to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )   |         | 0V to V <sub>CC</sub>             |
| 34AU/AU1   | 5.5     | -40°C to +85°C<br>-55°C to +125°C |
| Minimum Input Edge Ra<br>'AC Devices<br>V <sub>IN</sub> from 30% to 70%<br>V <sub>CC</sub> @3.3V, 4.5V, 5.5' | 6 of    |                                   |
| 'ACT Devices<br>V <sub>IN</sub> from 0.8V to 2.0\  | l turqi | ΔV/Δt) 125 mV/ns                  |

#### DC Electrical Characteristics for 'ACT Family Devices

|                   | an 0.01 0.1                          |            | 74               | ACT          | 54ACT                             | 74ACT                           | jation i | 89019 H.191   |  |
|-------------------|--------------------------------------|------------|------------------|--------------|-----------------------------------|---------------------------------|----------|---|--|
| Symbol            | Parameter                            |            | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units    | Conditions  |  |
| 8-8               | en 0,81 0,1                          |            | Тур              | 12.0         | Guaranteed Li                     | mits emil e                     | Enabl    | 1 <sub>PZL</sub> Output   |  |
| V <sub>IH</sub> S | Minimum High Level<br>Input Voltage  | 4.5<br>5.5 | 1.5<br>1.5       | 2.0          | 2.0                               | 2.0                             | ٧        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub>   | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5 | 1.5<br>1.5       | 0.8<br>0.8   | 0.8<br>0.8                        | 0.8                             | VV       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>   | Minimum High Level<br>Output Voltage | 4.5<br>5.5 | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | V        | $I_{OUT} = -50 \mu A$   |  |
|                   | Conditions Voc = 5.0V                | 4.5<br>5.5 | atint<br>Hq      | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | V        | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub>   | Maximum Low Level Output Voltage     | 4.5<br>5.5 | 0.001<br>0.001   | 0.1<br>0.1   | 0.0 0.1<br>0.1                    | 0.1                             | ٧        | $I_{OUT} = 50 \mu A$  |  |
|                   |                                      | 4.5<br>5.5 |                  | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | V        | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub>   | Maximum Input Leakage Current        | 5.5        |                  | ±0.1         | ±1.0                              | ±1.0                            | μΑ       | $V_I = V_{CC}$ , GND  |  |
| loz               | Maximum TRI-STATE<br>Current         | 5.5        |                  | ±0.5         | ±10.0                             | ±5.0                            | μА       | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Electrical Characteristics for 'ACT Family Devices (Continued)

| Symbol |                                     |                        | 74                          | ACT                        | 54ACT                            | 74ACT                           | dir sosi<br>dire kin |                              |  |
|--------|-------------------------------------|------------------------|-----------------------------|----------------------------|----------------------------------|---------------------------------|----------------------|------------------------------|--|
|        |                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> =            | + 25°C                     | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                | Conditions                   |  |
|        |                                     |                        | Тур                         | out Voltage                | Guaranteed Lin                   | mits                            | sel) trien           |                              |  |
| ГССТ   | Maximum<br>I <sub>CC</sub> /Input   | 5.5                    | 0.6                         | ilpul Volta<br>seraling Te | 1.6 05 +                         | 1.5                             | mA                   | $V_I = V_{CC} - 2.1V$ ††     |  |
| lold   | †Minimum Dynamic                    | 5.5                    |                             | EGANOANE                   | 50                               | 75 (xc                          | mA                   | V <sub>OLD</sub> = 1.65V Max |  |
| IOHD   | Output Current                      | 5.5                    | egbB ki                     | gal mumin                  | -50                              | -75                             | mA                   | V <sub>OHD</sub> = 3.85V Min |  |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | 18<br>0% to 7<br>1. 4.5V. 5 | 8.0                        | 160.0 + 00                       | of V8.0 <sub>80.0</sub>         | μΑ                   | $V_{IN} = V_{CC}$ or GND     |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

#### AC Electrical Characteristics: See Section 2 for Waveforms

| Symbol           |                     |                   |  | 74ACT   | epama  | e stoletie t | 54ACT  | 744 | CT          | n etricedA | Note 1: |        |
|------------------|---------------------|-------------------|--|---------|--|--------------|--|-----|-------------|------------|---------|--------|
|                  | Parameter           | V <sub>CC</sub> * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |         | $T_A = -55^{\circ}C$<br>$to + 125^{\circ}C$<br>$C_L = 50 pF$ |              | $T_{A} = -40^{\circ}C$ $to +85^{\circ}C$ $C_{L} = 50 \text{ pF}$ |     | Fig.<br>No. |            |         |        |
|                  |                     |                   |  |         | Min  | Тур          | Max  | Min | Max         | Min        | Max     | rioeli |
| t <sub>PLH</sub> | Propagation Delay   | 5.0               | 1.0  | 6.5     | 9.0  | 74           |  | 1.0 | 10.0        | ns         | 2-3, 4  |        |
| t <sub>PHL</sub> | Propagation Delay   | 5.0               | 1.0  | 6.0     | 9.0  |              | ron II   | 1.0 | 10.0        | ns         | 2-3, 4  |        |
| t <sub>PZH</sub> | Output Enable Time  | 5.0               | 01.0                                       | 8.0     | 10.0   | as Wi        | (A)  | 1.0 | 11.0        | ns         | 2-5     |        |
| t <sub>PZL</sub> | Output Enable Time  | 5.0               | 1.0  | 8.0     | 12.0   | Тур          |  | 1.0 | 13.0        | ns         | 2-6     |        |
| tpHZ             | Output Disable Time | 5.0               | 1.0  | 0.9.0   | 12.0   | 1,5          | 4.5  | 1.0 | 13.0        | ns         | 2-5     |        |
| t <sub>PLZ</sub> | Output Disable Time | 5.0               | 1.0  | 0.5 8.5 | 11.0   | 8.7          | 8.8  | 1.0 | 12.0        | ns         | 2-6     |        |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V.

| Symbol          | Parameter                        | AC/ACT | Units  | Conditions          |  |  |
|-----------------|----------------------------------|--------|--------|---------------------|--|--|
|                 | rarameter                        | Тур    | Onits  | Conditions          |  |  |
| CIN HOL         | Input Capacitance                | 01.4.5 | g pF a | $V_{\rm CC} = 5.0V$ |  |  |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40.0   | pF o   | $V_{CC} = 5.0V$     |  |  |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>††</sup>May be measured per the JEDEC Alternate Method.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.



# 54AC/74AC373 • 54ACT/74ACT373 Octal Transparent Latch with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable  $(\overline{\text{OE}})$  is LOW. When  $\overline{\text{OE}}$  is HIGH, the bus output is in the high impedance state.

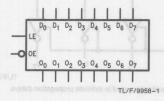
#### **Features**

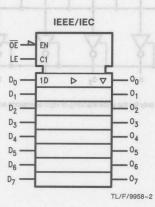
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT373 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC373: 5962-87555

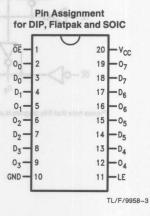
- 'ACT373: 5962-87556

Ordering Code: See Section 8
Logic Symbols

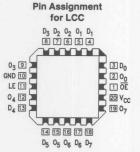
#### **Connection Diagrams**







| Pin Names                      | Description             |
|--------------------------------|-------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs             |
| LE                             | Latch Enable Input      |
| ŌĒ                             | Output Enable Input     |
| 00-07                          | TRI-STATE Latch Outputs |



TL/F/9958-4

#### **Functional Description**

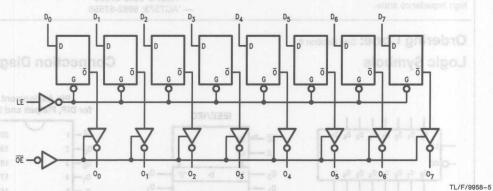
The 'AC/'ACT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the

## Truth Table

|    |        | Outputs  |         |
|----|--------|----------|---------|
| LE | ŌĒ     | Dn       | On      |
| X  | Here   | X        | Z       |
| Н  | E FOR  | waster ! | MARG    |
| Н  | Tribus | TATHET!  | I stoll |
| L  | L      | X        | 00      |

- H = HIGH Voltage Level
  L = LOW Voltage Level
- Z = High Impedance
- X = Immaterial
- O<sub>0</sub> = Previous O<sub>0</sub> before HIGH to Low transition of Latch Enable

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Rating (Note 1) Recommended Operating 1880 00

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )  | -0.5V to $+7.0V$                |
|--|---------------------------------|
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$                                       | -20 mA                          |
| $V_1 = V_{CC} + 0.5V$  | + 20 mA                         |
| DC Input Voltage (V <sub>I</sub> )   | $-0.5$ V to $V_{CC} + 0.5$ V    |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$                                      | -20 mA                          |
| $V_O = V_{CC} + 0.5V$  | + 20 mA                         |
| DC Output Voltage (V <sub>O</sub> )  | $-0.5$ V to to $V_{CC} + 0.5$ V |
| DC Output Source<br>or Sink Current (I <sub>O</sub> )                                      | ± 50 mA                         |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ± 50 mA                         |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Storage Temperature (T<sub>STG</sub>)

Junction Temperature (T<sub>J</sub>)

CDIP

PDIP

# Conditions

| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT   | 2.0V to 6.0V<br>4.5V to 5.5V      |
|--|-----------------------------------|
| Input Voltage (V <sub>I</sub> )  | 0V to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )   | ATELIAT MUMIKE OV to VCC          |
| Operating Temperature (T <sub>A</sub> )<br>74AC/ACT<br>54AC/ACT  | -40°C to +85°C<br>-55°C to +125°C |
| Minimum Input Edge Rate ( $\Delta V$ 'AC Devices $V_{IN}$ from 30% to 70% of $V_{CC}$ @ 3.3V, 4.5V, 5.5V | C 125 mV/ns                       |
|  | /Δt) memuo yaqque                 |
|  |                                   |

#### **DC Characteristics for 'AC Family Devices**

-65°C to +150°C

175°C

140°C

| V1.0                               | = TUOV V                                   | 0.8                    | 74                     | AC OS                | 54AC                         | aar      | 4.5                             | 74AC                 | igh Level    | V <sub>BH</sub> Minimum P<br>Inout Volla   |  |
|------------------------------------|--|------------------------|------------------------|----------------------|------------------------------|----------|---------------------------------|----------------------|--------------|--|--|
| Symbol                             | Parameter                                  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |                      | T <sub>A</sub> = -55°C to +1 | 25°C     | T <sub>A</sub> = -40°C to +85°C |                      | Units        | Conditions   |  |
| V 1.0                              | 33 x 40                                    | G.U.                   | Тур                    | Geo                  | Guaran                       | teed L   | imits                           |                      | 98           | Budy indut   |  |
| VIH HIV 10 JI                      | Minimum High Level<br>Input Voltage        | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75    | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85          | 5,49     | 8.8                             | 2.1<br>3.15<br>3.85  | V            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VILLS-                             | Maximum Low Level<br>Input Voltage         | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75    | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65          | 1001     | 5.5<br>4.5                      | 0.9<br>1.35<br>1.65  | eve. J wo.   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VOH<br>HIV TO JI<br>Am AS<br>Am AS | Minimum High Level Output Voltage          | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49   | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4            | 100.     | 6.A                             | 2.9<br>4.4<br>5.4    | ٧            | $I_{OUT} = -50 \mu\text{A}$  |  |
|                                    | $\mu A  \forall I = V_{CC}$ $V_I = V_{IC}$ | 3.0                    |                        | 2.56<br>3.86         | 2.4<br>3.7                   |          | 8.8                             | 2.40                 | sell tuon    | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ |  |
|                                    | oV = oV Au                                 | 5.5                    |                        | 4.86                 | 4.7                          |          | 5.5                             | 4.76                 | et i V       | −24 mA   |  |
| V <sub>OL</sub> S —                | Maximum Low Level<br>Output Voltage        | 3.0<br>4.5             | 0.002<br>0.001         | 0.1<br>0.1           | 0.1<br>0.1                   | 8.0      | 8.8                             | 0.1                  | ٧            | $I_{OUT} = 50 \mu\text{A}$   |  |
| postvi Vaa. n                      |  | 5.5                    | 0.001                  | 0.1                  | 0.1                          |          | 8.8                             | 0.1                  | Оуматио      | distributed and  |  |
| 3.85V Min                          | MA VOND = VIV = VIV OF END                 | 3.0<br>4.5<br>5.5      |                        | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50         |          |                                 | 0.44<br>0.44<br>0.44 | tner<br>Quic | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $^I_{OL}$ 24 mA 24 mA               |  |
| I <sub>IN</sub>                    | Maximum Input<br>Leakage Current           | 5.5                    |                        | ±0.1                 | ±1.0                         | euna fut | duo rime<br>sind a ta           | ±1.0                 | μΑ           | $V_{I} = V_{CC}$ , GND   |  |

<sup>\*</sup>All outputs loaded, thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) printed mumbers a studyed A

| Symbol Vo.s F |                                     | V <sub>CC</sub> (V) | 74AC                     |           | 54AC                              | 74AC                            | ace spi<br>tha No | Military/Aerosyla  |  |
|---------------|-------------------------------------|---------------------|--------------------------|-----------|-----------------------------------|---------------------------------|-------------------|--|--|
|               | VO.S Parameter                      |                     | T <sub>A</sub> =         | + 25°C    | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units             | Conditions   |  |
|               | /0                                  |                     | Тур                      | sfloV juc | Guaranteed L                      | imits                           | nent (lpd         | DC input Diode Cun   |  |
| lozoV of      | Maximum TRI-STATE® Current          | 5.5                 | lage (Vo<br>Fempen<br>OT | ±0.5      | ±10.0 + 00                        | of Va.c±5.0                     | μА                | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I} = V_{CC}$ , GND<br>$V_{O} = V_{CC}$ , GND |  |
| lold          | †Minimum Dynamic                    | 5.5                 | drill trice              | Longonia  | 50 05-                            | 75                              | mA                | $V_{OLD} = 1.65V Max$  |  |
| IOHD          | Output Current                      | 5.5                 | 200                      | AC Dev    | -50                               | -75                             | mA                | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc           | Maximum Quiescent<br>Supply Current | 5.5                 | 30% A.5%<br>3V, A.5%     | 8.0       | 160.0                             | 80.0                            | μА                | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

#### **DC Characteristics for 'ACT Family Devices**

|                  |                                     |                        | 74/                    | ACT          | 54ACT                            | 74ACT  | ab adT       | to the device may occup   |  |
|------------------|-------------------------------------|------------------------|------------------------|--------------|----------------------------------|--|--------------|---|--|
| Symbol           | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = -55°C to +125°C | and the state of t | Units        | Conditions  |  |
|                  |                                     |                        | Тур                    | 890          | Guaranteed L                     | imits 10 80 1  | eite         | DC Charact  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage |                        | 1.5<br>1.5             | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0   | ٧            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| VIL shell        | Maximum Low Level<br>Input Voltage  | 4.5<br>5.5             | 1.5                    | 0.8          | 0.8                              | 0.8<br>0.8   | V            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| VOH              | Minimum High Level Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4 lave.   | V            | $I_{OUT} = -50 \mu\text{A}$   |  |
|                  | 3.65 V or Voc 3.65 0.8 Vour = 0     | 4.5<br>5.5             |                        | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76   | V            | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$              |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage    | 4.5<br>5.5             | 0.001<br>0.001         | 0.1          | 0.1<br>0.1                       | 0,1<br>0.1   | ٧            | $I_{OUT} = 50 \mu A$  |  |
| Au 08            | 2.9 V 1007 = -                      | 4.5<br>5.5             |                        | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44   | roltage<br>V | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{1}OL$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ |  |
| IIN              | Maximum Input Leakage Current       | 5.5                    |                        | ±0.1         | ±1.0                             | ±1.0   | μΑ           | $V_I = V_{CC}$ , GND  |  |
| loz              | Maximum TRI-STATE®                  | 5.5                    |                        | ±0.5         | ±10.0                            | ± 5.0  | μΑ           | $V_{I} = V_{IL}, V_{IH}$<br>$V_{O} = V_{CC}, GND$                                     |  |
| ICCT             | Maximum I O                         | 5.5                    | 0.6                    | 0,1          | 1.6                              | 0.0 0.0 lave.  | mA           | $V_{\rm I} = V_{\rm CC} - 2.1V$   |  |
| IOLD             | †Minimum Dynamic                    | 5.5                    |                        | 0.1          | 50                               | 75   | mA           | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub> | Output Current                      | 5.5                    |                        | 200          | -50                              | -75  | mA           | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc AS           | Maximum Quiescent Supply Current    | 5.5                    |                        | 8.0          | 160.0                            | 80.0   | μΑ           | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| ٠,٠.             | Ct = 50 pF  | (V)        | (V) $C_L = 50 \text{ pF}$ |             |              | CL =       | 50 pF        | CL =           | 50 pF        | Omis | No.    |
|------------------|---|------------|---------------------------|-------------|--------------|------------|--------------|----------------|--------------|------|--------|
|                  | Min Max   |            | Min                       | Тур         | Max          | Min        | Max          | Min            | Max          |      |        |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.3<br>5.0 | 1.5<br>1.5                | 10.0<br>7.0 | 13.5<br>9.5  | 1.0 a.     | 16.5<br>11.5 | 1.5            | 15.0<br>10.5 | ns   | 2-3, 4 |
| tPHLS            | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.3<br>5.0 | 1.5<br>1.5                | 9.5<br>7.0  | 13.0<br>9.5  | 1.0 o.     | 16.0<br>11.5 | 1.5            | 14.5<br>10.5 | ns   | 2-3, 4 |
| tPLHS            | Propagation Delay<br>LE to O <sub>n</sub>             | 3.3<br>5.0 | 1.5<br>1.5                | 10.0<br>7.5 | 13.5<br>9.5  | 8 1.0 a.   | 16.5<br>12.0 | 1.5 Val<br>1.5 | 15.0<br>10.5 | ns   | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 3.3<br>5.0 | 1.5                       | 9.5<br>7.0  | 12.5<br>9.5  | 1.0 o.     | 15.0<br>11.0 | 1.5<br>1.5     | 14.0<br>10.5 | ns   | 2-3, 4 |
| t <sub>PZH</sub> | Output Enable Time                                    | 3.3<br>5.0 | 1.5                       | 9.0         | 11.5         | 1.0        | 14.0<br>10.5 | 1.0            | 13.0<br>9.5  | ns   | 2-5    |
| t <sub>PZL</sub> | Output Enable Time                                    | 3.3        | 1.5                       | 8.5<br>6.5  | 11.5         | 1.0        | 13.5<br>10.0 | 1.0            | 13.0         | ns   | 2-6    |
| t <sub>PHZ</sub> | Output Disable Time                                   | 3.3<br>5.0 | 1.5<br>1.5                | 10.0<br>8.0 | 12.5<br>11.0 | 1.0<br>1.0 | 16.0<br>13.5 | 1.0            | 14.5<br>12.5 | ns   | 2-5    |
| t <sub>PLZ</sub> | Output Disable Time                                   | 3.3<br>5.0 | 1.5<br>1.5                | 8.0<br>6.5  | 11.5         | 1.0        | 13.0<br>10.5 | 1.0            | 12.5<br>10.0 | ns   | 2-6    |

# \*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V AC Operating Requirements: See Section 2 for Waveforms

|                | muminiss bi                     | V <sub>CC</sub> * | 74           | AC           | 54AC  | 74AC   | Units | Fig.<br>No. |
|----------------|---------------------------------|-------------------|--------------|--------------|---|--|-------|-------------|
| Symbol         | Parameter                       |                   |              | + 25°C 50 pF | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 \text{ pF}$ |       |             |
|                | en 0,1                          |                   | Тур          | 9            | Guaranteed Min  | imum   |       |             |
| ts             | Setup Time, HIGH or LOW         | 3.3<br>5.0        | 3.5<br>2.0   | 5.5          | 6.5<br>5.0  | 6.0  | ns    | 2-7         |
| t <sub>h</sub> | Hold Time, HIGH or LOW Dn to LE | 3.3<br>5.0        | -3.0<br>-1.5 | 1.0          | 1.0   | 1.0  | ns    | 2-7         |
| t <sub>w</sub> | LE Pulse Width,                 | 3.3<br>5.0        | 4.0          | 5.5<br>4.0   | 6.5<br>5.0  | 6.0<br>4.5   | ns    | 2-3         |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

## AC Electrical Characteristics: See Section 2 for Waveforms (1781) 1801 1801 1801 1801

|                  | 74AC   |                   | SAAC                      | 7  | 4ACT |                 |  | AT ! | 4AC  | T  | 74A | CT    |             |        |
|------------------|--|-------------------|---------------------------|--|------|-----------------|--|------|------|--|-----|-------|-------------|--------|
| Symbol           | Parameter of                                       | V <sub>CC</sub> * | 55°C<br>- 125°C<br>- 50 p | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |      | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |      |      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |     | Units | Fig.<br>No. |        |
|                  | xeM niN  | 20                | Min                       | nillä  | Тур  | (eAA            | Max  | Min  | nild | Max  | Min | Max   |             |        |
| t <sub>PLH</sub> | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | 5.0               | 2.5                       | 0.1  | 8.5  | 18.1            | 10.0   | 1.0  | 1.6  | 12.5   | 1.5 | 11.5  | ns          | 2-3, 4 |
| tPHL             | Propagation Delay                                  | 5.0               | 2.0                       | 1.0  | 8.0  | 18.0            | 10.0   | 1.0  | 1.5  | 12.5   | 1.5 | 11.5  | ns          | 2-3, 4 |
| tPLH             | Propagation Delay<br>LE to On                      | 5.0               | 2.5                       | 0.7  | 8.5  | 1.61            | 11.0   | 1.0  | 1.6  | 12.5   | 2.0 | 11.5  | ns          | 2-3, 4 |
| tPHL             | Propagation Delay                                  | 5.0               | 2.0                       | 1.0  | 8.0  | 12.1            | 10.0   | 1.0  | 1.5  | 11.5   | 1.5 | 11.5  | ns          | 2-3, 4 |
| t <sub>PZH</sub> | Output Enable Time                                 | 5.0               | 2.0                       | 0,1  | 8.0  | 111             | 9.5  | 1.0  | 8.1  | 11.5   | 1.5 | 10.5  | ns          | 2-5    |
| tpzL             | Output Enable Time                                 | 5.0               | 2.0                       | 0.1  | 7.5  | 8.8             | 9.0  | 1.0  | 1.6  | 11.0   | 1.5 | 10.5  | ns          | 2-6    |
| t <sub>PHZ</sub> | Output Disable Time                                | 5.0               | 2.5                       | 0.1  | 9.0  | 11.             | 11.0   | 1.0  | 1.5  | 14.0   | 2.5 | 12.5  | ns          | 2-5    |
| t <sub>PLZ</sub> | Output Disable Time                                | 5.0               | 1.5                       | Will   | 7.5  | 0.6             | 8.5  | 1.0  | 0.1  | 11.0   | 1.0 | 10.0  | ns          | 2-6    |

#### 

| Symbol         |  |                          | 74  | ACT               | 54ACT   | 74ACT  | Units | Fig.<br>No. |
|----------------|--|--------------------------|-----|-------------------|---|--|-------|-------------|
|                | Parameter                                      | V <sub>CC</sub> *<br>(V) |     | + 25°C<br>= 50 pF | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |       |             |
|                | ZAAC   | BAAG                     | Тур | 7640              | Guaranteed Min  | imum   |       |             |
| t <sub>s</sub> | Setup Time, HIGH or LOW                        | 5.0                      | 3.0 | 7.0               | 8.5   | 8.0  | ns    | 2-7         |
| th             | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0                      | 0   | 0                 | 1.0   | 1.0  | ns    | 2-7         |
| tw             | LE Pulse Width, HIGH                           | 5.0                      | 2.0 | 7.0               | 8.5 WO  | 8.0  | ns    | 2-3         |

\*Voltage Range 5.0 is 5.0V ±0.5V

| Symbol          | Parameter as                     | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40.0 | pF    | V <sub>CC</sub> = 5.0V |



# 54AC/74AC374 • 54ACT/74ACT374 Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable  $(\overline{\text{OE}})$  are common to all flip-flops.

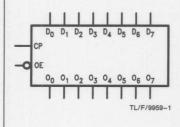
#### **Features**

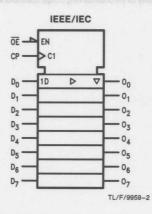
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- See '273 for reset version
- See '377 for clock enable version
- See '373 for transparent latch version
- See '574 for broadside pinout version
- See '564 for broadside pinout version with inverted outputs
- 'ACT374 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  - 'AC374: 5962-87694
  - 'ACT374: 5962-87631

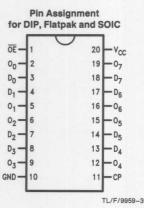
Ordering Code: See Section 8

#### **Logic Symbols**

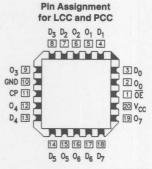
#### **Connection Diagrams**







| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| CP                             | Clock Pulse Input             |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Outputs             |



TL/F/9959-4

#### **Functional Description**

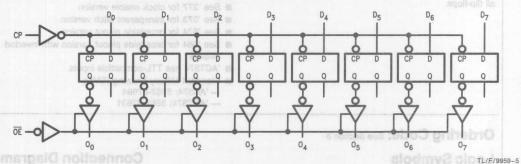
The 'AC/'ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable  $(\overline{OE})$  LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

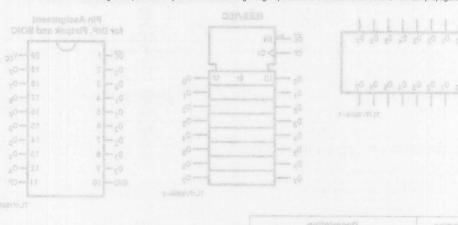
|          |                                 | Inputs | regina e.gra<br>bannai osa | Outputs |
|----------|---------------------------------|--------|----------------------------|---------|
| [        | O <sub>n</sub>                  | СР     | ŌĒ                         | On      |
| the same | H <sub>1</sub> / <sub>1</sub> 1 | 3 /kes | MARCH                      | OAH2    |
| 2 4 8 4  | Farm's                          | 1      | soma Far a                 | most    |
| - 197    | X                               | X      | -aiH (                     | Z       |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance
- ✓ = LOW-to-HIGH Transition

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



 Pin Manies
 Description

 On-Dr
 Data Inputs

 CP
 Chock Pulse Input

 CE
 TRI-STATE Output Enable Input

 On-Or
 TRI-STATE Outputs

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

 $\begin{array}{lll} \text{Supply Voltage (V$_{CC}$)} & -0.5 \text{V to } +7.0 \text{V} \\ \text{DC Input Diode Current (I$_{IK}$)} & & & & & \\ V_I = -0.5 \text{V} & & & & & \\ V_I = \text{V}_{CC} + 0.5 \text{V} & & & & \\ \end{array}$ 

DC Input Voltage (V<sub>I</sub>)  $-0.5 \text{V to V}_{CC} + 0.5 \text{V}$  DC Output Diode Current (I<sub>OK</sub>)  $V_O = -0.5 \text{V}$  -20 mA  $V_O = V_{CC} + 0.5 \text{V}$  +20 mA

DC Output Voltage ( $V_O$ ) -0.5V to to  $V_{CC} + 0.5V$ DC Output Source or Sink Current ( $I_O$ )  $\pm 50$  mA

 DC V<sub>CC</sub> or Ground Current
 ±50 mA

 Storage Temperature (T<sub>STG</sub>)
 -65°C to +150°C

Storage Temperature (T<sub>STG</sub>) -69

Junction Temperature (T<sub>J</sub>)

CDIP

PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 'AC
 2.0V to 6.0V

 'ACT
 4.5V to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

 Output Voltage (V<sub>O</sub>)
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 74AC/ACT

 74AC/ACT
 -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)
'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices
V<sub>IN</sub> from 0.8V to 2.0V
V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

125 mV/ns

## DC Characteristics for 'AC Family Devices

|  | - 00V 10                             | 0.5                 | 74                            | AC                   | 54AC                                     | 74AC                          | ega             |  |
|--|--------------------------------------|---------------------|-------------------------------|----------------------|--|-------------------------------|-----------------|--|
| Symbol                                   | ymbol Parameter                      |                     | $V_{CC}$ $T_A = +25^{\circ}C$ |                      | T <sub>A</sub> = 00<br>0-55°C to + 125°C | T <sub>A</sub> = -40°C to +85 | °C Units        | Conditions   |
|  | = Tuol v                             | 4,4                 | Тур                           | 4                    | Guaranteed L                             | imits d.a                     | High Level      |  |
| V <sub>IH</sub><br>H <sub>I</sub> V to J | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75           | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85                      | 2.1<br>3.15<br>3.85           | V               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub> as -                     | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75           | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65                      | 0.9<br>1.35<br>1.65           | Low Level       | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| VoH no a<br>Am AS<br>Am AS               | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49          | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                        | 2.9<br>4.4<br>5.4             | V               | $I_{OUT} = -50 \mu\text{A}$  |
|  | V = V                                | 3.0 ±<br>4.5<br>5.5 |                               | 2.56<br>3.86<br>4.86 | 2.4 0 ±<br>3.7<br>4.7                    | 2.46<br>3.76<br>4.76          | Input<br>Darynt | $^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $-12 \text{ mA}$ $I_{\text{OH}}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |
| Vol                                      | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001       | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                        | 0.1<br>0.1<br>0.1             | V               | I <sub>OUT</sub> = 50 μA   |
| xaM Vd9.<br>nlM Vd9.s                    | mA Volo =                            | 3.0<br>4.5<br>5.5   |                               | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50                     | 0.44<br>0.44<br>0.44          | Dynamic<br>mcV  | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}\text{OL}$ $^{24} \text{ mA}$ $^{24} \text{ mA}$                |
| IIN                                      | Maximum Input<br>Leakage Current     | 5.5                 |                               | ±0.1                 | ±1.0                                     | ±1.0                          | μА              | $V_I = V_{CC}$ , GND   |

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) This is a summing the stude of A

|                       |                                     |                        | 74                       | AC        | 54AC                              | 74AC                            | ece spa | H Military/Aerosp  |
|-----------------------|-------------------------------------|------------------------|--------------------------|-----------|-----------------------------------|---------------------------------|---------|--|
| Symbol VO.8 Parameter |                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C   |           | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units   | Conditions   |
|                       |                                     |                        | Typ Guaranteed Limits    |           |                                   |                                 |         | DC Input Diode Cu  |
| loz <sup>OV</sup>     | Maximum TRI-STATE® Current          | 5.5                    | age (Vo<br>Tempera<br>ST | ±0.5      | ± 10.0                            | otva. ±5.0                      | μА      | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND |
| IOLD                  | †Minimum Dynamic                    | 5.5                    | of the same              | I courois | 50 05 -                           | 75                              | mA      | V <sub>OLD</sub> = 1.65V Max   |
| IOHD                  | Output Current                      | 5.5                    | 880                      | VeO DA    | -50                               | -75                             | mA      | V <sub>OHD</sub> = 3.85V Min   |
| I <sub>CC</sub>       | Maximum Quiescent<br>Supply Current | 5.5                    | SV, 4.5V                 | 8.0       | 160.0                             | 80.0                            | μА      | V <sub>IN</sub> = V <sub>CC</sub><br>or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

#### **DC Characteristics for 'ACT Family Devices**

|                  |                                      |                        | 74/              | ACT          | 54ACT                             | 74ACT                           | poset real          | Note it Absolute medic  |  |
|------------------|--------------------------------------|------------------------|------------------|--------------|-----------------------------------|---------------------------------|---------------------|---|--|
| Symbol           | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units               | Conditions  |  |
|                  |                                      |                        | Тур              |              | Guaranteed Li                     | mits                            |                     |   |  |
| V <sub>IH</sub>  | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   | 2.0<br>2.0                        | 2.0<br>2.0                      | ٧                   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5              | 0.8          | 0.8                               | 0.8<br>0.8                      | na Varia            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| VoH              | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧                   | $I_{OUT} = -50 \mu\text{A}$   |  |
|                  | = 00 V 00 V                          | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | V                   | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | V                   | $I_{OUT} = 50 \mu A$  |  |
|                  | Tuol V                               | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | al rigits<br>epstic | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| IN ST            | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | ±1.0                              | ± 1.0                           | μА                  | $V_{I} = V_{CC}$ , GND  |  |
| loz Au o         | Maximum TRI-STATE® Current           | 5.5                    |                  | ±0.5         | ±10.0                             | ±5.0                            | μА                  | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| ICCT             | Maximum I <sub>CC</sub> /Input       | 5.5                    | 0.6              | 1.           | 1.6                               | 1.5                             | mA                  | $V_{\rm I} = V_{\rm CC} - 2.1V$   |  |
| IOLD             | †Minimum Dynamic                     | 5.5                    |                  | - 0.0        | 50                                | 75                              | mA                  | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub> | Output Current                       | 5.5                    |                  | 68           | -50                               | -75                             | mA                  | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc              | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 160.0                             | 80.0                            | μА                  | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

### AC Electrical Characteristics: See Section 2 for waveforms

|                  | TARCT                         | 1          | TO,A       | 74AC   |              | TO A 5     | 4AC   | 74         | AC                     |       | 1348        |
|------------------|-------------------------------|------------|------------|--|--------------|------------|---|------------|------------------------|-------|-------------|
| Symbol           | Symbol Parameter              |            |            | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              |            | $T_{A} = -55^{\circ}C$<br>to + 125°C<br>$C_{L} = 50 \text{ pF}$ |            | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                  | xaM n                         | 95 ] 1     | Min        | Тур  | Max          | Min        | Max   | Min        | Max                    |       |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency    | 3.3<br>5.0 | 60<br>100  | 110<br>155                                       |              | 60<br>95   | 0 100   | 60<br>100  | mum Olack<br>Jency     | MHz   | xहाती       |
| tPLH             | Propagation Delay<br>CP to On | 3.3<br>5.0 | 3.0<br>2.5 | 11.0<br>8.0                                      | 13.5<br>9.5  | 1.0<br>1.0 | 16.5<br>12.0  | 1.5<br>1.5 | 15.5<br>10.5           | ns    | 2-3, 4      |
| tPHL             | Propagation Delay<br>CP to On | 3.3<br>5.0 | 2.5        | 10.0<br>7.0                                      | 12.5         | 1.0<br>1.0 | 15.0<br>11.0  | 2.0<br>1.5 | 14.0<br>10.0           | ns    | 2-3, 4      |
| tpzH             | Output Enable Time            | 3.3<br>5.0 | 3.0        | 9.5<br>7.0                                       | 11.5<br>8.5  | 1.0        | 14.0<br>10.5  | 1.5<br>1.0 | 13.0<br>9.5            | ns    | 2-5         |
| t <sub>PZL</sub> | Output Enable Time            | 3.3<br>5.0 | 2.5        | 9.0<br>6.5                                       | 11.5<br>8.5  | 1.0<br>1.0 | 14.0<br>10.5  | 1.5<br>1.0 | 13.0<br>9.5            | ns    | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time           | 3.3<br>5.0 | 3.0<br>2.0 | 10.5<br>8.0                                      | 12.5<br>11.0 | 1.0<br>1.0 | 16.0<br>12.5  | 2.0<br>2.0 | 14.5<br>12.5           | ns    | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time           | 3.3<br>5.0 | 2.0        | 8.0<br>6.5                                       | 11.5<br>8.5  | 1.0        | 13.0<br>10.5  | 1.0        | 12.5<br>10.0           | ns    | 2-6         |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

#### AC Operating Requirements: See Section 2 for waveforms

|                | d Minimum                                       |            | $V_{CC}^*$ $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |                | 54AC  | 74AC   |       | Fig.<br>No. |
|----------------|---|------------|---|----------------|---|--|-------|-------------|
| Symbol         | Parameter                                       |            |   |                | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units |             |
| 1.5 ns 2-7     | 1.5   | Тур        |   | Guaranteed Min | imum 90 c   |  |       |             |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 3.3<br>5.0 | 2.0   | 5.5<br>4.0     | 6.5<br>5.0  | 6.0<br>4.5   | ns    | 2-7         |
| t <sub>h</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 3.3<br>5.0 | -1.0<br>0   | 1.0<br>1.5     | 1.0<br>1.5  | 1.0<br>1.5   | ns    | 2-7         |
| t <sub>w</sub> | CP Pulse Width,<br>HIGH or LOW                  | 3.3<br>5.0 | 4.0<br>2.5  | 5.5<br>4.0     | 6.5<br>5.0  | 6.0<br>4.5   | ns    | 2-3         |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

| ck      | 3   | Min      | Тур          | Maria            |                      |                          | to +85°C<br>C <sub>L</sub> = 50 pF |                                   | 4                                      | No.                                       |
|---------|-----|----------|--------------|------------------|----------------------|--------------------------|------------------------------------|-----------------------------------|--|---|
| ck      |     | 1        | 11           | Max              | Min                  | Max                      | Min                                | Max                               |  |   |
| VVI     | 5.0 | 100      | 160          |                  | 70                   | 3 60<br>0 100            | 90                                 | nom Clack<br>sency                | MHz                                    | tmax                                      |
| Delay 8 | 5.0 | 2.0      | 8.5          | 10.0             | 1.0                  | 12.0                     | 2.0                                | 11.5                              | ns                                     | 2-3, 4                                    |
| Delay 0 | 5.0 | 2.0      | 8.0          | 9.5              | 1.0                  | 11.5                     | 1.5                                | 11.0                              | ns                                     | 2-3, 4                                    |
| e Time  | 5.0 | 2.0      | 8.0          | 9.5              | 1.0                  | 11.5                     | 1.5                                | 10.5                              | ns                                     | 2-5                                       |
| e Time  | 5.0 | 1.5      | 8.0          | 9.0              | 1.0                  | 11.5                     | 1.5                                | 10.5                              | ns                                     | 2-6                                       |
| e Time  | 5.0 | 1.5      | 8.5          | 11.5             | 1.0                  | 13.0                     | 1.0                                | 12.5                              | ns                                     | 2-5                                       |
| e Time  | 5.0 | 1.5      | 7.0          | 8.5              | 1.0                  | 11.0                     | 1.0                                | 10.0                              | ns                                     | 2-6                                       |
| е       | 0.  | Time 5.0 | Time 5.0 1.5 | Time 5.0 1.5 7.0 | Time 5.0 1.5 7.0 8.5 | Time 5.0 1.5 7.0 8.5 1.0 | Time 5.0 1.5 7.0 8.5 1.0 11.0      | Time 5.0 1.5 7.0 8.5 1.0 11.0 1.0 | Time 5.0 1.5 7.0 8.5 1.0 11.0 1.0 10.0 | Time 5.0 1.5 7.0 8.5 1.0 11.0 1.0 10.0 ns |

#### 

|                  | 1 0.01 0.1                                     | 10,01   | 74  | ACT   | 54ACT  | 74ACT | A Range 3.9 | Voltage |
|------------------|--|---|-----|---|--|-------|-------------|---------|
| Symbol Parameter |  | $V_{CC}^*$ $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |     | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units | Fig.<br>No. |         |
|                  | YAAC   | DAVE  | Тур | 442   | Guaranteed Min   | imum  |             |         |
| t <sub>s</sub>   | Setup Time, HIGH or LOW                        | 5.0   | 1.0 | 5.0   | 8.5  | 5.5   | ns          | 2-7     |
| t <sub>h</sub>   | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0   | 0   | 1.5   | 1.5  | 1.5   | ns          | 2-7     |
| T-Sw             | CP Pulse Width,<br>HIGH or LOW                 | 5.0   | 2.5 | 5.0   | 8.6<br>8.5 WO  | 5.0   | ns          | 2-3     |

\*Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

| Symbol          | Parameter 0.3                    | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 80.0 | pF    | V <sub>CC</sub> = 5.0V |

### 54AC/74AC377 ● 54ACT/74ACT377 Octal D Flip-Flop with Clock Enable

#### **General Description**

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ( $\overline{\text{CE}}$ ) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The  $\overline{\text{CE}}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

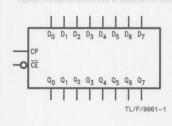
#### **Features**

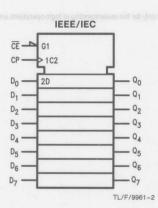
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs
- Standard Military Drawing (SMD)
- 'AC377: 5962-88702
- 'ACT377: 5962-87697

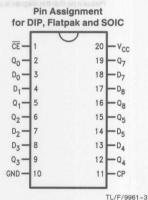
Ordering Code: See Section 8

#### **Logic Symbols**

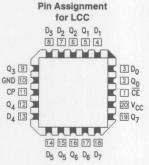
### **Connection Diagrams**







| Pin Names                      | Description               |
|--------------------------------|---------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs               |
| CE                             | Clock Enable (Active LOW) |
| Q <sub>0</sub> -Q <sub>7</sub> | Data Outputs              |
| CP                             | Clock Pulse Input         |



TL/F/9961-4

4

#### Mode Select-Function Table

| Operating Mode    |    | Inputs |    | Outputs   |
|-------------------|----|--------|----|-----------|
| Operating mode    | СР | CE     | Dn | Qn        |
| Load '1'          | _  | L      | Н  | Н         |
| Load '0'          | _  | L      | L  | 1 JEAN    |
| Hold (Do Nothing) | _  | Н      | X  | No Change |
| Hold (Do Nothing) | X  | Н      | X  | No Change |

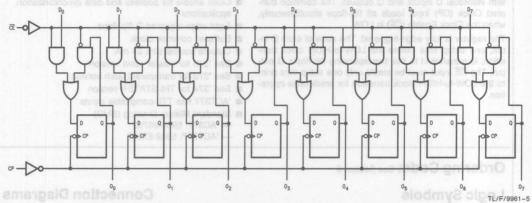
H = HIGH Voltage Level

L = LOW Voltage Level
X = Immaterial

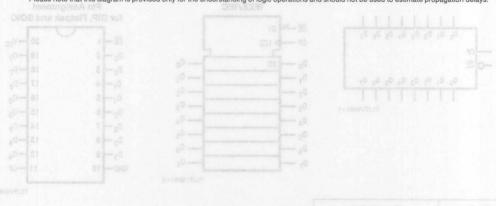
\_\_ = LOW-to-HIGH Clock Transition

#### **Logic Diagram**

E EDO



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



Pin Names Description

Do-D7 Data Inputs

CE Clock Enable (Active LOW)

Og-C7 Data Outputs

CP Clock Pulse Input

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for availab  | mility and spe | cilications.             |
|--|----------------|--------------------------|
| Supply Voltage (V <sub>CC</sub> )  | 0 48*0 10 +88  | 0.5V to +7.0V            |
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$<br>$V_I = V_{CC} + 0.5V$              |                | -20 mA<br>+20 mA         |
| DC Input Voltage (V <sub>I</sub> )   | -0.5V to       | 0 V <sub>CC</sub> + 0.5V |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$             |                | -20 mA<br>+20 mA         |
| DC Output Voltage (V <sub>O</sub> )  | -0.5V to to    | 0 V <sub>CC</sub> + 0.5V |
| DC Output Source or Sink Current (I <sub>O</sub> )   |                | ±50 mA                   |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) |                | ±50 mA                   |
| Storage Temperature (T <sub>STG</sub> )  | -65            | °C to +150°C             |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

Junction Temperature (T<sub>J</sub>)

CDIP PDIP

#### Absolute Maximum Rating (Note 1) Recommended Operating and OO Conditions

| -  |  |                      |                        |                              |
|----|--|----------------------|------------------------|------------------------------|
| S  | Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT                                 |                      |                        | 2.0V to 6.0V<br>4.5V to 5.5V |
| II | nput Voltage (V <sub>I</sub> )   |                      |                        | 0V to V <sub>CC</sub>        |
| (  | Output Voltage (V <sub>O</sub> )   |                      |                        | 0V to V <sub>CC</sub>        |
| C  | perating Temperature 74AC/ACT 54AC/ACT                                     | re (T <sub>A</sub> ) | memiO fue<br>-40       |                              |
| ٨  | ninimum Input Edge   | Rate (A              | V/Δt) memo ylq         |                              |
|    | 'AC Devices V <sub>IN</sub> from 30% to 70 V <sub>CC</sub> @ 3.3V, 4.5V, 5 |                      | CC AME DE MODERNA      | 125 mV/ns                    |
| ٨  | Ainimum Input Edge I<br>'ACT Devices<br>VIN from 0.8V to 2.                | 01/                  | ΔV/Δt)                 |                              |
|    | V <sub>CC</sub> @ 4.5V, 5.5V   |                      |                        | 125 mV/ns                    |
| N  | ete 2. Con individual data   | schoots f            | or those devices which | h differ from the            |

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

### **DC Characteristics for 'AC Family Devices**

|                          | = mol "                              | K                      | 74                      | AC                   |               | 54AC                 |          | 74AC                            | e High Le |   |
|--------------------------|--------------------------------------|------------------------|-------------------------|----------------------|---------------|----------------------|----------|---------------------------------|-----------|---|
| Symbol                   | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | -55           | T <sub>A</sub> =     | 125°C    | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions  |
|                          | $\Lambda = NI_{\Lambda_x}$           | 26                     | Тур                     |                      | 3.70          | Guara                | nteed L  | imits                           |           |   |
| V <sub>IH</sub> PS —     | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 0.70          | 2.1<br>3.15<br>3.85  | 4.86     | 2.1<br>3.15<br>3.85             | V I WOLIN | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                                    |
| V <sub>IL</sub><br>Am as | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.50          | 0.9<br>1.35<br>1.65  | 85.0     | 0.9<br>1.35<br>1.65             | V         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| VOH                      | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 0.10<br>± 1.0 | 2.9<br>4.4<br>5.4    | ±0.1     | 2.9<br>4.4<br>5.4               | Sugn) a   | $I_{OUT} = -50 \mu\text{A}$   |
|                          | mA. Vi = Voc                         | 3.0                    |                         | 2.56                 | 8.3           | 2.4                  |          | 2.46                            | 11        | $*V_{IN} = V_{IL} \text{ or } V_{IH}$<br>-12 mA   |
| xsM V88.                 | t = quoV Am                          | 4.5<br>5.5             |                         | 3.86<br>4.86         | 50            | 3.7<br>4.7           |          | 3.76<br>4.76                    | man Vam   | l <sub>OH</sub> −24 mA<br>−24 mA  |
| V <sub>OL</sub>          | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 160.0         | 0.1<br>0.1<br>0.1    |          | 0.1<br>0.1<br>0.1               |           | $I_{OUT} = 50 \mu\text{A}$  |
|                          |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 |               | 0.50<br>0.50<br>0.50 | tobnu tu | 0.44<br>0.44<br>0.44            |           | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA I <sub>OL</sub> 24 mA 24 mA |
| I <sub>IN</sub>          | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 |               | ± 1.0                |          | ±1.0                            | μΑ        | $V_I = V_{CC}$ , GND  |

175°C

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) The American American

|         |                                     |                        | 7                | 4AC         | 54AC                              | 74AC         | eça aşa<br>eli eri | If Military/Aerosp           |
|---------|-------------------------------------|------------------------|------------------|-------------|-----------------------------------|--------------|--------------------|------------------------------|
| Symbol  | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C      | T <sub>A</sub> = -55°C to + 125°C | - In         | Units              | Conditions                   |
| ooV et  | (0                                  |                        | Тур              | egatioV ha  | Guaranteed Li                     | mits         | (lip)              | DC Input Diode Cur           |
| lold    | †Minimum Dynamic                    | 5.5                    | (0X) at          | alio V tugt | 50                                | 75           | mA                 | V <sub>OLD</sub> = 1.65V Max |
| IOHD    | Output Current                      | 5.5                    | mperatu          | BESTEEN TE  | -50 0 + 00                        | / of V3.0-75 | mA (               | V <sub>OHD</sub> = 3.85V Min |
| Icc 482 | Maximum Quiescent<br>Supply Current | 5.5                    | n Edge           | 8.0         | 160.0 08-                         | 80.0         | μΑ                 | $V_{IN} = V_{CC}$ or GND     |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.
I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### **DC Characteristics for 'ACT Family Devices**

|                       |                                      |                        |                  |              |              |                  | Met - on                        |                                 | Comp. D. a. | Slorada Tampardiu  |
|-----------------------|--------------------------------------|------------------------|------------------|--------------|--------------|------------------|---------------------------------|---------------------------------|-------------|--|
| edt mott              | or tirose devices which diffe        | elseriani              | 744              | CT           | 606/6        | 54ACT            |                                 | 74ACT                           | (j,T) en    | Junction Temperate   |
| Symbol                | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | -55°         | T <sub>A</sub> = | 125°C                           | T <sub>A</sub> = -40°C to +85°C | Units       | Conditions   |
|                       |                                      |                        | Тур              |              |              | Guara            | nteed L                         | imits to another body at        | pdatab erit | to the device may occur.   |
| V <sub>IH</sub>       | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   |              | 2.0              | now sup<br>to not rec<br>tiens. | 2.0 sans p                      | 1/          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>       | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 800          | 0.8              | ylim                            | 0.8                             | V           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub>       | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | = AT         | 4.4<br>5.4       | 25°C                            | 4.4<br>5.4                      | V           | $I_{OUT} = -50 \mu\text{A}$  |
| VI.0                  | = ruoV                               | 4.5<br>5.5             | edion            | 3.86<br>4.86 | Guara<br>2.1 | 3.70<br>4.70     | r.s.                            | 3.76<br>4.76                    | ve J ngiH   | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$         |
| V <sub>OL</sub>       | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001            | 0.1<br>0.1   | 3.15         | 0.1<br>0.1       | 3,15                            | 0.1<br>0.1                      | V OQS       | I <sub>OUT</sub> = 50 μA   |
| 0.1V<br>- 0.1V        |                                      | 4.5<br>5.5             |                  | 0.36<br>0.36 | 1.35         | 0.50<br>0.50     | 1.95                            | 0.44<br>0.44                    | egs<br>V    | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$ |
| IIN                   | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | 4.4<br>5.4   | ±1.0             | 4,4<br>5,4                      | 95.5 ± 1.0 5<br>98.8 ± 1.0 5    | μА          | V <sub>I</sub> = V <sub>CC</sub> , GND   |
| ICCTIO_I/V<br>Am St — | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |              | 2,4          | 1.6              | 2.56                            | 1.5                             | mA          | $V_I = V_{CC} - 2.1V$  |
| I <sub>OLD</sub>      | †Minimum Dynamic                     | 5.5                    |                  |              | 3.7          | 50               | 3.86                            | 75                              | mA          | V <sub>OLD</sub> = 1.65V Max   |
| IOHD                  | Output Current                       | 5.5                    |                  |              | + 0          | -50              | N. (5)                          | -75                             | mA          | V <sub>OHD</sub> = 3.85V Min   |
| loc                   | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 1.0          | 160.0            | 1.0                             | 100.0 80.0                      | μА          | V <sub>IN</sub> = V <sub>CC</sub><br>or GND                                    |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms and an add a section 2 for Waveforms

|                  | PARCT                                     |                   | TOAR                           | 74AC                                       | Y    | DANT 5   | 4AC                           | 74         | AC                      |       |             |
|------------------|---|-------------------|--------------------------------|--|------|----------|-------------------------------|------------|-------------------------|-------|-------------|
| Symbol           | Parameter                                 | V <sub>CC</sub> * | = - 55°C<br>- 125°C<br>= 50 pP | T <sub>A</sub> = +2<br>C <sub>L</sub> = 50 |      | to-      | = −55°C<br>+ 125°C<br>= 50 pF | to +       | -40°C<br>-85°C<br>50 pF | Units | Fig.<br>No. |
|                  | n Max                                     |                   | Min                            | Тур  | Max  | Min      | Max                           | Min        | Max                     |       |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency                | 3.3<br>5.0        | 90<br>140                      | 125<br>175                                 |      | 75<br>95 | 140                           | 75<br>125  | muim Clack<br>vency     | MHz   | xemî        |
| t <sub>PLH</sub> | Propagation Delay<br>CP to Q <sub>n</sub> | 3.3<br>5.0        | 3.0                            | 8.0<br>6.0                                 | 13.0 | 1.0      | 14.0<br>10.0                  | 1.5<br>1.5 | 14.0                    | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>CP to Q <sub>n</sub> | 3.3<br>5.0        | 3.5<br>2.5                     | 8.5<br>6.5                                 | 13.0 | 1.0      | 15.0<br>11.0                  | 2.0        | 14.5<br>11.0            | ns    | 2-3, 4      |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

# AC Operating Requirements: See Section 2 for Waveforms

|        |        |                             |                     | 10000         | 74/          | AC         | 54AC   | 74AC   |       |      |
|--------|--------|-----------------------------|---------------------|---------------|--------------|------------|--|--|-------|------|
| Symbol | ilnU   | Parameter                   | 88°C<br>8°C<br>1 pF | 200           | TA =<br>CL = |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|        |        |                             | niss be             | einstenS      | Тур          | dás        | Guaranteed Min   | imum   |       |      |
| ts     | 1      | up Time, HIGH or l<br>to CP | LOW                 | 3.3<br>5.0    | 3.5<br>2.5   | 5.5<br>4.0 | 7.5<br>6.0   | 6.0<br>4.5   | ns ns | 2-7  |
| thS    | 1000   | d Time, HIGH or Lo<br>to CP | OW                  | 5.0           | -2.0<br>-1.0 | 1.0        | 0.01.5<br>2.5  | 0 90 0   | no ns | 2-7  |
| ts     |        | up Time, HIGH or I<br>to CP | LOW                 | 0.73.3<br>5.0 | 4.0<br>2.5   | 6.0<br>4.0 | 9.5<br>6.0   | 7.5<br>4.5   | 30 ns | 2-7  |
| thS    |        | d Time, HIGH or LO<br>to CP | WC                  | 3.3<br>5.0    | -3.5<br>-2.0 | 1.0        | 1.0<br>2.0   | 0<br>1.0   | ns    | 2-7  |
| tw     | 17.000 | Pulse Width<br>iH or LOW    |                     | 3.3<br>5.0    | 3.5<br>2.5   | 5.5<br>4.0 | 6.5<br>5.0   | 6.0<br>4.5   | ns ns | 2-3  |

\*Voltage Range 3.3 is 3.0V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

| Voc = 5.0V |  |  |
|------------|--|--|

| Symbol           | Parameter + of                | V <sub>CC</sub> * | 126°C<br>= 80 pF | T <sub>A</sub> = +2<br>C <sub>L</sub> = 50 |          | U   | - 55°C<br>- 125°C<br>= 50 pF | to + | -40°C<br>-85°C<br>50 pF | Units | Fig.<br>No. |
|------------------|-------------------------------|-------------------|------------------|--|----------|-----|------------------------------|------|-------------------------|-------|-------------|
|                  | n Max                         | N                 | Min              | Тур  | Max      | Min | Max                          | Min  | Max                     |       |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency    | 5.0               | 140              | av<br>ag 175                               |          | 85  | 90                           | 125  | mum Cladk<br>uendy      | MHz   | xami        |
| t <sub>PLH</sub> | Propagation Delay<br>CP to Qn | 5.0               | 3.0              | 6.5  | 0.8      | 0.8 | 0.8<br>0.5<br>11.0           | 2.5  | 10.0                    | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay             | 5.0               | 3.5              | 7.0  | 0.0 10.0 | 3.8 | 12.0                         | 2.5  | 11.0                    | ns    | 2-3, 4      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$  0.5V

#### AC Operating Requirements: See Section 2 for Waveforms

|                | 7680  |      | IAA3               | 74A                               | CT  | 54AC   | Г     | 74ACT  |       |      |
|----------------|---|------|--------------------|-----------------------------------|-----|--|-------|--|-------|------|
| Symbol         | Parameter                                   | 85°C | V <sub>CC</sub> *  | T <sub>A</sub> = C <sub>L</sub> = |     | T <sub>A</sub> = -5<br>to + 125<br>C <sub>L</sub> = 50 | 5°C   | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|                | CL = 50 pF                                  | 191  | O <sub>L</sub> = 8 | Тур                               |     | Guarantee  | d Min | imum   |       |      |
| t <sub>s</sub> | Setup Time, HIGH or<br>D <sub>n</sub> to CP | LOW  | 5.0                | 2.5                               | 4.5 | 8 8 7.0  | WO.   | 10 HOI5.5mill qu   | es ns | 2-7  |
| t <sub>h</sub> | Hold Time, HIGH or Dn to CP                 | LOW  | 5.0                | -1,0                              | 1.0 | 8.81.0   | WC    | U to HE1.0, amil' to   | oH ns | 2-7  |
| t <sub>s</sub> | Setup Time, HIGH or CE to CP                | LOW  | 6.0                | 2.5                               | 4.5 | €.87.0   | WO.   | 10 HD 5.5  | ns ns | 2-7  |
| t <sub>h</sub> | Hold Time, HIGH or                          | LOW  | 0.15.0             | -1.0                              | 1.0 | 8,81.0   | WC    | J to Hall.0,emiT b   | oH ns | 2-7  |
| t <sub>w</sub> | CP Pulse Width<br>HIGH or LOW               |      | 5.0                | 2.0                               | 4.0 | 5.5  |       | (4.5) selu9  | 90 ns | 2-3  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 90.0 | pF    | V <sub>CC</sub> = 5.0V |



# 54AC/74AC378 Parallel D Register with Enable

#### **General Description**

The 'AC378 is a 6-bit register with a buffered common Enable. This device is similar to the 'AC174, but with common Enable rather than common Master Reset.

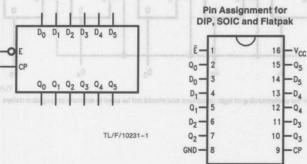
#### **Features**

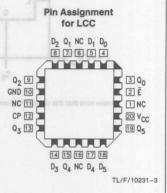
- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects

Ordering Code: See Section 8

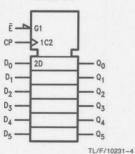
**Logic Symbols** 

#### **Connection Diagrams**





IEEE/IEC



TL/F/10231-2

| Pin Names                      | Description                            |
|--------------------------------|--|
| Ē                              | Enable Input (Active LOW)              |
| D <sub>0</sub> -D <sub>5</sub> | Data Inputs                            |
| CP                             | Clock Pulse Input (Active Rising Edge) |
| Q <sub>0</sub> -Q <sub>5</sub> | Outputs                                |

#### **Functional Description**

The 'AC378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q inputs. The Clock (CP) and Enable (E) inputs are common to all flip-flops.

When the E input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the E input is HIGH the register will retain the present data independent of the CP input.

## Truth Table

|          | Inputs | shnonis | Output    |  |  |
|----------|--------|---------|-----------|--|--|
| Ē        | СР     | Dn      | Qn        |  |  |
| Н        | 100    | X       | No Change |  |  |
| L        | 1      | Н       | Н         |  |  |
| a residu | 1      | SAC     | Paralle   |  |  |

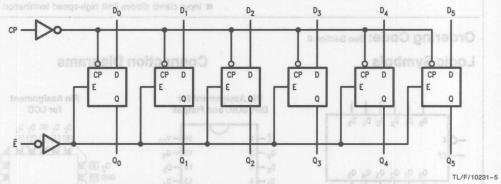
H = HIGH Voltage Level

L = LOW Voltage Level

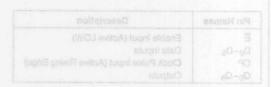
= LOW-to-HIGH Clock Transition

#### M Positive adge-briggered D-type inputs Logic Diagram

ULA A MAL



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



| - 1 | 107 | ٦ |
|-----|-----|---|
| -1  | Λ   | 1 |
| -1  | ш   | í |
|     |     |   |

| DO 1 - 1 D' - 1 - 0 1 (1 )   |  | 701   |                       |                       |                                    | / to 5.5V            |
|--|--|---|-----------------------|-----------------------|------------------------------------|----------------------|
| DC Input Diode Current (I <sub>IK</sub> )  | -20 mA   | Input Voltag                                    |                       |                       |                                    | V to V <sub>CC</sub> |
| $V_1 = -0.5V$<br>$V_1 = V_{CC} + 0.5V$   | + 20 mA  | Output Volta                                    | age (V <sub>O</sub> ) |                       | 0 Minimum Dynamic                  | V to V <sub>CC</sub> |
| DC Input Voltage (V <sub>I</sub> )   | -0.5V to V <sub>CC</sub> + 0.5V  | Operating T                                     |                       | ure (T <sub>A</sub> ) | -40°C to                           | +85°C                |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$  | -20 mA   | 54AC/AC   | Т                     | 8.8                   | −55°C to                           |                      |
| $V_{O} = V_{CC} + 0.5V$  | + 20 mA  | Minimum In                                      |                       | Rate (ΔV              | /Δt)                               |                      |
| DC Output Voltage (V <sub>O</sub> )  | $-0.5V$ to $V_{CC} + 0.5V$   | 'AC Device VIN from S                           |                       | 70% of V <sub>C</sub> | feet dumbon 2.0 ms, or             |                      |
| DC Output Source   | otive limit @ 5.5V Voc.  | V <sub>CC</sub> @ 3.3                           |                       |                       | naming sta VO.8 6 00 125           |                      |
| or Sink Current (IO)   | ± 50 mA  | Minimum In                                      | put Edge              | Rate (ΔV              | 7At)                               |                      |
|  |  |   |                       |                       |                                    |                      |
| DC V <sub>CC</sub> or Ground Current   |  | 'ACT Dev  | rices                 |                       | nd'i lanistoal                     | 300                  |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )   | ±50 mA   | V <sub>IN</sub> from                            | 0.8V to 2             | sotoos                | lectrical Cha                      | AC E                 |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )  | ±50 mA<br>-65°C to +150°C  |   | 0.8V to 2             | sotoos                | lectrical Cha                      | 5 mV/ns              |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) Storage Temperature (T <sub>STG</sub> ) Junction Temperature (T <sub>J</sub> ) CDIP PDIP  |  | V <sub>IN</sub> from                            | 0.8V to 2<br>5V, 5.5V | sotoos                | lectrical Cha                      | 5 mV/ns              |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) Storage Temperature (T <sub>STG</sub> ) Junction Temperature (T <sub>J</sub> ) CDIP PDIP Note 1: Absolute maximum ratings are those  | -65°C to +150°C  175°C  140°C  e values beyond which damage  | V <sub>IN</sub> from 0<br>V <sub>CC</sub> @ 4.5 | 0.8V to 2<br>5V, 5.5V | 2.0V 381              | lectrical Char<br>121              |                      |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) Storage Temperature (T <sub>STG</sub> ) Junction Temperature (T <sub>J</sub> ) CDIP PDIP Note 1: Absolute maximum ratings are those to the device may occur. The databook speciexception, to ensure that the system design i | -65°C to +150°C  175°C  140°C  e values beyond which damage flications should be met, without s reliable over its power supply,                              | V <sub>IN</sub> from V <sub>CC</sub> @ 4.5      | 0.8V to 2<br>5V, 5.5V | 2.0V                  | lectrical Char<br>129<br>Paremeter |                      |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) Storage Temperature (T <sub>STG</sub> ) Junction Temperature (T <sub>J</sub> ) CDIP PDIP   | -65°C to +150°C  175°C 140°C e values beyond which damage fications should be met, without so reliable over its power supply, bles. National does not recom- | V <sub>IN</sub> from 0<br>V <sub>CC</sub> @ 4.5 | 0.8V to 2<br>5V, 5.5V | 2.0V 381              | lectrical Char<br>121              |                      |

#### DC Characteristics for 'AC Family Devices

|                           | 6 11.0                               | 8                      | 74                      | AC                   | 10,5                              | 54AC                | 2.6                             | 74AC                 | sion Deia                       | spacon9 Jaq   |  |
|---------------------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------|---------------------------------|----------------------|---------------------------------|---|--|
| Symbol                    | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to + 125°C |                     | T <sub>A</sub> = -40°C to +85°C |                      | Units                           | Conditions  |  |
|                           |                                      |                        | Тур                     |                      |                                   | Guaranteed L        | imits                           |                      | 18.0 ± V0.6                     | Voltage Flange 5.0 is   |  |
| V <sub>IH</sub>           | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | aW rot S<br>AC                    | 2.1<br>3.15<br>3.85 | :eine                           | 2.1<br>3.15<br>3.85  | V                               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> IN<br>No. | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | + 26°C<br>50 pF                   | 0.9<br>1.35<br>1.65 | Ycc."<br>(V)                    | 0.9<br>1.35<br>1.65  | ٧                               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>           | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 0.8<br>0.8                        | 2.9<br>4.4<br>5.4   | 3.3                             | 2.9<br>4.4<br>5.4    | DIH Vmil                        | I <sub>OUT</sub> = -50 μA<br>guide3<br>of nO  |  |
| 2-7                       | 2.0 ns                               | 3.0                    | 4.0<br>4.0              | 2.56                 | 2.0                               | 2.4 0.1             | 3.3                             | 2.46                 | ime, HiGh                       | $*V_{IN} = V_{IL} \text{ or } V_{IH} - 12 \text{ mA}$                                   |  |
| 2-7                       | an 0.S                               | 4.5<br>5.5             | 2.5                     | 3.86<br>4.86         | 2.0                               | 3.7<br>4.7          | 3.8<br>R.0                      | 3.76<br>4.76         | Firms, HIG                      | l <sub>OH</sub> −24 mA<br>−24 mA  |  |
| V <sub>OL</sub>           | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 2.0                               | 0.1<br>0.1<br>0.1   | 3.8                             | 0.1<br>0.1<br>0.1    | all em                          | Ι <sub>ΟυΤ</sub> = 50 μΑ  |  |
| 2-3                       | 6,5<br>4,0 ns                        | 3.0<br>4.5<br>5.5      | 8.8                     | 0.36<br>0.36<br>0.36 | 3.6                               | 0.5<br>0.5<br>0.5   | 5.0                             | 0.44<br>0.44<br>0.44 | WOJ W<br>Ve,o voje<br>Ve,o voje | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA I <sub>OL</sub> 24 mA 24 mA |  |
| I <sub>IN</sub>           | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 |                                   | ±1.0                |                                 | ±1.0                 | μΑ                              | $V_{l} = V_{CC}$ , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

|                  | 1/2 /                               | (4) | TZ     | 00       | -33 C 10 T 123 C | -40 C TO TOO C |          | Supply Voltage (Vod                      |  |
|------------------|-------------------------------------|-----|--------|----------|------------------|----------------|----------|--|--|
| anV st V0        |                                     |     | Тур    | palioV   | Guaranteed I     | Limits         | (NI) the | DC Input Diode Curt                      |  |
| I <sub>OLD</sub> | †Minimum Dynamic                    | 5.5 | oV) es | siloV fi | 1qtuO 50 Am 02 - | 75             | mA       | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD             | Output Current                      | 5.5 | steque | T gails  | -50/30 4 5       | oV of Velt 75  | mA       | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc si           | Maximum Quiescent<br>Supply Current | 5.5 | 7      | 4.0      | 0.08 Selection   | 40.0           | μА       | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. ICC for 54AC @ 25°C is identical to 74AC @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  | 121                                       |                          | 5V, 5.5V   | 74AC  | 0           | 081 - 54   | AC          | 74         | AC   | negme T     | Storage                          |
|------------------|---|--------------------------|------------|---|-------------|------------|-------------|------------|--|-------------|----------------------------------|
| Symbol           | Parameter                                 | V <sub>CC</sub> *<br>(V) |            | $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ |             | Units      | Fig.        |            |  |             |                                  |
|                  |   |                          | Min        | Тур   | Max         | Min        | Max         | Min        | Max  | ice resy on | no sine de                       |
| f <sub>max</sub> | Maximum Clock<br>Frequency                | 3.3<br>5.0               | 125<br>160 | 160<br>200  |             | 95<br>95   |             | 110<br>145 | THAT THE BYTEN<br>SOLL TINDENT TO<br>SECTIVE CROSSES | MHz         | temperal<br>temperal<br>toend op |
| t <sub>PLH</sub> | Propagation Delay<br>CP to Q <sub>n</sub> | 3.3<br>5.0               | 2.5<br>1.5 | 8.5<br>6.0  | 11.0<br>8.0 | 1.5<br>1.5 | 12.0<br>9.0 | 2.5<br>1.5 | 12.5<br>9.0  | ns          | 2-3, 4                           |
| t <sub>PHL</sub> | Propagation Delay<br>CP to Q <sub>n</sub> | 3.3<br>5.0               | 2.5        | 8.0<br>5.5  | 10.5<br>7.5 | 1.5<br>1.5 | 12.0<br>7.5 | 2.5<br>1.5 | 11.0<br>8.0  | ns          | 2-3, 4                           |

<sup>\*</sup>Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

#### AC Operating Requirements: See Section 2 for Waveforms

|   | 30 4.10                    |                      | 8.85           |                   | 74/  | AC         | 8.85               | 54AC  | 3.5        | 74AC   | NO SPICE |      |
|---|----------------------------|----------------------|----------------|-------------------|--|------------|--------------------|---|------------|--|----------|------|
| Symbol  | Vour *                     | Paramet              | er 9.0<br>1.35 | V <sub>CC</sub> * | * T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | 0.0<br>88.1        | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |            | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units    | Fig. |
| An 02-  | = mol                      |                      | 2.9            |                   | Тур  |            | Guaranteed Minimum |   |            |  | minulyi  |      |
| t <sub>s</sub>                                | Setup<br>D <sub>n</sub> to | Time, HIG<br>CP      | H or LOW       | 3.3<br>5.0        | 1.5  | 3.0<br>2.0 | 4.4                | 4.0   | 4,5<br>5.5 | 3.5 No / 1<br>2.5  | ns ns    | 2-7  |
| V <sub>R</sub> or V <sub>d</sub> t<br>- 12 mA | Hold 7                     | ime, HIGH            | or LOW         | 3.3<br>5.0        | 1.0  | 2.0<br>2.0 | 2,56               | 4.0   | 0.8        | 2.0<br>2.0   | ns       | 2-7  |
| ts  |                            | Time, HIG<br>E to CP | H or           | 3.3<br>5.0        | 0  | 2.0        | 88.4               | 2.5<br>2.5  | 4.5<br>5.5 | 2.0  | ns       | 2-7  |
| th Autor                                      |                            | ime, HIGH<br>E to CP | lor 1.0        | 3.3<br>5.0        | 1.0<br>1.0   | 2.0<br>2.0 | 1.0                | 4.0<br>4.0  | 3.0<br>4.5 | 2.0<br>2.0   | ns ns    | 2-7  |
| t <sub>w</sub> V no JIV                       | THE RESERVE OF             | lse Width<br>or LOW  |                | 3.3<br>5.0        | 3.0<br>2.0   | 4.5<br>3.5 |                    | 6.5<br>6.5  |            | 5.5<br>4.0   | ns       | 2-3  |

<sup>\*</sup>Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

#### Capacitance

| Symbol          | Parameter                     | Тур | Units                    | Conditions      |
|-----------------|-------------------------------|-----|--------------------------|-----------------|
| CIN             | Input Capacitance             | 4.5 | a ta bebea PFotus era an | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 28  | pF                       | $V_{CC} = 5.0V$ |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.



### 54ACT/74ACT399 Quad 2-Port Register

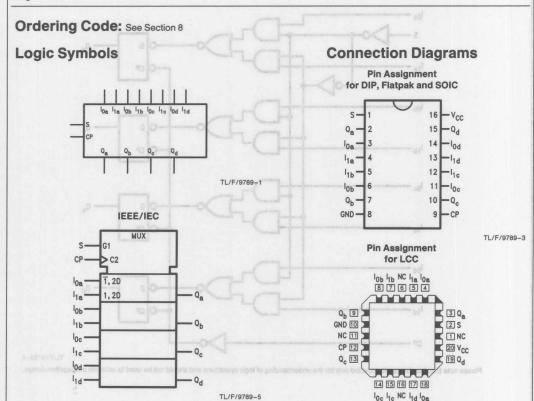
#### **General Description**

The 'ACT399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock.

The 'ACT399 is a high-speed quad 2-port register. It selects four bits of data from either of two sources (Porte) under control of a common Select Input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH iransition of the Clock Input (CP). The 4-bit D-type output register is fully edite-triggered. The Data inputs (IDs. (Is)) and Select Input (S) must be stable only a

#### **Features**

- Select inputs from two data sources
- Fully positive edge-triggered operation
- Outputs source/sink 24 mA
- 'ACT399 has TTL-compatible inputs 1990 3



| Pin Names                        | Description               |  |
|----------------------------------|---------------------------|--|
| S                                | Common Select Input       |  |
| CP                               | Clock Pulse Input         |  |
| I <sub>0a</sub> -I <sub>0d</sub> | Data Inputs from Source 0 |  |
| I <sub>1a</sub> -I <sub>1d</sub> | Data Inputs from Source 1 |  |
| Qa-Qd                            | Register True Outputs     |  |

TL/F/9789-2

#### **Functional Description**

The 'ACT399 is a high-speed quad 2-port register. It selects four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I<sub>0x</sub>, I<sub>1x</sub>) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation.

log he MO he log

W Select inputs from two data sources

a 'AOTSS9 has TTL-compa

a Fully positive edge-inggered operation M Outputs source/sink 24 mA

#### **Function Table**

|   | In             | puts |    | Out | puts |
|---|----------------|------|----|-----|------|
| S | I <sub>0</sub> | 11   | CP | Q   | Q    |
| L | L              | X    | 5  | L   | Н    |
| L | HO             | X    | AV | Н   | L    |
| Н | X              | L    | 5  | L   | Н    |
| Н | X              | Н    |    | Н   | SU L |

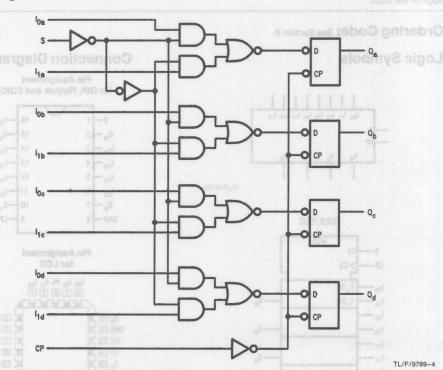
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

✓ = LOW-to-HIGH Clock Transition

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1) If Military/Aerospace specified devices are required,

please contact the National Semiconductor Sales Office/Distributors for availability and specifications. Supply Voltage ( $V_{\rm CC}$ )  $-0.5 {\rm V} \ {\rm to} \ +7.0 {\rm V}$ 

DC Input Diode Current ( $I_{IK}$ )  $V_I = -0.5V$   $V_I = V_{CC} + 0.5V$ DC Input Voltage ( $V_I$ ) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Diode Current ( $I_{OK}$ )  $V_O = -0.5V$  $V_O = V_{CC} + 0.5V$ 

DC Output Voltage (V<sub>O</sub>) -0.5V to V<sub>CC</sub> + 0.5V DC Output Source or Sink Current (I<sub>O</sub>) ±50 mA

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) Storage Temperature (T<sub>STG</sub>)

Junction Temperature (T<sub>J</sub>)

CDIP

+ 175°C

+ 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Recommended Operating 100 B OA Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 'ACT
 4.5V to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

 Output Voltage (V<sub>O</sub>)
 0V to V<sub>CC</sub>

Operating Temperature (T<sub>A</sub>)
74AC/ACT
54AC/ACT

-40°C to +85°C -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices V<sub>IN</sub> from 0.8V to 2.0V

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

125 mV/ns

#### **DC Electrical Characteristics for 'ACT Family Devices**

-20 mA

+20 mA

±50 mA

-65°C to +150°C

|                 |                                     |                        | 744                   | CT           | 54ACT                             | 74ACT                           | o HENH  | smiT gute2  |  |
|-----------------|-------------------------------------|------------------------|-----------------------|--------------|-----------------------------------|---------------------------------|---------|---|--|
| Symbol          | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units   | Conditions  |  |
|                 |                                     |                        | Тур                   | 2.5          | Guaranteed L                      | imits 0.8                       | HOH OF  | Canti piori   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5            | 2.0<br>2.0   | 2.0<br>2.0                        | 2.0<br>2.0                      | V       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5            | 0.8          | 0.8<br>0.8                        | 0.8<br>0.8                      | va.V. v | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level                  | 4.5<br>5.5             | 4.49<br>5.49          | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧       | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 | Condition Voc = 8                   | 4.5<br>5.5             |                       | 3.86<br>4.85 | 3.70<br>4.70                      | 3.76<br>4.76                    | n) V    | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OH</sub> -24 mA<br>-24 mA |  |
| VOL             | Maximum Low Level<br>Output Voltage | 4.5<br>5.5             | 0.001<br>0.001        | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧       | 1 <sub>OUT</sub> = 50 μA  |  |
|                 |                                     | 4.5<br>5.5             |                       | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | ٧       | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OL</sub> 24 mA<br>24 mA   |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current    | 5.5                    |                       | ±0.1         | ±1.0                              | ±1.0                            | μΑ      | V <sub>I</sub> = V <sub>CC</sub> , GND  |  |
| ГССТ            | Maximum I <sub>CC</sub> /Input      | 5.5                    | 0.6                   |              | 1.6                               | 1.5                             | mA      | $V_1 = V_{CC} - 2.1V$   |  |
| IOLD            | †Minimum Dynamic                    | 5.5                    |                       |              | 50                                | 75                              | mA      | V <sub>OLD</sub> = 1.65V Max  |  |
| IOHD            | Output Current                      | 5.5                    |                       |              | -50                               | -75                             | mA      | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc             | Maximum Quiescent<br>Supply Current | 5.5                    |                       | 8.0          | 160                               | 80                              | μА      | V <sub>IN</sub> = V <sub>CC</sub><br>or Ground  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test,

Note: I<sub>CC</sub> for the 54ACT device is identical to the 74ACT device at 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |                              |                   | 74ACT   | 54ACT |  | 74ACT    |  | restyrach<br>contra | elense |             |
|------------------|------------------------------|-------------------|---|-------|--|----------|--|---------------------|--------|-------------|
| Symbol           | Vo.8<br>Va.b Parameter       | V <sub>CC</sub> * | $T_A = +25^{\circ}$<br>$V_{CC} = +5.0$<br>$C_L = 50 \text{ pF}$ | V     | T <sub>A</sub> , V <sub>CC</sub> = Mil<br>C <sub>L</sub> = 50 pF |          | T <sub>A</sub> , V <sub>CC</sub> = Com<br>C <sub>L</sub> = 50 pF |                     | Units  | Fig.<br>No. |
| 20V et V0        |                              | Min Typ           | Max   | Min   | Max  | Min      | Max  | V8.0-               | = (V - |             |
| f <sub>max</sub> | Input Clock Frequency        | 5.0               | 165 160   | V     | 90   | os Vã 0- | 160  | AVLO                | MHz    | DC lat      |
| tPLH             | Propagation Delay<br>CP to Q | 5.0               | 1.5 7.0   | 8.0   | m 03 —   | 10.0     | 1.5  | 8.5                 | ns ns  | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>CP to Q | 5.0               | 2.0 6.0   | 9.0   | + 20 nl  | 10.0     | 2.0  | 9.5                 | lo ns  | 2-3, 4      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

#### AC Operating Requirements: See Section 2 for Waveforms

|                  | 125                                | . Va              | 74   | CT                    | 54ACT  |     |          | 74ACT   |   | eT noits | mut   |
|------------------|------------------------------------|-------------------|--|-----------------------|--|-----|----------|---|---|----------|-------|
| Symbol Parameter |                                    | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |                       | T <sub>A</sub> = -55°C to +125°C<br>C <sub>L</sub> = 50 pF |     |          | T <sub>A</sub> = -40°C to +85°C<br>C <sub>L</sub> = 50 pF |   | Units    | Fig.  |
|                  |                                    |                   | Тур  | yp Guaranteed Minimum |  |     |          |   |   |          | to th |
| ts               | Setup Time, HIGH or LOW In to CP   | 5.0               | 3.0  | 2.5                   | opply,<br>sount-   | 3.5 |          | grid te<br>enidelse<br>de den                             | e gribs 2.5 qui taque bin<br>o de PACTEM circuits outsi | ns       | 2-7   |
| t <sub>h</sub>   | Hold Time, HIGH or LOW In to CP    | 5.0               | 0  | 1.0                   | ACT  | 3.0 | eoiteir  | oto   | cirleal 0.nara  | ns       | 2-7   |
| ts               | Setup Time, HIGH or LOW<br>S to CP | 5.0               | 3.0  | 4.0                   |  | 6.0 | ANS - AT | soV   | 4.0   | ns       | 2-7   |
| t <sub>h</sub>   | Hold Time, HIGH or LOW<br>S to CP  | 5.0               | -1.0   | 0.5                   | 0 08   | 2.5 | Typ      | (4)   | 0.5   | ns       | 2-7   |
| t <sub>w</sub>   | CP Pulse Width<br>HIGH or LOW      | 5.0               | 5.5  | 3.5                   |  | 5.0 | 1.5      | 6.5   | 3.5 SalloV luc  | ns       | 2-3   |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

#### Capacitance

| Symbol   |      | Parameter            |         | Тур |       | Unit | Condition           | ns  |
|--|------|----------------------|---------|-----|-------|------|---------------------|-----|
| Am CIN HO  | Inpu | ıt Capacitance       | 3.70    | 4.5 |       | pF   | V <sub>CC</sub> = 5 | .0V |
| C <sub>PD</sub>  | Pow  | er Dissipation Capac | citance | 30  | 1000  | pF   | $V_{CC} = 5$        | .0V |
|  | V    | t.0                  | t.0     | 1.0 | 0.001 | 8.6  | Output Voltage      | 30. |
| *V <sub>HV</sub> = V <sub>H</sub> , or V <sub>H</sub><br>24 mA<br>24 mA<br>24 mA | ٧    | 0.44                 |         |     |       |      |                     |     |
| VI = V <sub>CO</sub> , GND   |      |                      |         |     |       |      |                     |     |
| VIS-30V=IV   | Am   |                      |         |     |       |      |                     |     |
| Vol.0 = 1.65V Max  | Am   |                      |         |     |       | 5.5  |                     |     |
| VOND = 3.86V Min   |      |                      |         |     |       |      |                     | ано |
| V <sub>IN</sub> = V <sub>CC</sub><br>or Ground                                   |      |                      |         |     |       |      |                     |     |



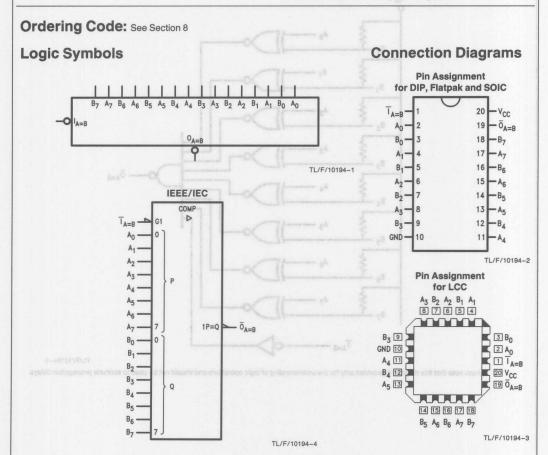
### 54AC/74AC520 • 54ACT/74ACT520 8-Bit Identity Comparator

#### **General Description**

The 'AC/'ACT520 are expandable 8-bit comparators. They compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input  $\tilde{I}_{A} \equiv B$  also serves as an active LOW enable input.

#### **Features**

- Compares two 8-bit words in 6.5 ns typ
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT520 has TTL-compatible inputs



| Pin Names                      | Description               |
|--------------------------------|---------------------------|
| A <sub>0</sub> -A <sub>7</sub> | Word A Inputs             |
| B <sub>0</sub> -B <sub>7</sub> | Word B Inputs             |
| $T_A = B$                      | Expansion or Enable Input |
| $\overline{O}_A = B$           | Identity Output           |

#### **Truth Table**

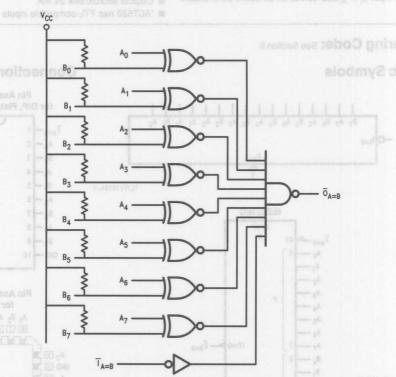
| In                 | Inputs     |                      |  |  |  |  |  |
|--------------------|------------|----------------------|--|--|--|--|--|
| Ī <sub>A</sub> = B | A, B       | $\overline{O}_A = B$ |  |  |  |  |  |
| L                  | A = B*     | odaro                |  |  |  |  |  |
| L                  | $A \neq B$ | Horse                |  |  |  |  |  |
| Н                  | $A = B^*$  | Н                    |  |  |  |  |  |
| Н                  | $A \neq B$ | Н                    |  |  |  |  |  |

H = HIGH Voltage Level L = LOW Voltage Level

\*A<sub>0</sub> = B<sub>0</sub>, A<sub>1</sub> = B<sub>1</sub>, A<sub>2</sub> = B<sub>2</sub>, etc.

#### **Logic Diagram**

08 E 380



TL/F/10194-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Fin Hames Description

Ao-Ar Word A Inputs.

Bo-Br World B Inputs

TA - B Expansion or Enable Input

CA - B Identity Output

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V Supply Voltage (V<sub>CC</sub>) DC Input Diode Current (IIK) -20 mA  $V_1 = -0.5V$ +20 mA  $V_I = V_{CC} + 0.5V$ -0.5V to  $V_{CC} + 0.5V$ 

DC Input Voltage (V<sub>I</sub>) DC Output Diode Current (IOK)  $V_0 = -0.5V$ -20 mA

 $V_O = V_{CC} + 0.5V$ +20 mA -0.5V to  $V_{CC} + 0.5V$ DC Output Voltage (VO) DC Output Source

or Sink Current (IO) DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) -65°C to +150°C Storage Temperature (TSTG)

Junction Temperature (T<sub>J</sub>) CDIP PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

#### Recommended Operating **Conditions**

Supply Voltage (VCC) 2.0V to 6.0V 'AC AS + AT 'ACT 4.5V to 5.5V OV to VCC Input Voltage (VI) OV to V<sub>CC</sub> Output Voltage (VO) Operating Temperature (TA) -40°C to +85°C 74AC/ACT -55°C to +125°C 54AC/ACT

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

125 mV/ns

#### DC Characteristics for 'AC Family Devices

±50 mA

±50 mA

175°C

140°C

|  | UJ* 12                               | 1000              | 74                      | AC                   | 1000  | 54AC                 | 0.0        | 74AC                            | - Congravi                     | and the same of th |  |
|--|--------------------------------------|-------------------|-------------------------|----------------------|-------|----------------------|------------|---------------------------------|--------------------------------|--|--|
| Symbol                                     | Parameter                            | V <sub>CC</sub>   | T <sub>A</sub> =        | + 25°C               | -55   | T <sub>A</sub> =     | 125°C      | T <sub>A</sub> = -40°C to +85°C | Units                          | Conditions   |  |
|  | A = NIA.                             | .76               | Тур                     |                      | 3.70  | Guara                | nteed L    | imits                           |                                |  |  |
| VIH  | Minimum High Level                   | 3.0               | 1.5                     | 2.1                  | 4,70  | 2.1                  | 4.86       | 2.1                             |                                | V <sub>OUT</sub> = 0.1V  |  |
| Aq 0                                       | Input Voltage                        | 4.5<br>5.5        | 2.25<br>2.75            | 3.15<br>3.85         | 0.1   | 3.15<br>3.85         | 1.0<br>1.0 | 3.15<br>3.85                    | n Law Law                      | or V <sub>CC</sub> - 0.1V  |  |
| IL Or V <sub>I</sub> LIV<br>24 mA<br>24 mA | Maximum Low Level Input Voltage      | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.50  | 0.9<br>1.35<br>1.65  | 80.0       | 0.9<br>1.35<br>1.65             | V                              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub> M <sub>O</sub>             | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 0.1±  | 2.9<br>4.4<br>5.4    |            | 2.9<br>4.4<br>5.4               | n Input<br>Cultrent            | $I_{OUT} = -50 \mu\text{A}$  |  |
|  | $mA$ $V_1 = V_{QC}$                  | 1.5               |                         |                      | 1.6   |                      |            | 8.8 0.8                         | 1                              | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>  |  |
|  | = gueV Am                            | 3.0<br>4.5        |                         | 2.56<br>3.86         | so    | 2.4<br>3.7           |            | 2.46<br>3.76                    | V                              | -12 mA<br>I <sub>OH</sub> -24 mA   |  |
| nIM Yea.s                                  | = aHoV Am                            | 5.5               |                         | 4.86                 | -50   | 4.7                  |            | 4.76                            | METRI                          | -24 mA   |  |
| V <sub>OL</sub>                            | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 160.0 | 0.1<br>0.1<br>0.1    |            | 0.1<br>0.1<br>0.1               | n Ourleade<br>Surr Vitt        | 001  |  |
|  |                                      | 3.0<br>4.5<br>5.5 |                         | 0.36<br>0.36<br>0.36 |       | 0.50<br>0.50<br>0.50 |            | 0.44<br>0.44<br>0.44            | 2.0 ms, un<br>serb la los<br>V | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA 1 <sub>OL</sub> 24 mA 24 mA  |  |
| I <sub>IN</sub>                            | Maximum Input<br>Leakage Current     | 5.5               |                         | ±0.1                 |       | ±1.0                 |            | ±1.0                            | μА                             | $V_I = V_{CC}$ , GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

### DC Characteristics for 'AC Family Devices (Continued) The American American

|          |                                     |                        | 74               | AC        | 54AC             | 74AC                            | Light ent  | please contact                           |  |
|----------|-------------------------------------|------------------------|------------------|-----------|------------------|---------------------------------|------------|--|--|
| Symbol   | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C    | T <sub>A</sub> = | T <sub>A</sub> = -40°C to +85°C | Units      | Conditions                               |  |
| coV of V | 0                                   |                        | Тур              | ut Voltag | Guaranteed L     | imits                           | (hit) Inev | DC Input Diode Cu                        |  |
| IOLD     | †Minimum Dynamic                    | 5.5                    | (9,k) eds        | aloV augi | 50m 95+          | 75                              | mA         | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD     | Output Current                      | 5.5                    | asneqnia<br>T    | argeng 1  | -50 0 + 00       | / of V2.0=75                    | mA (       | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc      | Maximum Quiescent<br>Supply Current | 5.5                    | T<br>out Edge    | 8.0       | 160.0 05         | 80.0                            | μΑ         | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### **DC Characteristics for 'ACT Family Devices**

|  |                                      |                     | 74A                    | CT           |                                  | 54ACT        |                                 | 74ACT                  | (LT) en                       |   |  |  |
|--|--------------------------------------|---------------------|------------------------|--------------|----------------------------------|--------------|---------------------------------|------------------------|-------------------------------|---|--|--|
| Symbol                                       | Parameter                            | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = -55°C to +125°C |              | T <sub>A</sub> = -40°C to +85°C | Units                  | Conditions                    |   |  |  |
|  |                                      |                     | Тур                    |              |                                  | Guarai       | nteed L                         | imits                  | The databook                  | to the device may occur,  |  |  |
| V <sub>IH</sub>                              | Minimum High Level<br>Input Voltage  | 4.5<br>5.5          | 1.5<br>1.5             | 2.0<br>2.0   |                                  | 2.0          | is not rac<br>stions.           | 2.0<br>2.0             | probabilismo<br>too etapV) en | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |  |
| V <sub>IL</sub>                              | Maximum Low Level Input Voltage      | 4.5<br>5.5          | 1.5<br>1.5             | 0.8          | eeol                             | 0.8          | mily                            | 0.8                    | is lie                        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |  |
| V <sub>OH</sub>                              | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49           | 4.4<br>5.4   | = AT                             | 4.4<br>5.4   | 3.62                            | 4.4<br>5.4             | V                             | $I_{OUT} = -50 \mu\text{A}$   |  |  |
|  | PIC Vout =                           | 4.5<br>5.5          | o ua<br>stimi          | 3.86<br>4.86 | Guara<br>Guara<br>2.1            | 3.70<br>4.70 | 2.1                             | 3.76<br>4.76           | V<br>High Level               | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &-24 \mbox{ mA} \\ I_{OH} &-24 \mbox{ mA} \end{tabular}$ |  |  |
| Vol  | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5          | 0.001<br>0.001         | 0.1<br>0.1   | 3.15                             | 0.1          | 3.15                            | 0.1<br>0.1<br>0.1      | v ega                         | Ι <sub>ΟUT</sub> = 50 μΑ  |  |  |
| V1.0<br>- 0.1V                               | TUOV<br>OO OF VO                     | 4.5<br>5.5          |                        | 0.36<br>0.36 | 0.9<br>1,35<br>1.65              | 0.50<br>0.50 | 1.65                            | 0.44<br>0.44           | Low Level                     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$  |  |  |
| IIN  | Maximum Input<br>Leakage Current     | 5.5                 |                        | ±0.1         | 8.8<br>4.4                       | ±1.0         | 2.9                             | 08.S 0.6<br>03.5 ±1.05 | μA                            | $V_I = V_{CC}$ , GND  |  |  |
| ICCT   | Maximum<br>I <sub>CC</sub> /Input    | 5.5                 | 0.6                    |              | 9.0                              | 1.6          | 9,0                             | 1.5                    | mA                            | $V_I = V_{CC} - 2.1V$   |  |  |
| lold   | †Minimum Dynamic                     | 5.5                 |                        |              | 2.7                              | 50           | 88.8                            | 75                     | mA                            | V <sub>OLD</sub> = 1.65V Max  |  |  |
| IOHD -                                       | Output Current                       | 5.5                 |                        |              | 4.7                              | -50          | 4,88                            | -75                    | mA                            | V <sub>OHD</sub> = 3.85V Min  |  |  |
| I <sub>CC</sub> <sup>A</sup> <sub>A</sub> 08 | Maximum Quiescent<br>Supply Current  | 5.5                 |                        | 8.0          | 1.0                              | 160.0        | 1.0                             | 80.0                   | μА                            | V <sub>IN</sub> = V <sub>CC</sub> or GND  |  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

|   | 7 | 'n |   |   |  |
|---|---|----|---|---|--|
| ľ | 1 | •  |   | ۹ |  |
|   |   | Ł  | Ц |   |  |
|   |   |    |   |   |  |

| Symbol Parameter |  | (V)        | C <sub>L</sub> = 50 pF |            |             | to + 125°C<br>C <sub>L</sub> = 50 pF |              | to +85°C<br>C <sub>L</sub> = 50 pF |              | Units        | No.   |
|------------------|--|------------|------------------------|------------|-------------|--------------------------------------|--------------|------------------------------------|--------------|--------------|-------|
|                  |  |            | Min                    | Тур        | Max         | Min                                  | Max          | Min                                | Max          | in the man f | man A |
| t <sub>PLH</sub> | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$           | 3.3<br>5.0 | 4.0<br>2.5             | 7.5<br>5.5 | 11.5<br>8.5 | 1.0<br>1.5                           | 14.0<br>10.5 | 3.0<br>2.0                         | 13.0<br>9.5  | ns           | 2-3,  |
| t <sub>PHL</sub> | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$           | 3.3<br>5.0 | 4.5                    | 8.0<br>5.5 | 12.0<br>9.0 | 1.0<br>1.5                           | 15.0<br>11.0 | 3.5<br>2.5                         | 13.5<br>10.0 | ns           | 2-3,  |
| t <sub>PLH</sub> | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 3.3<br>5.0 | 3.5<br>2.5             | 5.5<br>4.5 | 8.5<br>6.5  | 1.0<br>1.5                           | 10.0<br>7.5  | 2.5<br>2.0                         | 9.5<br>7.0   | ns           | 2-3,  |
| t <sub>PHL</sub> | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 3.3<br>5.0 | 3.5<br>2.5             | 5.5<br>4.5 | 8.5<br>6.5  | 1.0<br>1.5                           | 10.5<br>8.0  | 2.5<br>2.0                         | 9.5<br>7.0   | ns           | 2-3,  |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### AC Electrical Characteristics: See Section 2 for Waveforms

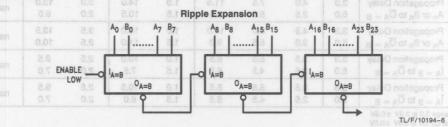
|                  | 55   | a Azs             | e aya  | 74ACT | As Ba | 54   | ACT . | 74/  | ACT  |       |             |
|------------------|--|-------------------|--|-------|-------|--|-------|--|------|-------|-------------|
| Symbol           | Parameter  | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |       | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |       | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.<br>No. |
|                  |  | O <sub>A=8</sub>  | Min  | Тур   | Max   | Min  | Max   | Min  | Max  |       |             |
| <sup>t</sup> PLH | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$       | 5.0               | 3.0  | 5.5   | 8.5   | 1.5  | 12.0  | 2.5  | 9.5  | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$       | 5.0               | 3.0  | 6.0   | 10.0  | 1.5  | 12.0  | 2.5  | 11.5 | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay $\overline{I}_A = B$ to $\overline{O}_A = B$ | 5.0               | 2.0  | 4.0   | 6.0   | 1.5  | 8.5   | 2.0  | 6.5  | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $\overline{I}_A = B$ to $\overline{O}_A = B$ | 5.0               | 2.5  | 5.0   | 7.5   | 1.5  | 9.0   | 2.0  | 8.5  | ns    | 2-3, 4      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

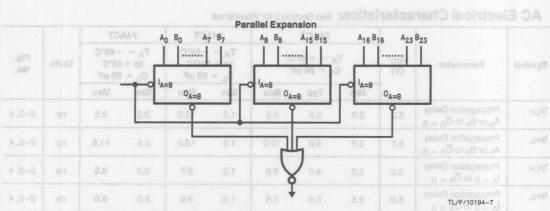
#### Capacitance

| Symbol | Parameter OAM                 | Тур | Units | Conditions      |
|--------|-------------------------------|-----|-------|-----------------|
| CIN    | Input Capacitance             | 4.5 | pF    | $V_{CC} = 5.0V$ |
| CPD    | Power Dissipation Capacitance | 40  | pF    | $V_{CC} = 5.0V$ |

#### **Applications**







Truth Table



### 54AC/74AC521 • 54ACT/74ACT521 **8-Bit Identity Comparator**

#### **General Description**

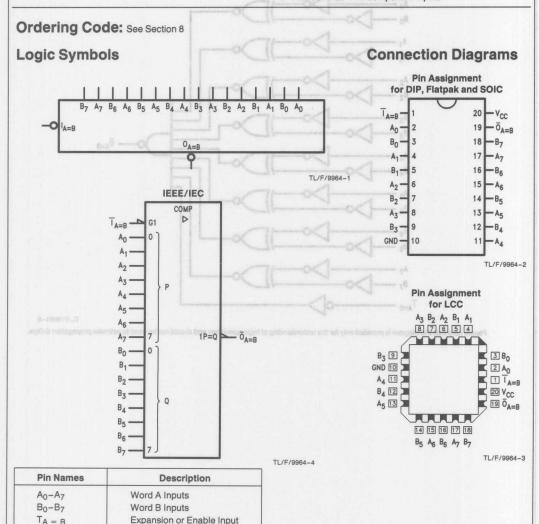
 $T_A = B$  $\overline{O}_A = B$ 

**Identity Output** 

The 'AC/'ACT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input  $\bar{I}_A = B$  also serves as an active LOW enable input.

#### **Features**

- Compares two 8-bit words in 6.5 ns typ = \_\_\_\_\_
- Expandable to any word length
- 20-pin package
- Outputs source/sink 24 mA
- 'ACT521 has TTL-compatible inputs



#### **Truth Table**

| In              | Outputs    |                      |
|-----------------|------------|----------------------|
| $\bar{I}_A = B$ | A, B       | $\overline{O}_A = B$ |
| L               | A = B*     | 5. L. 15. 1914       |
| L               | $A \neq B$ | THOIS                |
| Н               | $A = B^*$  | Н                    |
| Н               | $A \neq B$ | Н                    |

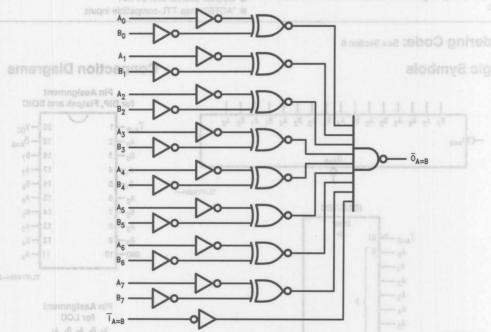
H = HIGH Voltage Level

L = LOW Voltage Level  $*A_0 = B_0$ ,  $A_1 = B_1$ ,  $A_2 = B_2$ , etc.

#### **Logic Diagram**

SAAC/74AC521 • 54ACT/74A 8-Bit Identity Comparator

The 'ACI'ACT521 is an expandable 8-bit comparator, it compares two words of up to eight bits each and provides a LOV output when the two words match bit for bit. The expansion input  $I_A=\mathfrak{g}$  also serves as an active LOW enable



TL/F/9964-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

08 (I) 80 0A (I) 88 8=A (II) 88

 Pln Names
 Description

 Ag-Ag
 Wiced A inputs

 Eq-Bg
 Word 8 inputs

 TA = p
 Expansion or Enable input

 CA = g
 Identity Output

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Output Voltage ( $V_O$ ) -0.5V to  $V_{CC}+0.5V$  DC Output Source or Sink Current ( $I_O$ )  $\pm 50$  mA

DC V<sub>CC</sub> or Ground Current per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) Storage Temperature (T<sub>STG</sub>)

Junction Temperature (T<sub>J</sub>)

CDIP

PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 'AC
 2.0V to 6.0V

 'ACT
 4.5V to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

 Output Voltage (V<sub>O</sub>)
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)

74AC/ACT —40°C to +85°C 54AC/ACT —55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

#### DC Characteristics for 'AC Family Devices

|                 | = Tuol v   | 3.3                 | 74                     | AC   | 5.5                               | 54AC           | 74AC                                 | out rimited    | VOH Minimun   |  |
|-----------------|--|---------------------|------------------------|------|-----------------------------------|----------------|--------------------------------------|----------------|---|--|
| Symbol          | Parameter  | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C |      | T <sub>A</sub> = -55°C to + 125°C |                | T <sub>A</sub> = 0<br>-40°C to +85°C | Units          | Conditions  |  |
|                 | The state of the s | 3.76                | Тур                    |      |                                   | Guaranteed L   | imits 8.4                            |                |   |  |
| VIH             | Minimum High Level   | 3.0                 | 1.5                    | 2.1  | 16.2                              | 2.1            | 2.1                                  |                | V <sub>OUT</sub> = 0.1V                               |  |
|                 | Input Voltage  | 4.5                 | 2.25                   | 3.15 | 1.0                               | 3.15           | 100.0 3.15 lev                       | V              | or V <sub>CC</sub> - 0.1V                             |  |
|                 |  | 5.5                 | 2.75                   | 3.85 | 1.0                               | 3.85           | 100.0 3.85                           | eggilo'        | / fugleO  |  |
| VILV 10 JI      | Maximum Low Level  | 3.0                 | 1.5                    | 0.9  |                                   | 0.9            | 0.9                                  |                | V <sub>OUT</sub> = 0.1V                               |  |
|                 | Input Voltage  | 4.5                 | 2.25                   | 1.35 | 0.50                              | 1.35           | 1.35                                 | V              | or V <sub>CC</sub> - 0.1V                             |  |
|                 | 701 A  | 5.5                 | 2.75                   | 1.65 | 0.50                              | 1.65           | 1.65                                 |                |   |  |
| VOH             | Minimum High Level   | 3.0                 | 2.99                   | 2.9  |                                   | 2.9            | 2.9                                  | n Input        | $I_{OUT} = -50 \mu\text{A}$                           |  |
|                 | Output Voltage   | 4.5                 | 4.49                   | 4.4  | MIT.                              | 4.4            | 4.4                                  | TO V           |   |  |
|                 | $V_l = V_{OO}$   | 5.5                 | 5.49                   | 5.4  |                                   | 5.4            | 5.4                                  |                |   |  |
|                 | Am   | C.T.                |                        |      | 5.1                               |                | 8.0   6.0                            | 1              | *V <sub>IN</sub> = V <sub>II</sub> or V <sub>IH</sub> |  |
|                 | = gloV Am  | 3.0                 |                        | 2.56 | Ga .                              | 2.4            | 2.46                                 | vsay() m       | 10  |  |
|                 |  | 4.5                 |                        | 3.86 | -                                 | 3.7            | 3.76                                 | V              | I <sub>OH</sub> -24 mA                                |  |
| 3.85V Min       | = akoV Am  | 5.5                 |                        | 4.86 | 98-                               | 4.7            | 4.76                                 | 71.151 4 557   | -24 mA  |  |
| V <sub>OL</sub> | Maximum Low Level  | 3.0                 | 0.002                  | 0.1  | 160                               | 0.1            | 0.1                                  | n Quiesq       | $I_{OUT} = 50 \mu A$                                  |  |
|                 | Output Voltage   | 4.5                 | 0.001                  | 0.1  |                                   | 0.1            | 0.1                                  | V              |   |  |
|                 |  | 5.5                 | 0.001                  | 0.1  |                                   | 0.1st sebra to | to rith to 0.1 see man               | o ablortes:    |   |  |
|                 |  |                     | K. 1. 1. 1.            |      |                                   |                | and a le bassol fugluo en            | n 2.0 ma, 1    | $*V_{IN} = V_{IL} \text{ or } V_{IH}$                 |  |
|                 |  | 3.0                 | 1-1                    | 0.36 |                                   | 0.50           | 0.44                                 | of all DYSS, 6 | 12 mA   |  |
|                 |  | 4.5                 | - 18                   | 0.36 |                                   | 0.50           | 0.44                                 | V              | I <sub>OL</sub> 24 mA                                 |  |
|                 |  | 5.5                 |                        | 0.36 |                                   | 0.50           | 0.44                                 | Out I V        | 24 mA   |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current   | 5.5                 |                        | ±0.1 |                                   | ±1.0           | ±1.0                                 | μΑ             | $V_{I} = V_{CC}$ , GND                                |  |

±50 mA

175°C

140°C

-65°C to +150°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) MISS MUMINISM STUDENTS

|           |                                     |                     | 74                     | AC         | 54AC                             | 74AC                            | ige sos   | If Military/Aaross                       |
|-----------|-------------------------------------|---------------------|------------------------|------------|----------------------------------|---------------------------------|-----------|--|
| Symbol Pa | Parameter                           | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C |            | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions                               |
|           | 0                                   |                     | Тур                    | ut Voltag  | Guaranteed L                     | imits                           | rent (lac | DC Input Diode Cu                        |
| IOLD OF   | †Minimum Dynamic                    | 5.5                 | (QV) eg                | put Volta  | 50                               | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max             |
| IOHD      | Output Current                      | 5.5                 | emperat                | Pretting T | -50.0 + 00                       | / of Va.0-75                    | mA        | V <sub>OHD</sub> = 3.85V Min             |
| Icc       | Maximum Quiescent<br>Supply Current | 5.5                 |                        | 8.0        | 160.0                            | 80.0                            | μΑ        | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .  $I_{CC}$  for 54AC @ 25°C is identical to 74AC @ 25°C.

#### **DC Characteristics for 'ACT Family Devices**

|                        |                                     |                        | 74.                    | ACT                   |                                      | 54ACT        |                   |                        | 74ACT                          | (i,T) en                    | Junction Temperat  |
|------------------------|-------------------------------------|------------------------|------------------------|-----------------------|--------------------------------------|--------------|-------------------|------------------------|--------------------------------|-----------------------------|--|
| Symbol                 | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |                       | T <sub>A</sub> =<br>-55°C to + 125°C |              |                   | -40°                   | T <sub>A</sub> =<br>C to +85°C |                             | Conditions   |
|                        |                                     |                        | Тур                    | Typ Guaranteed Limits |                                      |              |                   |                        | ok appecification              | um relings u<br>The detailo | to the device may occur  |
| V <sub>IH</sub>        | Minimum High Level Input Voltage    | 4.5<br>5.5             | 1.5<br>1.5             | 2.0<br>2.0            |                                      | 2.0          | power<br>of rueon | n teob ti<br>nestuolik | 2.0                            | graty and                   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>        | Maximum Low Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5             | 0.8                   | eeoi                                 | 0.8          | lims              | A O                    | 0.8                            | V                           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub>        | Minimum High Level Output Voltage   | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4            | SAAR<br>YA                           | 4.4<br>5.4   | AC                | 24                     | 4.4<br>5.4                     | V                           | $I_{OUT} = -50 \mu\text{A}$  |
| VEO                    | E mio∧                              | 4.5<br>5.5             | O'GA-<br>etim          | 3.86<br>4.86          | el Or<br>ticulo<br>e e               | 3.70<br>4.70 | 2 1               | Typ                    | 3.76<br>4.76                   | V                           | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| Vol.1.0 -              | Maximum Low Level<br>Output Voltage | 4.5<br>5.5             | 0.001                  | 0.1<br>0.1            | 3.85                                 |              | 3.19              | 2.25<br>2.76           | 0.1                            | V                           | I <sub>OUT</sub> = 50 μA   |
| V1.0<br>V1.0 -         | Vour =<br>V or Vac                  | 4.5                    |                        | 0.36<br>0.36          | 0.8<br>1,35<br>1,85                  | 0.50         | 1.9               | 1.5<br>2.25<br>2.75    | 0.44<br>0.44                   | V V                         | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub> 4 08 - | Maximum Input<br>Leakage Current    | 5.5                    |                        | ±0.1                  | 2.5                                  | ±1.0         | 2.9               | 2.98                   | ±1.0                           | μΑ                          | V <sub>I</sub> = V <sub>CC</sub> , GND   |
| ICCT                   | Maximum<br>I <sub>CC</sub> /Input   | 5.5                    | 0.6                    |                       | 4,8                                  | 1.6          | 6.4               | 8.48                   | 1.5                            | mA                          | $V_I = V_{CC} - 2.1V$  |
| I <sub>OLD</sub>       | †Minimum Dynamic                    | 5.5                    |                        |                       | 2.5                                  | 50           | 2.6               |                        | 75                             | mA                          | V <sub>OLD</sub> = 1.65V Max   |
| lohd                   | Output Current                      | 5.5                    |                        |                       | 4.7                                  | -50          | 8.5               |                        | -75                            | mA                          | V <sub>OHD</sub> = 3.85V Min   |
| loc <sub>All</sub> 08  | Maximum Quiescent<br>Supply Current | 5.5                    |                        | 8.0                   | 1.0<br>1.0                           | 160.0        | 0.0               | 0.002                  | 80.0                           | μА                          | V <sub>IN</sub> = V <sub>CC</sub> or GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: ICC for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |  |                   |            | 74AC   | ppie Exp      | 9 54       | AC                      | 74/              | AC          |       |             |
|------------------|--|-------------------|------------|--|---------------|------------|-------------------------|------------------|-------------|-------|-------------|
| Symbol           | Parameter  | V <sub>CC</sub> * |            | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF | gA<br>andread | to +       | -55°C<br>125°C<br>50 pF | T <sub>A</sub> = | 85°C        | Units | Fig.<br>No. |
|                  |  |                   | Min        | Тур  | Max           | Min        | Max                     | Min              | Max         |       |             |
| t <sub>PLH</sub> | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$           | 3.3<br>5.0        | 3.5<br>2.5 | 7.0<br>5.0                                       | 11.0<br>8.0   | 1.0        | 15.0<br>10.5            | 3.0<br>2.0       | 12.0<br>9.0 | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$           | 3.3<br>5.0        | 4.5<br>3.0 | 7.5<br>5.5                                       | 11.5<br>8.5   | 1.0        | 15.0<br>10.5            | 3.5<br>2.5       | 12.5<br>9.0 | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay $\overline{I}_{A} = B$ to $\overline{O}_{A} = B$ | 3.3<br>5.0        | 3.0<br>2.5 | 5.5<br>4.0                                       | 8.0<br>6.0    | 1.0        | 10.5<br>8.0             | 2.5<br>2.0       | 9.0<br>7.0  | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $\overline{I}_{A} = B$ to $\overline{O}_{A} = B$ | 3.3<br>5.0        | 3.0<br>2.0 | 5.5<br>4.0                                       | 8.0<br>6.0    | 1.0<br>1.5 | 10.5<br>8.0             | 2.5<br>2.0       | 9.0<br>7.0  | ns    | 2-3, 4      |

<sup>\*</sup>Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

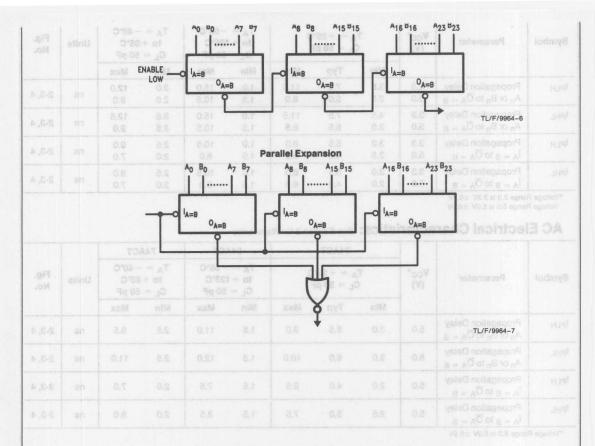
#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |  |                   |     | 74ACT  | NOR OTHER CHIEFLES | 54   | ACT                     | 74/  | ACT  |       |             |
|------------------|--|-------------------|-----|--|--------------------|------|-------------------------|--|------|-------|-------------|
| Symbol           | Parameter  | V <sub>CC</sub> * |     | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |                    | to + | -55°C<br>125°C<br>50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.<br>No. |
|                  |  |                   | Min | Тур  | Max                | Min  | Max                     | Min  | Max  |       |             |
| t <sub>PLH</sub> | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$           | 5.0               | 3.0 | 5.5  | 9.0                | 1.5  | 11.0                    | 2.5  | 9.5  | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $A_n$ or $B_n$ to $\overline{O}_A = B$           | 5.0               | 3.0 | 6.0  | 10.0               | 1.5  | 12.0                    | 2.5  | 11.0 | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay $\overline{I}_{A = B}$ to $\overline{O}_{A = B}$ | 5.0               | 2.0 | 4.0  | 6.5                | 1.5  | 7.5                     | 2.0  | 7.0  | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay $\overline{I}_A = B$ to $\overline{O}_A = B$     | 5.0               | 2.5 | 5.0  | 7.5                | 1.5  | 8.5                     | 2.0  | 8.0  | ns    | 2-3, 4      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### Capacitance

| Symbol          | Parameter                     | Тур | Units | Conditions      |
|-----------------|-------------------------------|-----|-------|-----------------|
| CIN             | Input Capacitance             | 4.5 | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 40  | pF    | $V_{CC} = 5.0V$ |



| V <sub>OC</sub> = 5.0V |  |  |
|------------------------|--|--|
|                        |  |  |

#### **General Description**

The 'ACT534 is a high-speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The 'ACT534 is the same as the 'ACT374 except that the outputs are inverted.

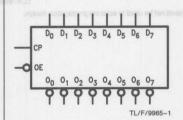
#### **Features**

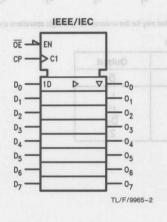
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT534 has TTL-compatible inputs
- Inverted output version of 'ACT374

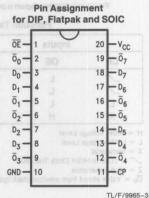
Ordering Code: See Section 8

**Logic Symbols** 

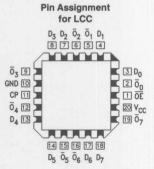
#### **Connection Diagrams**







| Pin Names                         | Description                     |
|-----------------------------------|---------------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                     |
| CP                                | Clock Pulse Input               |
| ŌĒ                                | TRI-STATE Output Enable Input   |
| $\overline{O}_0 - \overline{O}_7$ | Complementary TRI-STATE Outputs |



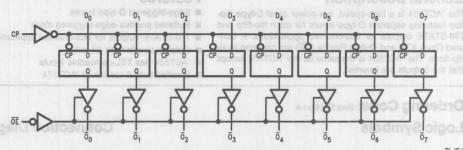
TL/F/9965-4

#### **Functional Description**

The 'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) Octal D File-Flop with TRI-STATE

transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the

#### **Logic Diagram**



TL/F/9965-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Function Table**

| 20 - Voc | Inputs |      |   | Output |
|----------|--------|------|---|--------|
| CP       | OE S   | h 00 | D | ō      |
| 1        | L      | - 0G | Н | .o.L   |
| 1        | L      |      | L | Н      |
| 30 L 31  | L o    |      | X | Ōo     |
| X        | H. 8   |      | X | Z      |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Clock Transition

Z = High Impedance

O0 = Value stored from previous clock cycle

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

-0.5V to +7.0V ACT Supply Voltage (V<sub>CC</sub>) DC Input Diode Current (IIK)  $V_1 = -0.5V$ -20 mA  $V_I = V_{CC} + 0.5V$ +20 mA DC Input Voltage (Vi) -0.5V to V<sub>CC</sub> + 0.5V DC Output Diode Current (IOK)

-20 mA  $V_0 = -0.5V$ +20 mA  $V_0 = V_{CC} + 0.5V$ DC Output Voltage (Vo) -0.5V to to  $V_{CC} + 0.5V$ 

DC Output Source ±50 mA or Sink Current (Io)

DC V<sub>CC</sub> or Ground Current

±50 mA per Output Pin (ICC or IGND) -65°C to +150°C Storage Temperature (TSTG) Junction Temperature (T<sub>J</sub>) CDIP 175°C PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating Conditions

Supply Voltage (VCC) 2.0V to 6.0V 'AC 4.5V to 5.5V Input Voltage (V<sub>I</sub>) OV to Vcc Output Voltage (Vo) Operating Temperature (TA)

74AC/ACT -40°C to +85°C 54AC/ACT 100000 - 55°C to + 125°C Minimum Input Edge Rate (ΔV/Δt)

'AC Devices VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

Minimum Input Edge Rate (ΔV/Δt)

ACT Devices
V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

#### **DC Characteristics for 'ACT Family Devices**

|                 | 80                  |  |                     |                        | 744            | CT           | 54ACT                       | 0.0         | 74ACT VALUE                     | ation D     | IPHIL Propa   |
|-----------------|---------------------|--|---------------------|------------------------|----------------|--------------|-----------------------------|-------------|---------------------------------|-------------|---|
| Symbol          | en                  | Parameter                                    |                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> | =<br>5°C     | T <sub>A</sub> = -55°C to + | 125°C       | T <sub>A</sub> = -40°C to +85°C | Units       | Conditions  |
|                 | en                  |  |                     |                        | Тур            | 1.0          | Guaran                      | teed Li     | Enable                          | tezt Outpu  |   |
| PHIV<br>2-8     | Minimur<br>Input Vo | m High Level                                 | 4.5                 | 4.5<br>5.5             | 1.5            | 2.0          | 2.0                         | 1.5         | 2.0                             | V           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>IL</sub> | Maximu<br>Input Vo  | m Low Level<br>oltage                        |                     | 4.5<br>5.5             | 1.5<br>1.5     | 0.8          | 0.8<br>0.8                  |             | 0.8<br>0.8                      | Voas        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimur<br>Output \ | m High Level<br>Voltage                      |                     | 4.5<br>5.5             | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                  | - 6311      | 4.4<br>5.4                      | V           | $I_{OUT} = -50 \mu\text{A}$   |
| Fig.            | allaU               | $T_A = -40^{\circ}C$ to +85°C $C_L = 60  pF$ | 59°C<br>5°C<br>0 pF | 4.5<br>5.5             | T              | 3.86<br>4.86 | 3.70<br>4.70                | Voo"<br>(V) | 3.76 4.76                       | ned V       | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$  |
| VOL             | Maximu<br>Output \  | m Low Level<br>/oltage                       | init# be            | 4.5<br>5.5             | 0.001<br>0.001 | 0.1          | 0.1<br>0.1                  | 0.3         | 0.1<br>WC0.1 <sub>0</sub> HOJH  | V<br>anii q | I <sub>OUT</sub> = 50 μA  |
| 2-7             | en                  | 1.6  |                     | 4.5<br>5.5             |                | 0.36<br>0.36 | 0.50                        | 5.0         | 0.44 HOLH<br>0.44               | Tye         | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| IIN             | Maximu              | m Input Leakage C                            | Current             | 5.5                    |                | ±0.1         | ± 1.0                       | 5.0         | ±1.0                            | μΑ          | $V_1 = V_{CC}$ , GND  |
| loz             | Maximu<br>Current   | m TRI-STATE®                                 |                     | 5.5                    |                | ±0.5         | ±10.0                       |             | ±5.0 va.o                       | μΑ          | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |
| ГССТ            | Maximul             |  |                     | 5.5                    | 0.6            |              | 1.6                         |             | 1.5                             | mA          | $V_I = V_{CC} - 2.1V$   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'ACT Family Devices (Continued) 11888 THE TRANSPORT OF THE PROPERTY OF

|        |                                     |                        | 74ACT<br>T <sub>A</sub> =<br>+ 25°C |        | 00                                | 54ACT        | 74ACT                           | talf of    | n Mariary/Aaroap                         |
|--------|-------------------------------------|------------------------|-------------------------------------|--------|-----------------------------------|--------------|---------------------------------|------------|--|
| Symbol | OS Parameter                        | V <sub>CC</sub><br>(V) |                                     |        | T <sub>A</sub> = -55°C to + 125°C |              | T <sub>A</sub> = -40°C to +85°C | Units      | Conditions                               |
|        | DOV of VD                           |                        | Тур                                 | Voltag | Guaranteed                        |              | Limits                          | (Mil) Iner |  |
| IOLD   | †Minimum Dynamic                    | 5.5                    | oV) egs                             | HoV tu | ghiO                              | 50 Am 02 +   | 75                              | mA         | V <sub>OLD</sub> = 1.65V Max             |
| IOHD   | Output Current                      | 5.5                    | aregme<br>T                         | ACKAC  | Oper<br>74                        | -5000 + 0    | VorVaA75                        | mA (       | V <sub>OHD</sub> = 3.85V Min             |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | T<br>out Edg                        | 8.0    | se<br>tiniM                       | 160.0 - 00 - | 80.0                            | μΑ         | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for waveforms

|                  | 12  |                          | 4.5V, 5.5V | 74ACT  | 0.09         | 1+05 | 4ACT   | 74   | ACT                    | qmeT eş                   | Store                |
|------------------|---|--------------------------|------------|--|--------------|------|--|------|------------------------|---------------------------|----------------------|
| Symbol           | Parameter   | V <sub>CC</sub> *<br>(V) |            | C <sub>L</sub> = +25°C<br>C <sub>L</sub> = 50 pF | orar<br>orar | to - | - 55°C<br>- 125°C<br>= 50 pF                           | to + | -40°C<br>85°C<br>50 pF | Units                     | Fig.                 |
|                  |   |                          | Min        | Тур  | Max          | Min  | Max  | Min  | Max                    | Philosophia<br>Rivide may | bedini               |
| f <sub>max</sub> | Maximum Clock<br>Frequency                        | 5.0                      |            | 100  | - Nigh       | 85   | s reteble over 1<br>olos, National o<br>detabook spect | 120  |                        | MHz                       | risqual<br>a briseri |
| t <sub>PLH</sub> | Propagation Delay CP to $\overline{\mathbb{Q}}_n$ | 5.0                      | 2.5        | 6.5  | 11.5         | 1.0  | 14.0   | 2.0  | 12.5                   | ns                        | 2-3, 4               |
| t <sub>PHL</sub> | Propagation Delay CP to Qn                        | 5.0                      | 2.0        | 6.0  | 10.5         | 1.0  | 13.0   | 2.0  | 12.0                   | ns                        | 2-3, 4               |
| t <sub>PZH</sub> | Output Enable Time                                | 5.0                      | 2.5        | 6.5  | 12.0         | 1.0  | 14.0   | 2.0  | 12.5                   | ns                        | 2-5                  |
| t <sub>PZL</sub> | Output Enable Time                                | 5.0                      | 2.0        | 6.0  | 11.0         | 1.0  | 13.0   | 2.0  | 11.5                   | ns                        | 2-6                  |
| t <sub>PHZ</sub> | Output Disable Time                               | 5.0                      | 1.5        | 7.0  | 12.5         | 1.0  | 14.5   | 1.0  | 13.5                   | ns                        | 2-5                  |
| t <sub>PLZ</sub> | Output Disable Time                               | 5.0                      | 1.5        | 5.5  | 10.5         | 1.0  | 11.5   | 1.0  | 10.5                   | ns                        | 2-6                  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for waveforms

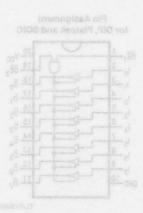
|                 |                                    |                |                   | 4.8 74 | ACT             | 54ACT   | 74ACT  | Output |             |
|-----------------|------------------------------------|----------------|-------------------|--------|-----------------|---|--|--------|-------------|
| Symbol          | HOI Par                            | rameter as g   | V <sub>CC</sub> * |        | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units  | Fig.<br>No. |
| Au De =         | tuol .                             | 1.0            |                   | Тур    | 1.0             | Guaranteed Min  | imum suca i vica i m   | UmixaM | w.V         |
| t <sub>s</sub>  | Setup Time<br>D <sub>n</sub> to CP | e, HIGH or LOW | 5.0               | 1.0    | 3.5             | 5.0   | 4.0 spello   | ns     | 2-7         |
| Ath 48<br>Am 48 | Hold Time,<br>D <sub>n</sub> to CP | HIGH or LOW    | 5.0               | 03.0   | 1.0             | 3.0   | 1.5  | ns     | 2-7         |
| tw 10 .00V      | CP Pulse W                         |                | 5.0               | 2.0    | 3.5             | 5.0   | 3.5  | ns     | 2-3         |

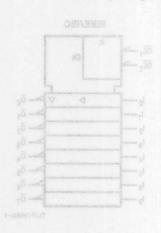
<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

#### Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40.0 | pF    | V <sub>CC</sub> = 5.0V |







|  | H |
|--|---|
|  |   |
|  |   |

# 54AC/74AC540 Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'AC540 is an octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers.

These devices are similar in function to the 'AC240 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

#### **Features**

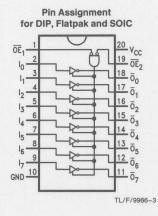
- TRI-STATE inverting outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA

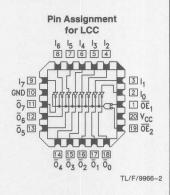
#### Ordering Code: See Section 8

#### **Logic Symbol**

## 

#### **Connection Diagrams**





#### **Truth Table**

|                 | Inputs          | Outputs |         |
|-----------------|-----------------|---------|---------|
| OE <sub>1</sub> | OE <sub>2</sub> | -1      | Outputs |
| L               | L               | Н       | L       |
| Н               | X               | X       | Z       |
| X               | Н               | X       | Z       |
| L               | L               | L       | Н       |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance

| -U.5V tO + 1.UV                    | 'ACT 4.5V to 5.5V  |
|------------------------------------|--|
|                                    | Input Voltage (V <sub>I</sub> ) 0V to V <sub>CC</sub>  |
| -20 mA                             | Output Voltage (Vo)  |
| $-0.5V$ to $V_{CC} + 0.5V$         | Operating Temperature (T <sub>A</sub> ) 74AC/ACT -40°C to +85°C  |
|                                    | 54AC/ACT —55°C to +125°C   |
| -20 mA<br>+20 mA                   | Minimum Input Edge Rate (ΔV/Δt) 'AC Devices  |
| -0.5V to to V <sub>CC</sub> + 0.5V | V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub>   |
|                                    | V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns   |
| ± 50 mA                            | Minimum Input Edge Rate (ΔV/Δt)  |
|                                    | 'ACT Devices The belances there no ablode and the beland abundant A"   |
| ±50 mA                             | V <sub>IN</sub> from 0.8V to 2.0V happened and an 0.5 nothing test mumbered?   |
| -65°C to +150°C                    | V <sub>CC</sub> @ 4.5V, 5.5V   |
|                                    |  |
| 175°C<br>140°C                     | AC Electrical Characteristics: See Section   |
|                                    | -20 mA<br>+20 mA<br>-0.5V to V <sub>CC</sub> + 0.5V<br>-20 mA<br>+20 mA<br>-0.5V to to V <sub>CC</sub> + 0.5V<br>±50 mA<br>-65°C to +150°C |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### DC Characteristics for 'AC Family Devices

|                 | en 6.0                              |                        | 74                      | AC                   | 54AC                              | 74AC                            | sion Delet                                    | PLH Propaga  |
|-----------------|-------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|---|--|
| Symbol          | Parameter 0.1                       | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units   | Conditions   |
|                 | 2.5 12.0                            |                        | Тур                     | 1.0                  | Guaranteed L                      | imits 88                        | Talden  | Output F   |
| VIH             | Minimum High Level                  | 3.0                    | 011.5                   | 2.1                  | 8 2.18.8                          | 0.5 2.13                        |   | $V_{OUT} = 0.1V$   |
|                 | Input Voltage                       | 4.5<br>5.5             | 2.25                    | 3.15                 | 3.15                              | 3.15<br>3.85                    | it eVien                                      | or V <sub>CC</sub> - 0.1V  |
| VIL             | Maximum Low Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9 0.9 1.35<br>1.65              | 0.9<br>1.35<br>1.65             | Nsable Til                                    | $V_{OUT} = 0.1V_{OUT}$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub> | Minimum High Level                  | 3.0                    | 2.99                    | 2.9                  | 2.90                              | 2.9                             |   | $I_{OUT} = -50 \mu A$  |
| Output Voltage  | 4.5<br>5.5                          | 4.49<br>5.49           | 4.4<br>5.4              | 4.4<br>5.4           | 4.4<br>5.4                        | VS.0 V VS.E                     | *Voltage Range 3.8 is<br>Voltage Range 5.0 is |  |
|                 | an                                  | 3.0                    | 6                       | 2.56                 | 2.4                               | 2.46<br>3.76                    | V   | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$               |
|                 | VO                                  | 5.5                    | V -                     | 4.86                 | 4.7                               | 4.76                            |   | -24 mA   |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | V C   | $I_{OUT} = 50 \mu A$   |
|                 |                                     | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              | 0.44<br>0.44<br>0.44            | V   | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $12 \text{ mA}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$ |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current    | 5.5                    |                         | ±0.1                 | ±1.0                              | ±1.0                            | μА  | $V_{I} = V_{CC}$ , GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) MINER MUMILIAN STUIDED A

|                      |  | 74  | AC O                         | 54AC                   | 74AC       | 18 8004<br>18 e-18 | Military/Asrosj   |  |
|----------------------|--|---|------------------------------|------------------------|------------|--------------------|-------------------|--|
| Symbol               | bol Vos Parameter Vcc (V) T <sub>A</sub> = +25°C | +25°C T <sub>A</sub> = T <sub>A</sub> =<br>-55°C to +125°C -40°C to +85°C |                              | Units                  | Conditions |                    |                   |  |
| apV atV0             | No.  | Тур   | astoV tugni                  | Guaranteed Li          | mits       | (i) Inen           | DC Input Diode Cu |  |
| lozo <sup>V</sup> of | Maximum TRI-STATE® Current                       | 5.5   | lage (Vo)<br>Temperatu<br>OT | ±0.5                   | ±10.0      | ±5.0               | μΑ                | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND |
| IOLD                 | †Minimum Dynamic                                 | 5.5   | and Edge                     | A NUMBE<br>Lesurate 33 | 50         | 75                 | mA                | V <sub>OLD</sub> = 1.65V Max   |
| I <sub>OHD</sub>     | Output Current                                   | 5.5   | 2001                         | AC Dev                 | -50        | -75                | mA                | V <sub>OHD</sub> = 3.85V Min   |
| Icc Var              | Maximum Quiescent<br>Supply Current              | 5.5   | 30% to 7                     | 8.0                    | 160.0      | 80.0               | μА                | V <sub>IN</sub> = V <sub>CC</sub><br>or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |                                     |                       |            | 74AC                   | 54AC  | 74AC   | n etvloedA | Note fo     |
|------------------|-------------------------------------|-----------------------|------------|------------------------|---|--|------------|-------------|
| Symbol           | Parameter                           | V <sub>CC</sub> * (V) |            | C <sub>L</sub> = +25°C | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 \text{ pF}$ | Units      | Fig.<br>No. |
|                  |                                     |                       | Min        | Тур Мах                | Min Max   | Min Max  | Chara      |             |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0            | 1.5<br>1.5 | 5.5 7.5<br>4.0 6.0     | 1.0 9.0<br>1.0 7.0  | 1.0 8.0<br>1.0 6.5   | ns         | 2-3, 4      |
| tpHLnolf         | Propagation Delay<br>Data to Output | 3.3<br>5.0            | 1.5        | 5.0 7.0<br>4.0 5.5     | 1.0 8.0<br>1.0 6.5  | 1.0 7.5<br>1.0 6.0   | ns         | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time                  | 3.3<br>5.0            | 3.0<br>2.0 | 8.5 11.0<br>6.5 8.5    | 1.0 13.0<br>1.0 10.0  | 2.5 12.0<br>2.0 9.5  | ns         | 2-5         |
| t <sub>PZL</sub> | Output Enable Time                  | 3.3<br>5.0            | 2.5<br>2.0 | 7.5 10.0<br>6.0 7.5    | 1.0 12.0<br>1.0 9.0   | 2.0 11.0<br>1.5 8.5  | ns         | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                 | 3.3<br>5.0            | 2.5<br>1.5 | 8.5 13.0<br>7.5 10.5   | 1.0 15.5<br>1.0 12.0  | 1.5 14.0<br>1.0 11.0   | ns         | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time                 | 3.3<br>5.0            | 2.5<br>1.5 | 7.0 10.0<br>6.0 8.0    | 1.0 12.0<br>1.0 10.0  | 2.0 11.0<br>1.5 9.0  | ns         | 2-6         |

<sup>\*</sup>Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

#### Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 30.0 | pF o  | V <sub>CC</sub> = 5.0V |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# 54AC/74AC541 Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'AC541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The 'AC541 is a noninverting option of the 'AC540.

This device is similar in function to the 'AC244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

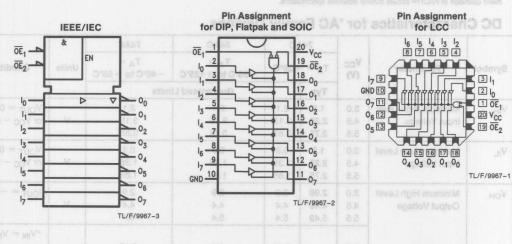
#### **Features**

- TRI-STATE outputs
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors
- Output source/sink 24 mA
- 'AC540 provides inverted outputs | memuO ani2 to
- Standard Military Drawing (SMD)

Ordering Code: See Section 8

#### **Logic Symbol**

#### **Connection Diagrams**



#### **Truth Table**

|                 | Inputs          | 4.76   | Outputs |  |  |
|-----------------|-----------------|--------|---------|--|--|
| OE <sub>1</sub> | OE <sub>2</sub> | 0.1    | Cutputs |  |  |
| L               | L               | н      | H       |  |  |
| H               | X               | X      | Z       |  |  |
| X               | Н               | X      | Z       |  |  |
| L               | L               | 34.0 L | 0.50    |  |  |

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

Z = High Impedance

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )  | -0.5V to $+7.0$ V                                    |
|--|--|
| DC Input Diode Current (I <sub>IK</sub> )                                      | -20 mA   |
| $V_{I} = -0.5V$ $V_{I} = V_{CC} + 0.5V$  | + 20 mA  |
| DC Input Voltage (V <sub>I</sub> )   | $-0.5$ V to $V_{CC} + 0.5$ V                         |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$ | atugua 3TA 12 20 mA<br>20 mA<br>20 mA                |
|  | $-0.5$ V to to $V_{CC} + 0.5$ V                      |
| Do output oouloo   | W Output source/sink 24<br>Am 02 £540 provides inver |
|  | M Standard Military Draw<br>Am 06±AC641: 6962-8870   |

Junction Temperature (T<sub>J</sub>)
CDIP 175°C
PDIP 140°C

Storage Temperature (TSTG)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> )       |                       |
|---|-----------------------|
| 'AC                                     | 2.0V to 6.0V          |
| 'ACT                                    | 4.5V to 5.5V          |
| Input Voltage (V <sub>I</sub> )         | 0V to V <sub>CC</sub> |
| Output Voltage (V <sub>O</sub> )        | 0V to V <sub>CC</sub> |
| Operating Temperature (T <sub>A</sub> ) |                       |
| 74AC/ACT                                | -40°C to +85°C        |
| 54AC/ACT                                | -55°C to +125°C       |
|   |                       |
| VIN 110111 30 % to 70 % 01 V(:):        |                       |
| V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V      | 125 mV/ns             |
|   |                       |
|   |                       |
| Vcc @ 4.5V .5.5V                        | 125 mV/ns             |

#### DC Characteristics for 'AC Family Devices

-65°C to +150°C

|                 | s s a a a                            |                               | 74AC                    |                       | 54AC                             | 74AC                            | 1 4        | Conditions  |  |
|-----------------|--------------------------------------|-------------------------------|-------------------------|-----------------------|----------------------------------|---------------------------------|------------|---|--|
| Symbol          | Parameter                            | Parameter V <sub>CC</sub> (V) |                         | + 25°C                | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units      |   |  |
|                 | Managan E Old                        | 40                            | Тур                     | Typ Guaranteed Limits |                                  |                                 |            |   |  |
| VIH             | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5             | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85   | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | V          | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5             | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65   | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | ٧          | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5             | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4     | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | V          | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 |                                      | 3.0<br>4.5<br>5.5             |                         | 2.56<br>3.86<br>4.86  | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | <b>V</b>   | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>-12 mA<br>I <sub>OH</sub> -24 mA<br>-24 mA |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5             | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1     | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V          | Ι <sub>ΟUT</sub> = 50 μΑ  |  |
|                 |                                      | 3.0<br>4.5<br>5.5             |                         | 0.36<br>0.36<br>0.36  | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | leve Legal | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA                                    |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                           |                         | ±0.1                  | ±1.0                             | ±1.0                            | μА         | $V_I = V_{CC}$ , GND  |  |

†Maximum test duration 2.0 ms, one output loaded at a time.

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

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#### DC Characteristics for 'AC Family Devices (Continued)

|                  |                                       |                        | 74AC<br>T <sub>A</sub> = +25°C |          | 54AC                             | 74AC                            | Units | Conditions   |  |
|------------------|---------------------------------------|------------------------|--------------------------------|----------|----------------------------------|---------------------------------|-------|--|--|
| Symbol           | Parameter                             | V <sub>CC</sub><br>(V) |                                |          | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C |       |  |  |
|                  |                                       | V                      | Тур                            |          | Guaranteed Limits                |                                 |       | PANIDAPO   |  |
| loz              | Maximum TRI-STATE®<br>Leakage Current | 5.5                    |                                | ±0.5     | ±10.0                            | ±5.0                            | μΑ    | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I} = V_{CC}$ , GND<br>$V_{O} = V_{CC}$ , GND |  |
| I <sub>OLD</sub> | †Minimum Dynamic                      | 5.5                    | to stucti                      | o bns    | tuant \$ 50 mag bers             | ited diw75 tal lateo            | mA    | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD             | Output Current                        | 5.5                    | to oc. oc. b                   | moi se l | -50                              | 75 enemo                        | mA    | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc              | Maximum Quiescent Supply Current      | 5.5                    | labitnet                       | 8.0      | 'ACTS70.001 Fund                 | ert of le 80.0 bi vitan         | μΑ    | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  | Parameter                           |                   |  |            | 74AC   |            | 54AC   |            | 74AC         |      |        |  |
|------------------|-------------------------------------|-------------------|--|------------|--|------------|--|------------|--------------|------|--------|--|
| Symbol           |                                     | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |            | Units        | Fig. |        |  |
|                  | 20 -Ver                             | 1 -30             | Min  | Тур        | Max  | Min        | 33 Max   | Min        | Max          |      |        |  |
| t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 2.0<br>1.5                                       | 5.5<br>4.0 | 8.0<br>6.0   | 1.0        | 10.0<br>7.0  | 1.5<br>1.0 | 9.0<br>6.5   | ns   | 2-3, 4 |  |
| t <sub>PHL</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0        | 2.0<br>1.5                                       | 5.5<br>4.0 | 8.0<br>6.0   | 1.0        | 9.5<br>7.0   | 1.5<br>1.0 | 8.5<br>6.5   | ns   | 2-3, 4 |  |
| t <sub>PZH</sub> | Output Enable Time                  | 3.3<br>5.0        | 3.0<br>2.0                                       | 8.0<br>6.0 | 11.5<br>8.5  | 1.0        | 13.5<br>10.0   | 3.0<br>1.5 | 12.5<br>9.5  | ns   | 2-5    |  |
| t <sub>PZL</sub> | Output Enable Time                  | 3.3<br>5.0        | 2.5<br>1.5                                       | 7.0<br>5.5 | 10.0<br>7.5  | 1.0        | 12.5<br>9.0  | 2.5<br>1.0 | 11.5<br>8.5  | ns   | 2-6    |  |
| t <sub>PHZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 3.5  | 9.0<br>7.0 | 12.5<br>9.5  | 1.0<br>1.0 | 15.0<br>12.0   | 2.5<br>1.0 | 14.0<br>10.5 | ns   | 2-5    |  |
| t <sub>PLZ</sub> | Output Disable Time                 | 3.3<br>5.0        | 2.5<br>2.0                                       | 6.5<br>5.5 | 9.5<br>7.5   | 1.0        | 11.0<br>9.0  | 2.0<br>1.0 | 10.5<br>8.5  | ns   | 2-6    |  |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

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#### Capacitance 2 2 2 2

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 30.0 | pF    | V <sub>CC</sub> = 5.0V |

# 54ACT/74ACT563 Octal Latch with TRI-STATE® Outputs

#### **General Description**

The 'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

The 'ACT563 device is functionally identical to the 'ACT573, but with inverted outputs.

#### **Features**

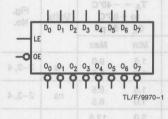
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT573 but with inverted outputs
- Outputs source/sink 24 mA
- 'ACT563 has TTL-compatible inputs

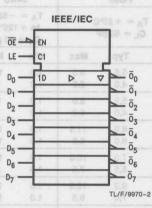
Ordering Code: See Section 8

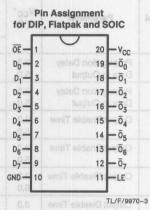
**Logic Symbols** 

#### **Connection Diagrams**

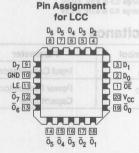
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| Pin Names                         | Description                   |
|-----------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                   |
| LE                                | Latch Enable Input            |
| ŌĒ                                | TRI-STATE Output Enable Input |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Latch Outputs       |



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onango stato caon umo no o mput changes, venen LL is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are in the bi-state mode. When OE is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

| Н      | Н | L       | Н   | (art) Zamu  | High-Z      |
|--------|---|---------|-----|-------------|-------------|
| H      | H | Н       | L   | Z           | High-Z      |
| H      | L | X       | NC  | Z           | Latched     |
| ASTO 4 | H | at Ya.p | Н   | H (M)       | Transparent |
| L      | Н | Н       | L 6 | Current (ig | Transparent |
| Antos  | L | X       | NC  | NC          | Latched     |

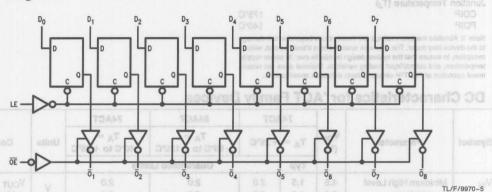
H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| $V_{OUT} = 0.1V$ or $V_{OO} - 0.1V$  |   | 8.0<br>8.0 |     |              | Maximum Low Level<br>Input Voltage |     |
|--|---|------------|-----|--------------|------------------------------------|-----|
|  | ٧ |            |     | 4,49<br>5.49 |                                    |     |
| "V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> -24 mA loH -24 mA                            | ٧ |            |     |              |                                    |     |
|  |   |            | 0.1 |              |                                    | JoV |
| $^{o}V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{i}V_{IL} = 24 \text{ mA}$ $^{i}V_{IL} = 24 \text{ mA}$ |   |            |     |              |                                    |     |
|  |   |            |     |              |                                    |     |
|  |   |            |     |              |                                    |     |
|  |   | 8.1        |     |              |                                    |     |

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply voltage (VCC)                      |   | -0.5V to +7.0V                     |
|---|---|------------------------------------|
| DC Input Diode Current (I <sub>IK</sub> ) |   |                                    |
| $V_1 = -0.5V$                             |   | -20 mA                             |
| $V_I = V_{CC} + 0.5V$                     |   | + 20 mA                            |
| DC Input Voltage (V <sub>I</sub> )        |   | $-0.5V$ to $V_{CC} + 0.5V$         |
| DC Output Diode Current (IOK)             |   |                                    |
| $V_{O} = -0.5V$                           |   | -20 mA                             |
| $V_O = V_{CC} + 0.5V$                     |   | + 20 mA                            |
| DC Output Voltage (V <sub>O</sub> )       | _ | -0.5V to to V <sub>CC</sub> + 0.5V |
|   |   |                                    |

DC Output Voltage (V<sub>O</sub>) = 0.5V to to V<sub>CC</sub> + 0.5V

DC Output Source
or Sink Current (I<sub>O</sub>) ± 50 mA

DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±50 mA
Storage Temperature (T<sub>STG</sub>) -65°C to +150°C

Junction Temperature (TJ)
CDIP
PDIP
175°C
140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Recommended Operating

| Conditions   |   |
|--|---|
| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT   | 2.0V to 6.0V  |
| Input Voltage (V <sub>I</sub> )  |   |
| Output Voltage (V <sub>O</sub> )   | emil quies s a 0V to V <sub>CC</sub>                            |
| Operating Temperature (T <sub>A</sub> ) 74AC/ACT 54AC/ACT  | -40°C to +85°C<br>-55°C to +125°C                               |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'AC Devices V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> $V_{CC}$ @ 3.3V, 4.5V, 5.5V | nom eonsbegmi ngirt ent<br>in dini alab wen pineme<br>125 mV/ns |
| Minimum Input Edge Rate $(\Delta V/\Delta t)$<br>'ACT Devices<br>$V_{IN}$ from 0.8V to 2.0V<br>$V_{CC}$ @ 4.5V, 5.5V                       | 125 mV/ns   |
|  | · 医克尔氏病 医高性原生性 (10) (10) (10) (10)                              |

#### **DC Characteristics for 'ACT Family Devices**

|                 |                                      |                        | 74               | ACT                        | 54ACT                             | 74ACT                           |       |   |  |
|-----------------|--------------------------------------|------------------------|------------------|----------------------------|-----------------------------------|---------------------------------|-------|---|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C                     | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |  |
|                 | - Sancer and residence               |                        | Тур              | aritari (filozofiki alaski | Guaranteed Li                     | mits                            | -     | 3 30  |  |
| VIH             | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0                 | 2.0<br>2.0                        | 2.0<br>2.0                      | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5       | 0.8<br>0.8                 | 0.8<br>0.8                        | 0.8<br>0.8                      | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4                 | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧     | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 |                                      | 4.5<br>5.5             |                  | 3.86<br>4.86               | 3.70<br>4.70                      | 3.76<br>4.76                    | V     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1                 | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧     | I <sub>OUT</sub> = 50 μA  |  |
|                 |                                      | 4.5<br>5.5             |                  | 0.36<br>0.36               | 0.50<br>0.50                      | 0.44<br>0.44                    | v     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1                       | ±1.0                              | ±1.0                            | μА    | $V_{I} = V_{CC}$ , GND  |  |
| loz             | Maximum TRI-STATE® Current           | 5.5                    |                  | ±0.5                       | ±10.0                             | ±5.0                            | μА    | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| ICCT            | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |                            | 1.6                               | 1.5                             | mA    | $V_I = V_{CC} - 2.1V$   |  |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

#### A

### DC Characteristics for 'ACT Family Devices (Continued)

|                  | 8                                   | notition        | TA = +25°C |     | 54ACT                                  | 74ACT                           |       | Conditions                               |  |
|------------------|-------------------------------------|-----------------|------------|-----|--|---------------------------------|-------|--|--|
| Symbol           | Parameter                           | V <sub>CC</sub> |            |     | T <sub>A</sub> = 5<br>-55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units |  |  |
|                  |                                     |                 | Тур        | Fq  | Guaranteed Li                          | mits sonations                  | sO    |  |  |
| lold             | †Minimum Dynamic                    | 5.5             |            |     | 50                                     | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max             |  |
| I <sub>OHD</sub> | Output Current                      | 5.5             |            |     | -50                                    | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5             |            | 8.0 | 160.0                                  | 80.0                            | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |  |                   |  | 74ACT |      | 54/   | ACT  | 74   | ACT  |       |             |
|------------------|--|-------------------|--|-------|------|---|------|--|------|-------|-------------|
| Symbol           | Parameter  | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |      | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |      | Units | Fig.<br>No. |
|                  |  |                   | Min  | Тур   | Max  | Min   | Max  | Min  | Max  |       |             |
| t <sub>PLH</sub> | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | 5.0               | 3.0  | 7.0   | 11.5 | 1.0   | 14.5 | 2.5  | 12.5 | ns    | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | 5.0               | 3.0  | 6.0   | 10.0 | 1.0   | 12.0 | 2.5  | 11.0 | ns    | 2-3,4       |
| <sup>t</sup> PLH | Propagation Delay<br>LE to On                      | 5.0               | 3.0  | 6.5   | 10.5 | 1.0   | 12.5 | 2.5  | 11.5 | ns    | 2-3,4       |
| t <sub>PHL</sub> | Propagation Delay<br>LE to On                      | 5.0               | 2.5  | 5.5   | 9.5  | 1.0   | 11.5 | 2.0  | 10.5 | ns    | 2-3,4       |
| t <sub>PZH</sub> | Output Enable Time                                 | 5.0               | 2.5  | 5.5   | 9.0  | 1.0   | 11.5 | 2.0  | 10.0 | ns    | 2-5         |
| t <sub>PZL</sub> | Output Enable Time                                 | 5.0               | 2.0  | 5.5   | 8.5  | 1.0   | 11.0 | 2.0  | 9.5  | ns    | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                                | 5.0               | 3.5  | 6.5   | 10.5 | 1.0   | 12.0 | 2.5  | 11.5 | ns    | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time                                | 5.0               | 2.0  | 4.5   | 8.0  | 1.0   | 9.5  | 1.0  | 8.5  | ns    | 2-6         |

\*Voltage Range 5.0 is 5.0V ±0.5V

#### AC Operating Requirements: See Section 2 for Waveforms

|                |   |                          | 74A                               | CT  | 54ACT   | 74ACT  | Units | Fig.<br>No. |
|----------------|---|--------------------------|-----------------------------------|-----|---|--|-------|-------------|
| Symbol         | Parameter                                       | V <sub>CC</sub> *<br>(V) | T <sub>A</sub> = C <sub>L</sub> = |     | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |       |             |
|                |   |                          | Тур                               |     | Guaranteed Mini   | mum  |       |             |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0                      | 1.5                               | 4.0 | 4.5   | 4.5  | ns    | 2-7         |
| th             | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 5.0                      | -2.0                              | 0   | 1.5   | 0  | ns    | 2-7         |
| t <sub>w</sub> | LE Pulse Width, HIGH                            | 5.0                      | 2.0                               | 3.0 | 5.0   | 3.0  | ns    | 2-3         |

\*Voltage Range 5.0 is 5.0V ±0.5V

#### Capacitance

| Symbol          | Parameter Input Capacitance |                              | Тур    | Units To | Con             | dition | s                |  |
|-----------------|-----------------------------|------------------------------|--------|----------|-----------------|--------|------------------|--|
| CIN             |                             |                              | 4.5 AT | pF       | Vcc             | = 5.0  | Parameter        |  |
| C <sub>PD</sub> |                             | ver Dissipation<br>pacitance | 50.0   | pF       | $V_{CC} = 5.0V$ |        |                  |  |
|                 |                             |                              |        |          |                 | 5.5    | †Minimum Dynamic |  |
|                 |                             |                              |        |          |                 |        |                  |  |
|                 |                             |                              |        |          |                 |        |                  |  |

All outputs loaded, threeholds on logul associated with output under test.

OSEO IN TENDET AN Incidental at OSEO IN TENANT AND ALL AND ME

Note: Ioc for SAACT @ 25°C is identical to 74ACT @ 25°C.

#### C Electrical Characteristics: See Section 2 for Waveforms

|             |   | 740 |  |     |        |     |     |      |
|-------------|---|-----|--|-----|--------|-----|-----|------|
| .gPl<br>No. | $T_A = +28^{\circ}C$ $T_A = -38^{\circ}C$ $T_A = -40^{\circ}C$ Un $(c_L = 50  pF)$ |     |  |     | Symbol |     |     |      |
|             |   |     |  |     |        |     |     |      |
| 2-8,4       |   |     |  |     |        |     |     |      |
| 2-3,4       |   |     |  |     |        |     |     |      |
|             |   |     |  |     |        |     |     |      |
|             |   |     |  |     |        | 2.5 |     |      |
|             |   |     |  |     |        |     | 5.0 |      |
|             |   |     |  | 8.5 |        |     |     | tezi |
|             |   |     |  |     |        |     |     |      |
|             |   |     |  |     |        |     |     |      |

AC Operating Requirements: see Section 2 for Wayesto

|     |  | $T_A = -66^{\circ}C$ $(\alpha + 126^{\circ}C)$ $C_L = 80 \text{ pF}$ | $Y_A = +26^{\circ}C$ $C_L = 60 \text{ pF}$ |      | Voc* |  |
|-----|--|--|--|------|------|--|
|     |  |  |  |      |      |  |
| 7-5 |  |  |  |      |      |  |
|     |  |  |  | -2.0 |      |  |
|     |  |  |  |      |      |  |



# 54ACT/74ACT564 Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'ACT564 device is functionally identical to the 'ACT574, but with inverted outputs.

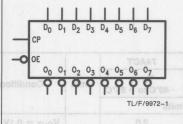
#### **Features**

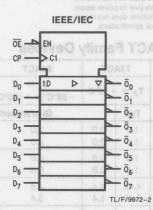
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT574 but with inverted outputs
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT564 has TTL-compatible inputs

Ordering Code: See Section 8

#### **Logic Symbols**

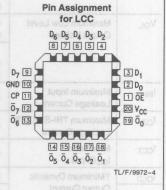
#### **Connection Diagrams**







| Pin Names                         | Description                   |
|-----------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                   |
| CP                                | Clock Pulse Input             |
| ŌĒ                                | TRI-STATE Output Enable Input |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Outputs             |



4

| Supply Voltage (V <sub>CC</sub> )  | -0.5V to +7.0V   | 'ACT   | 4.5V to 5.5V  |
|--|--|--|---|
| DC Input Diode Current ( $I_{IK}$ $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ DC Input Voltage ( $V_I$ )  DC Output Diode Current ( $I_{VO} = -0.5V$ $V_O = V_{CC} + 0.5V$ DC Output Voltage ( $V_O$ )  DC Output Source | $\begin{array}{c} -20 \text{ mA} \\ +20 \text{ mA} \\ -0.5 \text{V to V}_{CC} + 0.5 \text{V} \\ \text{OK} \\ -20 \text{ mA} \\ +20 \text{ mA} \\ -0.5 \text{V to to V}_{CC} + 0.5 \text{V} \\ \end{array}$ | Input Voltage (V <sub>I</sub> ) Output Voltage (V <sub>O</sub> ) Operating Temperature (T <sub>A</sub> ) 74AC/ACT 54AC/ACT Minimum Input Edge Rate (ΔV/Δt) 'AC Devices V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V | 0V to V <sub>CC</sub><br>0V to V <sub>CC</sub><br>0V to +85°C<br>-55°C to +125°C  |
| or Sink Current (I <sub>O</sub> )  DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GN</sub> Storage Temperature (T <sub>STG</sub>   | Silamenta: CTT and Lazerradio  | Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices V <sub>IN</sub> from 0.8V to 2.0V V <sub>CC</sub> @ 4.5V, 5.5V  | ab abotto A' art to be never artist to divide |
| Junction Temperature (T <sub>J</sub> ) CDIP  | 175°C  |  |   |

## **DC Characteristics for 'ACT Family Devices**

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT<sup>TM</sup> circuits outside databook specifications.

|                                 | 0,-2 19                            |                        | 744              | CT           | 54ACT                            | 74ACT                           |       | 3010-  |
|---------------------------------|------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|-------|--|
| Symbol                          | Parameter                          | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |
|                                 | 0 <sub>2</sub> -15 16              |                        | Тур              | add annual   | Guaranteed L                     | imits                           |       |  |
| V <sub>IH</sub> $_{a\bar{0}}$ - | Minimum High Level Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| VIL 30-                         | Maximum Low Level Input Voltage    | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8                              | 0.8<br>0.8                      | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub>                 | Minimum High Level Output Voltage  | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | ٧     | $I_{OUT} = -50 \mu\text{A}$  |
| L/F/9972-3                      | Pin Auslanment                     | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| V <sub>OL</sub>                 | Maximum Low Level Output Voltage   | 4.5<br>5.5             | 0.001            | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1<br>0.1                      | ٧     | I <sub>OUT</sub> = 50 μA   |
|                                 |                                    | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |
| IIN                             | Maximum Input<br>Leakage Current   | 5.5                    |                  | ±0.1         | ±1.0                             | ±1.0                            | μΑ    | $V_{I} = V_{CC}$ , GND   |
| loz                             | Maximum TRI-STATE® Leakage Current | 5.5                    |                  | ±0.5         | ± 10.0                           | ±5.0                            | μА    | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |
| ICCT                            | Maximum I <sub>CC</sub> /Input     | 5.5                    | 0.6              |              | 1.6                              | 1.5                             | mA    | $V_I = V_{CC} - 2.1V$  |
| IOLD                            | †Minimum Dynamic                   | 5.5                    |                  |              | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max   |
| IOHD                            | Output Current                     | 5.5                    |                  |              | -50                              | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'ACT Family Devices (Continued)

|        |                                     | lege.               | 74               | ACT    | 54ACT                            | 74ACT                           | Units | Conditions                               |
|--------|-------------------------------------|---------------------|------------------|--------|----------------------------------|---------------------------------|-------|--|
| Symbol | Parameter                           | V <sub>CC</sub> (V) | T <sub>A</sub> = | + 25°C | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C |       |  |
|        |                                     |                     | Тур              |        | Guaranteed Lin                   | nits                            |       |  |
| lcc    | Maximum Quiescent<br>Supply Current | 5.5                 |                  | 8.0    | 160.0                            | 80.0                            | μΑ    | V <sub>IN</sub> = V <sub>CC</sub> or GND |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: Icc for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics: See Section 2 for Waveforms

|                  | gnioshemi aud                             | 101 STUD          |  | 74ACT |      | 54/  | ACT     | 74ACT  |      | diuo bas | sindu       |
|------------------|---|-------------------|--|-------|------|--|---------|--|------|----------|-------------|
| Symbol           | Parameter (CMA)                           | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |         | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units    | Fig.<br>No. |
|                  |   |                   | Min  | Тур   | Max  | Min  | Max     | Min  | Max  |          |             |
| f <sub>max</sub> | Maximum Clock Frequency                   | 5.0               | 85   | 90    |      | 65   | 8 noits | 75   | Code | MHz      | bio         |
| fpLH             | Propagation Delay, CP to $\overline{O}_n$ | 5.0               | 2.0  | 6.5   | 10.5 | 1.0  | 12.5    | 1.5  | 11.5 | ns       | 2-3,4       |
| fPHL             | Propagation Delay, CP to On               | 5.0               | 1.5  | 6.0   | 9.5  | 1.0  | 11.5    | 1.5  | 10.5 | ns       | 2-3,4       |
| tpzH             | Output Enable Time                        | 5.0               | 1.5  | 5.5   | 9.0  | 1.0  | 10.5    | 1.5  | 9.5  | ns       | 2-5         |
| tPZL             | Output Enable Time                        | 5.0               | 1.5  | 5.5   | 8.5  | 1.0  | 10.5    | 1.0  | 9.5  | ns       | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time                       | 5.0               | 1.5  | 7.0   | 10.5 | 3. 1.0   | 12.5    | 1.5  | 11.5 | ns       | 2-5         |
| tpLZ             | Output Disable Time                       | 5.0               | 1.5  | 5.0   | 8.0  | 1.0  | 9.5     | 1.0  | 8.5  | ns       | 2-6         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                | 0,-16 15-0,                                     |                          | 744                               | CT              | 54ACT  | 74ACT  |       |             |
|----------------|---|--------------------------|-----------------------------------|-----------------|--|--|-------|-------------|
| Symbol         | Parameter - 3                                   | V <sub>CC</sub> *<br>(V) | T <sub>A</sub> = C <sub>L</sub> = | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units | Fig.<br>No. |
|                | 21-11 01-000                                    | 8-4                      | Тур                               |                 | Guaranteed Mini  | imum   |       |             |
| t <sub>s</sub> | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0                      | 1.0                               | 2.5             | 3.5  | 3.0  | ns    | 2-7         |
| th             | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 5.0                      | -0.5                              | 1.0             | 2.5 <sub>farqui s</sub>  | Data Inputs<br>Laufn Enabl                                 | ns    | 2-7         |
| t <sub>w</sub> | LE Pulse Width,<br>HIGH or LOW                  | 5.0                      | 2.5                               | 3.0             | 5.0  | 3.5  | ns    | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions      |
|-----------------|-------------------------------|------|-------|-----------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 50.0 | pF    | $V_{CC} = 5.0V$ |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.



## 54ACT/74ACT573 Octal Latch with TRI-STATE® Outputs

#### **General Description**

The 'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

The 'ACT573 is functionally identical to the 'ACT373 but has inputs and outputs on opposite sides.

#### **Features**

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT373
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA

TL/F/9973-2

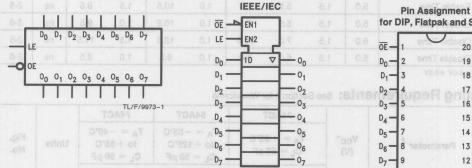
- 'ACT573 has TTL-compatible inputs
- Standard Military Drawing (SMD) - 'ACT573: 5962-87664

Ordering Code: See Section 8

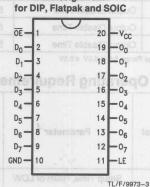
## **Logic Symbols**

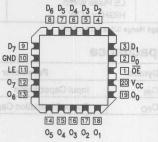
#### **Connection Diagrams**

Sym



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| TE SU                          | Latch Enable Input            |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Latch Outputs       |





Pin Assignment for LCC

TL/F/9973-4

state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{\text{OE}}$ ) input. When  $\overline{\text{OE}}$  is LOW, the buffers are enabled. When  $\overline{\text{OE}}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

| 10:3 + Lot Vo.3 | Н | H (4)       | Supply VHItage (V. |
|-----------------|---|-------------|--------------------|
| L               | Н | urent (Inc) | OC Input_Diode O   |
| CM 05           | L | X           | 00                 |
| H               | X | X           | 3.0 + 0Z = IV      |

H = HIGH Voltage

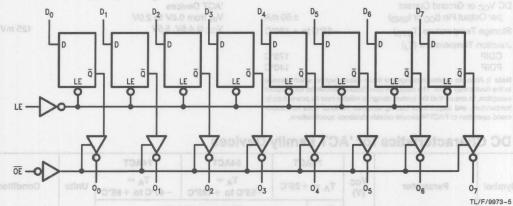
L = LOW Voltage

Z = High Impedance

X = Immaterial

O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW transition of Latch Enable

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

|  | ٧ | 6.4 |        |  |                                     |  |
|--|---|-----|--------|--|-------------------------------------|--|
| $V_{IJ} = V_{IJ} \text{ or } V_{IH}$ $V_{IJ} = V_{IJ} \text{ or } V_{IH}$ $V_{IJ} = V_{IJ} \text{ or } V_{IH}$ |   |     |        |  |                                     |  |
|  |   |     |        |  | Maximum Low Level<br>Output Voltage |  |
|  |   |     |        |  |                                     |  |
|  |   |     |        |  |                                     |  |
|  |   |     | 0.01 ± |  |                                     |  |

eximum test deration 2.0 ms, and output loaded at a time

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| -0.5V to $+7.0V$                |
|---------------------------------|
|                                 |
| -20 mA                          |
| + 20 mA                         |
| $-0.5$ V to $V_{CC} + 0.5$ V    |
| ensileV WOJ = J                 |
| -20 mA                          |
| + 20 mA                         |
| $-0.5$ V to to $V_{CC} + 0.5$ V |
|                                 |
|                                 |

or Sink Current (IO) DC V<sub>CC</sub> or Ground Current

per Output Pin (ICC or IGND) Storage Temperature (TSTG)

Junction Temperature (T<sub>J</sub>) CDIP PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>) 2.0V to 6.0V 'AC 'ACT 4.5V to 5.5V Input Voltage (V<sub>I</sub>) 0V to V<sub>CC</sub> Output Voltage (Vo) Operating Temperature (TA)

74AC/ACT — 40°C to +85°C 54AC/ACT — 55°C to +125°C Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V

125 mV/ns Minimum Input Edge Rate (ΔV/Δt)

'ACT Devices V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

## **DC Characteristics for 'ACT Family Devices**

|                 | 91 91                                | 91                     | 74             | CT           | 54ACT                             | 74ACT                           | 1          | Clo-10  |
|-----------------|--------------------------------------|------------------------|----------------|--------------|-----------------------------------|---------------------------------|------------|---|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) |                |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units      | Conditions  |
| /F/9873-6       | evalab nedapedong sizmites of        | meau edit              | Тур            | ha enoiters  | Guaranteed Li                     | imits                           | No sid tan | Please potal  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5     | 2.0<br>2.0   | 2.0<br>2.0                        | 2.0<br>2.0                      | ٧          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| VIL             | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5     | 0.8          | 0.8<br>0.8                        | 0.8<br>0.8                      | V          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧          | $I_{OUT} = -50 \mu\text{A}$   |
|                 |                                      | 4.5<br>5.5             |                | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | v          | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001 | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | V          | I <sub>OUT</sub> = 50 μA  |
|                 |                                      | 4.5<br>5.5             |                | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | v          | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                | ±0.1         | ±1.0                              | ±1.0                            | μΑ         | $V_I = V_{CC}$ , GND  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                | ±0.5         | ±10.0                             | ±5.0                            | μΑ         | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |

±50 mA

±50 mA

175°C

140°C

65°C to + 150°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'ACT Family Devices (Continued) mentuped published OA

| Symbol | TARCT                               |                        |     |     | 54ACT  T <sub>A</sub> =  -55°C to + 125°C |               |                                 | 74ACT            |       |                              |
|--------|-------------------------------------|------------------------|-----|-----|---|---------------|---------------------------------|------------------|-------|------------------------------|
|        | Parameter of                        | V <sub>CC</sub><br>(V) |     |     |   |               | T <sub>A</sub> = -40°C to +85°C |                  | Units | Conditions                   |
|        |                                     | 1 3                    | Тур | 9   |   | Guaranteed Li | mits                            |                  |       |                              |
| ICCT   | Maximum I <sub>CC</sub> /Input      | 5.5                    | 0.6 | Gua |   | 1.6           | 0.3                             | 1.5<br>WOJ 10 HE | mA    | $V_I = V_{CC} - 2.1V$        |
| IOLD   | †Minimum Dynamic                    | 5.5                    |     |     | -   | 50            | 10.50                           | 75               | mA    | V <sub>OLD</sub> = 1.65V Max |
| IOHD   | Output Current                      | 5.5                    | 0.1 |     | 0   | -50           | 6.0                             | -75 -10 H        | mA    | V <sub>OHD</sub> = 3.85V Min |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | 6.0 | 8.0 | 1.6                                       | 160.0         | 5.0                             | 80.0 HOH         | μА    | $V_{IN} = V_{CC}$ or GND     |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics: See Section 2 for Waveforms

|                  | V0.   | ê = poV           |  | 74ACT | n a  | 54/  | ACT  | 74   | ACT  | 090   |       |
|------------------|---|-------------------|--|-------|------|--|------|--|------|-------|-------|
| Symbol           | Parameter   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.  |
|                  |   |                   | Min  | Тур   | Max  | Min  | Max  | Min  | Max  |       |       |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>m</sub> to O <sub>n</sub> | 5.0               | 2.5  | 6.0   | 10.5 | 1.0  | 13.5 | 2.0  | 12.0 | ns    | 2-3,4 |
| t <sub>PHL</sub> | Propagation Delay D <sub>n</sub> to O <sub>n</sub>    | 5.0               | 2.5  | 6.0   | 10.5 | 1.0  | 13.5 | 2.0  | 12.0 | ns    | 2-3,4 |
| t <sub>PLH</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0               | 3.0  | 6.0   | 10.5 | 1.0  | 13.0 | 2.5  | 12.0 | ns    | 2-3,  |
| t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0               | 2.5  | 5.5   | 9.5  | 1.0  | 12.0 | 2.0  | 10.5 | ns    | 2-3,4 |
| t <sub>PZH</sub> | Output Enable Time                                    | 5.0               | 2.0  | 5.5   | 10.0 | 1.0  | 11.5 | 1.5  | 11.0 | ns    | 2-5   |
| t <sub>PZL</sub> | Output Enable Time                                    | 5.0               | 1.5  | 5.5   | 9.5  | 1.0  | 11.0 | 1.5  | 10.5 | ns    | 2-6   |
| t <sub>PHZ</sub> | Output Disable Time                                   | 5.0               | 2.5  | 6.5   | 11.0 | 1.0  | 13.5 | 1.5  | 12.5 | ns    | 2-5   |
| tpLZ             | Output Disable Time                                   | 5.0               | 1.5  | 5.0   | 8.5  | 1.0  | 10.5 | 1.0  | 9.5  | ns    | 2-6   |

\*Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol         | Parameter                                       | V <sub>CC</sub> * | T <sub>A</sub> = C <sub>L</sub> = |     | to + 125°C<br>C <sub>L</sub> = 50 pF | to +85°C<br>C <sub>L</sub> = 50 pF | Units    | Fig.<br>No. |  |
|----------------|---|-------------------|-----------------------------------|-----|--------------------------------------|------------------------------------|----------|-------------|--|
| Vr.S - n       | Vr. 2 2 - 1V                                    |                   | Тур                               |     | Guaranteed Min                       | imum                               | miret/   | roal        |  |
| t <sub>s</sub> | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0               | 1.5                               | 3.0 | 4.5                                  | 3.5                                | ns<br>ns | 2-7         |  |
| th// Ves.s     | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 5.0               | -1.5                              | 0   | 1.0                                  | Ourrent                            | ns       | 2-7         |  |
| tw             | LE Pulse Width, HIGH                            | 5.0               | 2.0                               | 3.5 | 5.0                                  | 4.0                                | ns       | 2-3         |  |

\*Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### Capacitance

| ou  | paorta          | 1100 |                        |                    |       |      |                          |         |                   | C in identical 1 |           |      |
|-----|-----------------|------|------------------------|--------------------|-------|------|--------------------------|---------|-------------------|------------------|-----------|------|
|     | Symbol          |      | Paran                  | neter              |       | Тур  | Units                    |         | Conditi           |                  |           |      |
|     | CIN             |      | Input Cap              | acitance           | amole | 5.0  | noise pF                 | isoli i | V <sub>CC</sub> = | 5.0V             | lectrical | ACE  |
|     | C <sub>PD</sub> | TO.  | Power Dis<br>Capacitar |                    |       | 25.0 | pF                       |         | $V_{CC} = $       | 5.0V             |           |      |
| .0H | Units           |      | + o)<br>= _(0          | + 125°C<br>= 50 pF |       |      | A = + 25°C<br>2( = 50 pF |         | Voc*              | 1016             |           |      |
|     |                 |      |                        |                    | niilä |      |                          |         |                   |                  |           |      |
|     |                 |      |                        |                    |       |      |                          |         |                   |                  |           |      |
|     |                 |      |                        |                    |       |      |                          |         |                   |                  |           |      |
|     |                 |      |                        |                    |       |      |                          |         |                   |                  |           |      |
|     | en              |      |                        |                    |       |      |                          |         |                   |                  |           |      |
|     |                 |      |                        |                    |       |      |                          |         |                   |                  |           |      |
|     |                 |      |                        |                    |       |      | 5.5                      |         |                   |                  |           |      |
|     |                 |      |                        | 13.5               |       |      |                          |         |                   |                  |           | ZHQİ |
|     |                 |      |                        |                    |       |      |                          |         |                   |                  |           |      |



# 54AC/74AC574 ◆ 54ACT/74ACT574 Octal D-Type Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ( $\overline{\text{OE}}$ ). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT574 is functionally identical to the 'AC/ 'ACT374 except for the pinouts.

#### **Features**

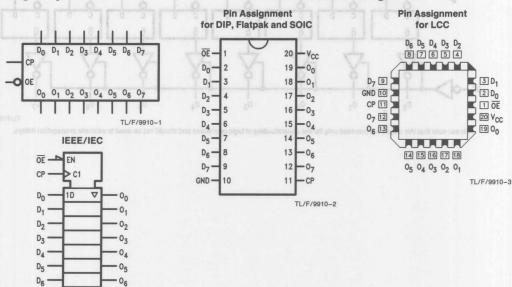
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'AC/'ACT374
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT574 has TTL-compatible inputs
- Standard Military Drawing (SMD)

- 'ACT574: 5962-89601

## Ordering Code: See Section 8

#### **Logic Symbols**

## **Connection Diagrams**



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| CP                             | Clock Pulse Input             |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Outputs             |

0<sub>7</sub>

#### **Functional Description**

The 'AC/'ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

#### **Function Table**

| [        | 1      | nputs |   | Internal  | Outputs      | Function          |
|----------|--------|-------|---|-----------|--------------|-------------------|
|          | OE     | СР    | D | Q         | ON           | runction          |
| No.      | Н      | Н     | L | NC        | Z            | Hold              |
| No.      | Н      | H     | H | NC        | Z            | Hold              |
|          | Н      | 1     | L | L         | Z            | Load              |
|          | Н      | _     | Н | H         | Z            | Load              |
|          | L      | _     | L | Form      | di idani     | Data Available    |
| -9       | I Late | 1     | H | ol bppgad | girl gHei by | Data Available    |
| THE SAME | L      | Н     | L | NC        | NC           | No Change in Data |
|          | L      | Н     | Н | NC        | NC           | No Change in Data |

H = HIGH Voltage Level

L = LOW Voltage Level

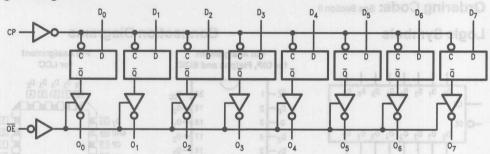
X = Immaterial

Z = High Impedance

= LOW-to-HIGH Transition

NC = No Change

#### **Logic Diagram**



TL/F/9910-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V<sub>CC</sub>) -0.5V to +7.0V DC Input Diode Current (I<sub>IK</sub>)

DC Output Diode Current ( $I_{OK}$ )  $V_O = -0.5V$  -20 mA  $V_O = V_{CC} + 0.5V$  +20 mADC Output Voltage ( $V_O$ )  $-0.5V \text{ to } V_{CC} + 0.5V$ 

DC Output Source or Sink Current (I<sub>O</sub>)

DC  $V_{CC}$  or Ground Current Per Output Pin ( $I_{CC}$  or  $I_{GND}$ )  $\pm 50$  mA Storage Temperature ( $T_{STG}$ )  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ 

Junction Temperature (T<sub>J</sub>)

 CDIP
 175°C

 PDIP
 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 (Unless Otherwise Specified) (AC)
 4.5V to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

Output Voltage (V<sub>O</sub>)
Operating Temperature (T<sub>A</sub>)

Minimum Input Edge Rate (ΔV/Δt) 'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt)
'ACT Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

OV to Vcc

### **DC Characteristics for 'AC Family Devices**

| V1.0                             | = TUOV                               | 8.0                    | 74                      | AC                   | 0.0  | 54AC                            | 1.5            | 74AC                 | levi                  | LL WOLL on         |                                       |                                    |
|----------------------------------|--------------------------------------|------------------------|-------------------------|----------------------|------|---------------------------------|----------------|----------------------|-----------------------|--------------------|---------------------------------------|------------------------------------|
| Symbol                           | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | 25°C                 | -5   | T <sub>A</sub> = 5°C to + 125°C | -40            | T <sub>A</sub> =     | 85°C                  | Units              | Con                                   | ditions                            |
|                                  |                                      | 5.4                    | Тур                     |                      | 5,4  | Guaranteed L                    | imits          | 6.5                  |                       |                    |                                       |                                    |
| VIL OF HIV<br>- 24 mA<br>- 24 mA | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 3,70 | 2.1<br>3.15<br>3.85             |                | 2.1<br>3.15<br>3.85  |                       | ٧                  | V <sub>OUT</sub> = or V <sub>CC</sub> |                                    |
| V <sub>ILA<sub>M</sub></sub> oa  | Maximum Low Level Input Voltage      | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | .0   | 0.9<br>1.35<br>1.65             | rgo,0<br>100.0 | 0.9<br>1.35<br>1.65  | lavi                  | V Color            | V <sub>OUT</sub> = or V <sub>CC</sub> |                                    |
| V <sub>OH</sub>                  | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 0.50 | 2.9<br>4.4<br>5.4               |                | 2.9<br>4.4<br>5.4    |                       | ٧                  | I <sub>OUT</sub> =                    | -50 μΑ                             |
| OND O                            | yV = /V Au                           | 3.0                    |                         | 2.56                 | 計士   | 2.4                             |                | 2.46                 |                       | n input<br>Current | *V <sub>IN</sub> =                    | V <sub>IL</sub> or V <sub>IH</sub> |
| N VIH                            | V = V $V = OV$ $V = OV$              | 4.5<br>5.5             |                         | 3.86<br>4.86         | 014  | 3.7<br>4.7                      |                | 3.76<br>4.76         | ATE                   | VT III             | ГОН                                   | -24 mA<br>-24 mA                   |
| Vol.                             | Maximum Low Level Output Voltage     | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 1.0  | 0.1<br>0.1<br>0.1               | 0.0            | 0.1<br>0.1<br>0.1    | nut                   | m loving           | lout =                                | 50 μΑ                              |
| 3.85V                            | GHOV Am                              | -75                    |                         |                      | 18-  |                                 |                | 8.8                  |                       | laenuk             | *V <sub>IN</sub> =                    | VIL or VIH                         |
| 33)                              | V <sub>IN</sub> = V                  | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | ar   | 0.50<br>0.50<br>0.50            |                | 0.44<br>0.44<br>0.44 | ins                   | V                  | loL                                   | 12 mA<br>24 mA<br>24 mA            |
| I <sub>IN</sub>                  | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 |      | ±1.0                            | Mind a to      | ±1.0                 | a tuqni i<br>qhio ani | μΑ                 | $V_I = V_0$                           | CC, GND                            |

±50 mA

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued) and the Continued of 
|        |                                      |                        | 74               | 4AC 54AC 74AC |                                     | 74AC                            | 08.00E0 | Willitary/Aeros  |  |
|--------|--------------------------------------|------------------------|------------------|---------------|-------------------------------------|---------------------------------|---------|--|--|
| Symbol | Parameter (bed                       | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | = 25°C        | T <sub>A</sub> = -55°C to + 125°C   | T <sub>A</sub> = -40°C to +85°C | Units   | Conditions   |  |
|        | (ACT) 4.5/                           |                        | Тур              | untint to     | Guaranteed Limits                   |                                 |         | DC loout Diode O   |  |
| loz    | Maximum TRI-STATE<br>Leakage Current | 5.5                    | DA) ebi          | ±0.5          | Am 02 -<br>± 10.002 +<br>V3.0 + mov | ±5.0                            | μА      | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , $V_{GND}$<br>$V_{O}$ = $V_{CC}$ , GND |  |
| IOLD   | †Minimum Dynamic                     | 5.5                    | 7                | DANDAN        | 50                                  | 75 66                           | mA      | $V_{OLD} = 1.65V$  |  |
| IOHD   | Output Current                       | 5.5                    | eut Ede          | nt mumis      | -50 OS-                             | -75                             | mA      | $V_{OHD} = 3.85V$  |  |
| Icc    | Maximum Quiescent<br>Supply Current  | 5.5                    | 30% to           | 8.0           | 160 0+ 00                           | 08_0.5V to                      | μА      | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

## **DC Characteristics for 'ACT Family Devices**

|                  |                                      |                        | 744              | ACT          |                   | 54ACT                             |                     | 74ACT                      |                      |                            |                                       |  |
|------------------|--------------------------------------|------------------------|------------------|--------------|-------------------|-----------------------------------|---------------------|----------------------------|----------------------|----------------------------|---------------------------------------|--|
| Symbol           | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | 25°C         | -55               | T <sub>A</sub> = -55°C to + 125°C |                     | T <sub>A</sub> =           | 85°C                 | Units                      | Conditions                            |  |
|                  |                                      |                        | Тур              |              |                   | Guaranteed l                      | Limits              | rrabbas. Na<br>de devaison | av gnibi<br>datos si | BU luqai Vid<br>OTTM eiren | e, and outp                           | nutenadmet<br>respo briem                              |
| VIH              | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0          | teol              | 2.0                               | R O                 | 2.0                        |                      | lelYe!                     | V <sub>OUT</sub> = or V <sub>CC</sub> | = 0.1V<br>- 0.1V                                       |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | A&3               | 0.8 OA<br>0.8                     | 45                  | 0.8                        |                      | ٧                          | V <sub>OUT</sub> = or V <sub>CC</sub> |  |
| V <sub>OH</sub>  | Minimum High Level                   | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | of 35             | 4.4<br>5.4                        | A                   | 4.4<br>5.4                 |                      | ٧                          | I <sub>OUT</sub> =                    | -50 μΑ   |
|                  | V VOUT                               | 4.5<br>5.5             |                  | 3.86<br>4.86 | 2.1<br>3.1<br>3.8 | 3.70 31 8<br>4.70 30 8            | 1.5<br>2.25<br>2.75 | 3.76<br>4.76               | leve                 | n High L                   | *V <sub>IN</sub> =                    | V <sub>IL</sub> or V <sub>IH</sub><br>-24 mA<br>-24 mA |
| VoL              | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1          | 1.3               | 0.1                               | 1.5                 | 0.1<br>0.1                 | leve                 | V ste                      | I <sub>OUT</sub> =                    | 50 μΑ  |
| - 50 µA          | = rool v                             | 4.5<br>5.5             |                  | 0.36<br>0.36 | 2.1               | 0.50<br>0.50                      | 2,99                | 0.44                       |                      | n High L<br>VolVge         | *V <sub>IN</sub> =                    | V <sub>IL</sub> or V <sub>IH</sub><br>24 mA<br>24 mA   |
| Am St —          | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | 2.4               | ±1.0                              |                     | ±1.0                       |                      | μА                         | $V_1 = V_0$                           | CC, GND  |
| loz              | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                  | ±0.5         | 8.7               | ±10.0                             |                     | ±5.0                       |                      | μΑ                         | $V_1 = V_1$ $V_0 = V_2$               | L, V <sub>IH</sub>                                     |
| I <sub>CCT</sub> | Maximum I <sub>CC</sub> /Input       | 5.5                    | 0.6              |              | 0.0               | 1.6                               | 0.002               | 1.5                        | leve                 | mA                         | $V_{\parallel} = V_{0}$               | CC - 2.1V  |
| lold             | †Minimum Dynamic                     | 5.5                    |                  |              | .0                | 50                                | 100.0               | 75                         |                      | mA                         | V <sub>OLD</sub> =                    | 1.65V  |
| IOHD IV          | Output Current                       | 5.5                    |                  |              |                   | -50                               |                     | -75                        |                      | mA                         | V <sub>OHD</sub> =                    | = 3.85V  |
| lcc              | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 8.0<br>8.0        | 160 38.9                          |                     | 80                         |                      | μΑ                         | V <sub>IN</sub> = V<br>or GND         |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| Symbol           | Parameter of        | V <sub>CC</sub> * |     | $A = +2$ $C_L = 50$ |      | to +1<br>C <sub>L</sub> = 8 | 25°C | to  | + 85°C<br>= 50 pF | Units        | Fig.<br>No. |
|------------------|---------------------|-------------------|-----|---------------------|------|-----------------------------|------|-----|-------------------|--------------|-------------|
|                  | Him Max             | 1085              | Min | Тур                 | Max  | Min                         | Max  | Min | Max               |              |             |
| fMAX             | Maximum Clock       | 3.3               | 75  | 112                 | HTH  | 100 55 TH                   | 5.0  | 60  |                   | MHz          | XAM         |
|                  | Frequency           | 5.0               | 95  | 153                 |      | 80                          |      | 85  | valid noting      | IVITZ        | 14.102      |
| tpLH             | Propagation Delay   | 3.3               | 3.5 | 8.5                 | 13.5 | 1.0                         | 16.5 | 3.5 | 15.0              | 0190         | 224         |
|                  | CP to On            | 5.0               | 2.0 | 6.0                 | 9.5  | 1.0                         | 11.5 | 2.0 | 11.0              | ns           | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay   | 3.3               | 3.5 | 7.5                 | 12.0 | 1.0                         | 15.0 | 3.5 | 13.5              | of 90        | 00.4        |
| 2-5              | CP to On            | 5.0               | 2.0 | 5.5                 | 8.5  | 1.0 <sub>0</sub> s          | 10.5 | 2.0 | 9.5               | ns           | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time  | 3.3               | 2.5 | 7.0                 | 11.0 | 1.0                         | 13.0 | 2.5 | 12.0              | ns           | 2-5         |
| 20               | 255 25              | 5.0               | 2.0 | 5.0                 | 8.5  | 1.0                         | 9.5  | 2.0 | 9.0               |              |             |
| t <sub>PZL</sub> | Output Enable Time  | 3.3               | 3.0 | 6.5                 | 10.5 | 1.0                         | 12.5 | 3.0 | 11.5              | J.Gruco      | ZHS         |
| 9-2              | en   0.6 6.1        | 5.0               | 2.0 | 5.0                 | 8.0  | 1.0                         | 9.5  | 1.5 | 9.0               | ns           | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time | 3.3               | 3.5 | 7.5                 | 12.0 | 1.0                         | 14.0 | 2.5 | 13.0              | U.C INDITION | O F         |
|                  |                     | 5.0               | 2.0 | 6.0                 | 9.5  | 1.0                         | 11.0 | 1.5 | 10.5              | ns           | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time | 3.3               | 2.0 | 5.5                 | 9.0  | 1.0                         | 10.5 | 1.5 | 10.0              |              | 0.0         |
|                  | 7 1000              | 5.0               | 1.0 | 4.5                 | 7.5  | 1.0                         | 9.0  | 1.0 | 8.5               | ns           | 2-6         |

\*Voltage Range 3.3 is 3.3V  $\pm$  0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                | 2.5 ng   | 3.6               | as 74      | AC              | 54AC  | 74AC   | Set         | 1    |
|----------------|--|-------------------|------------|-----------------|---|--|-------------|------|
| Symbol         | Parameter  | V <sub>CC</sub> * |            | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units       | Fig. |
| E-S            | n 0.3  | 6.0               | Тур        | 8.5             | Guaranteed Min  | mum dibiWestuS   | 90          | wit  |
| ts             | Set-Up Time, HIGH or LOW<br>D <sub>n</sub> to CP | 3.3<br>5.0        | 0.5        | 2.5<br>1.5      | 3.0<br>2.0  | 3.0<br>2.0   | e e ns en e | 2-7  |
| t <sub>h</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP   | 3.3<br>5.0        | -0.5<br>0  | 1.5<br>1.5      | 1.5<br>1.5  | 1.5<br>1.5   | ns          | 2-7  |
| t <sub>w</sub> | CP Pulse Width<br>HIGH or LOW                    | 3.3<br>5.0        | 3.5<br>2.0 | 6.0<br>4.0      | 7.5<br>5.5  | 7.0<br>5.0   | ns          | 2-3  |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

## 

|                  |                |                     | . 0  | SAA                    | 74AC1     |  | AAS 5 | 4AC  | T  | 74  | ACT        |             |        |
|------------------|----------------|---------------------|------|------------------------|-----------|--|-------|------|--|-----|------------|-------------|--------|
| Symbol           | edinU          | Parameter of        |      | The sales of the sales | 5°C<br>pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |       |      | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |     | Units      | Fig.<br>No. |        |
|                  |                | xetil niti          | X886 | Min                    | Тур       | Max  | Min   | mild | Max  | Min | Max        |             |        |
| f <sub>MAX</sub> | Maxin          | num Clock Frequency | 5.0  | 100                    | 110       |  | 70    | 75   | 8.8  | 85  | imum Clock | ns          | XSIMIT |
| <sup>t</sup> PLH | Propa<br>CP to | igation Delay       | 5.0  | 2.5                    | 7.0       | 11.0   | 1.0   |      | 13.5   | 2.0 | 12.0       | ns<br>ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propa<br>CP to | gation Delay        | 5.0  | 2.0                    | 6.5       | 10.0   | 1.0   | 2.0  | 12.5   | 1.5 | 11.0       | ns          | 2-3, 4 |
| t <sub>PZH</sub> | Outpu          | it Enable Time      | 5.0  | 2.0                    | 6.4       | 9.5  | 1.0   | 0.5  | 11.0   | 1.5 | 10.0       | ns          | 2-5    |
| t <sub>PZL</sub> | Outpu          | it Enable Time      | 5.0  | 2.0                    | 6.0       | 9.0  | 1.0   | 2.6  | 11.0   | 1.5 | 10.0       | ns          | 2-6    |
| t <sub>PHZ</sub> | Outpu          | t Disable Time      | 5.0  | 2.0                    | 7.0       | 10.5   | 1.0   | 0.5  | 12.0   | 1.5 | 11.5       | ns          | 2-5    |
| tpLZ             | Outpu          | it Disable Time     | 5.0  | 2.0                    | 5.5       | 8.5  | 1.0   | 0.0  | 10.0   | 1.5 | 9.0        | ns          | 2-6    |

\*Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                | 1.6 10.0 ns                                      | 10.5              | 74/  | ACT             | 54ACT  | 74ACT  | Outp  | 2741 |
|----------------|--|-------------------|------|-----------------|--|--|-------|------|
| Symbol         | Parameter  | V <sub>CC</sub> * |      | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|                |  | eme               | Тур  | Section 2       | Guaranteed Min   | imum P 2013  | орега | AC   |
| ts             | Set-Up Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0               | 1.5  | 2.5             | 3.5  | 2.5  | ns    | 2-7  |
| th             | Hold Time, HIGH or LOW                           | 5.0               | -0.5 | 1.0             | *30V<br>(V) 2.0  | 1.0  | ns    | 2-7  |
| t <sub>w</sub> | CP Pulse Width HIGH or LOW                       | 5.0               | 2.5  | 3.0             | 5.0  | 4.0  | ns    | 2-3  |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

## Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions      |
|-----------------|-------------------------------|------|-------|-----------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 40.0 | pF    | $V_{CC} = 5.0V$ |

## 54AC/74AC646 • 54ACT/74ACT646 Octal Transceiver/Register with TRI-STATE® Outputs

### **General Description**

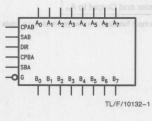
The 'AC/'ACT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in Figures 1-4.

#### **Features**

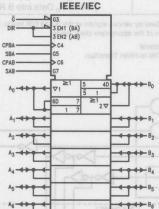
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- 'ACT646 has TTL compatible inputs
- Standard Military Drawing (SMD) - 'AC646: 5962-89682

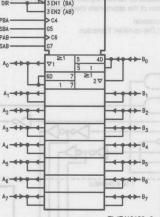
Ordering Code: See Section 8 **Logic Symbols** 

#### **Connection Diagrams**

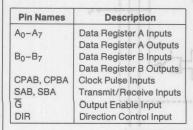


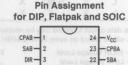






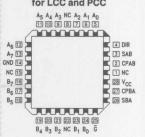
TL/F/10132-2



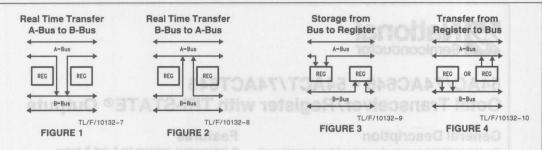








TL/F/10132-4



#### **Function Table**

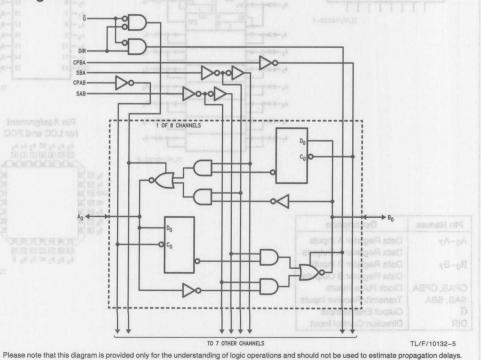
|             |             | Ir          | nputs       |             |             | Data                           | 1/0*                           | Function   |
|-------------|-------------|-------------|-------------|-------------|-------------|--------------------------------|--------------------------------|--|
| G           | DIR         | CPAB        | СРВА        | SAB         | SBA         | A <sub>0</sub> -A <sub>7</sub> | B <sub>0</sub> -B <sub>7</sub> | saded into the respective registers on the   |
| HHH         | X<br>X<br>X | H or L<br>X | Hor L<br>X  | X<br>X      | X<br>X      | Input                          | Input                          | Isolation Clock A <sub>n</sub> Data into A Register Clock B <sub>n</sub> Data into B Register  |
|             | H<br>H<br>H | X<br>HorL   | X<br>X<br>X | L<br>H<br>H | X<br>X<br>X | Input                          | Output                         | A <sub>n</sub> to B <sub>n</sub> —Real Time (Transparent Mode) Clock A <sub>n</sub> Data into A Register A Register to B <sub>n</sub> (Stored Mode) Clock A <sub>n</sub> Data into A Register and Output to B <sub>n</sub> |
| L<br>L<br>L | L<br>L<br>L | X<br>X<br>X | X<br>H or L | X<br>X<br>X | L<br>H<br>H | Output                         | Input                          | B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode) Clock B <sub>n</sub> Data into B Register B Register to A <sub>n</sub> (Stored Mode) Clock B <sub>n</sub> Data into B Register and Output to A <sub>n</sub> |

\*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

\_\_ = LOW-to-HIGH Transition

## **Logic Diagram**



4-266

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales for availability and enecifications

| Office/Distributors for availa            | bility and sp | ecifications.             |
|---|---------------|---------------------------|
| Supply Voltage (V <sub>CC</sub> )         | 18 + 01 O'04  | -0.5V to +7.0V            |
| DC Input Diode Current (I <sub>IK</sub> ) |               |                           |
| $V_1 = -0.5V$                             |               | -20 mA                    |
| $V_I = V_{CC} + 0.5V$                     |               | + 20 mA                   |
| DC Input Voltage (V <sub>I</sub> )        | -0.5V         | $to V_{CC} + 0.5V$        |
| DC Output Diode Current (IOK)             |               |                           |
| $V_0 = -0.5V$                             |               | -20 mA                    |
| $V_{\rm O} = V_{\rm CC} + 0.5V$           |               | + 20 mA                   |
| DC Output Voltage (V <sub>O</sub> )       | -0.5V to      | to V <sub>CC</sub> + 0.5V |
| DC Output Source                          |               |                           |
| or Sink Current (I <sub>O</sub> )         |               | ±50 mA                    |

DC V<sub>CC</sub> or Ground Current per Output Pin (ICC or IGND) ±50 mA Storage Temperature (TSTG) -65°C to +150°C

Junction Temperature (T<sub>J</sub>) 175°C CDIP PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Absolute Maximum Rating (Note 1) Recommended Operating Conditions

| Conditions  |  |
|---|--|
| Supply Voltage (V <sub>CC</sub> ) 'AC 'ACT 'ACT 'ACT 'ACT 'ACT 'ACT 'ACT  |  |
| Input Voltage (V <sub>I</sub> ) 0V to V <sub>CC</sub>   |  |
| Output Voltage (Vo)   |  |
| Operating Temperature (T <sub>A</sub> )  74AC/ACT  54AC/ACT  -40°C to +85°C  54AC/ACT  -55°C to +125°C  |  |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) AC Devices V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> $V_{CC}$ @ 3.3V, 4.5V, 5.5V 125 mV/ns |  |
| Minimum Input Edge Rate (ΔV/Δt) ON TOUR TOUR TOUR TOUR TOUR TOUR TOUR TOUR  |  |

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

## **DC Characteristics for 'AC Family Devices**

|                            | = ruoV v   | 0.5                    | 74                     | IAC                 | 54AC                                   | 2.1                             | 74AC                | lav       | High Le             | V <sub>ISI</sub> Minimum                       |  |
|----------------------------|--|------------------------|------------------------|---------------------|--|---------------------------------|---------------------|-----------|---------------------|--|--|
| Symbol                     | Parameter  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |                     | T <sub>A</sub> = 5<br>-55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C |                     |           | Units               | Conditions                                     |  |
|                            |  | 8.0                    | Тур                    | 8:0                 | Guaranteed Li                          | imits                           |                     |           | tage                | Input Vo                                       |  |
| VIH HIV 10 JI              | Minimum High Level<br>Input Voltage                                  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75    | 2.1<br>3.15<br>3.85 | 2.1<br>3.15<br>3.85                    | 5.49                            | 2.1<br>3.15<br>3.85 | igh Level |                     | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$            |  |
| VIL SS-                    | Maximum Low Level<br>Input Voltage                                   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75    | 0.9<br>1.35<br>1.65 | 0.9<br>1.35<br>1.65                    | 100.0                           | 0.9<br>1.35<br>1.65 | iev       | wol o               | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$         |  |
| VoH/no J<br>Am &S<br>Am &S | Minimum High Level<br>Output Voltage                                 | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49   | 2.9<br>4.4<br>5.4   | 2.9<br>4.4 0.0<br>5.4 0.0              |                                 | 2.9<br>4.4<br>5.4   |           | ٧                   | $I_{OUT} = -50 \mu\text{A}$                    |  |
|                            | DDV = IV Au  | 3.0                    |                        | 2.56                | 2.4                                    |                                 | 2.46                |           | n Input<br>Current  | $V_{IN} = V_{IL} \text{ or } V_{IH}$<br>-12 mA |  |
| YIH<br>C, GND              | V <sub>1</sub> = V <sub>10</sub> Au V <sub>1</sub> = V <sub>10</sub> | 4.5<br>5.5             |                        | 3.86<br>4.86        | 3.7<br>4.7                             |                                 | 3.76<br>4.76        | ATE       | n TIV-ST<br>Current | l <sub>OH</sub> −24 mA<br>−24 mA               |  |
| VOL                        | Maximum Low Level<br>Output Voltage                                  | 3.0<br>4.5             | 0.002<br>0.001         | 0.1<br>0.1          | 0.1<br>0.1                             | a.0                             | 0.1                 |           | V                   | $I_{OUT} = 50 \mu\text{A}$                     |  |
| xsM Vea:                   | = QJOV Am  | 5.5                    | 0.001                  | 0.1                 | 0.1                                    |                                 | 0.1                 | oile      |                     | OLD TMinimu                                    |  |
| niM Vea.s                  | = ahoV Ara   | -75                    |                        | -50                 |  |                                 |                     |           | inemu               | $*V_{IN} = V_{IL} \text{ or } V_{IH}$          |  |
| 0                          | MA OF GND  | 3.0<br>4.5             |                        | 0.36<br>0.36        | 0.50<br>0.50                           |                                 | 0.44                | ine       | 1 V                 | I <sub>OL</sub> 24 mA                          |  |
| ORND NI                    | Maximum Input Leakage Current  | 5.5<br>5.5             |                        | 0.36<br>±0.1        | 0.50<br>± 1.0                          |                                 | 0.44<br>±1.0        |           | monuO<br>μA         | $V_1 = V_{CC}$ , GND                           |  |

\*All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'AC Family Devices (Continued)

|         |                                     |                        | 74                           | AC        | 54AC                              | 74AC                            | tis sost | if Military/Aerost   |  |
|---------|-------------------------------------|------------------------|------------------------------|-----------|-----------------------------------|---------------------------------|----------|--|--|
| Symbol  | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C       |           | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units    | Conditions   |  |
| 95V 013 | ro.a                                | - 2 -                  | Typ Guaranteed Limits        |           |                                   |                                 |          | DC Input Digde Ct  |  |
| loz     | Maximum TRI-STATE® Current          | 5.5                    | age (Vo                      | ±0.5      | ±10.0                             | ±5.0                            | μА       | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , $V_{GND}$<br>$V_{O}$ = $V_{CC}$ , GND |  |
| IOLD    | †Minimum Dynamic                    | 5.5                    | TO                           | SAACAN    | 50                                | 75 (50)                         | mA       | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD    | Output Current                      | 5.5                    | nput Edg                     | I maminif | -50                               | -75                             | mA       | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc     | Maximum Quiescent<br>Supply Current | 5.5                    | 30% (g                       | 8.0       | 160.0                             | of of V680.0                    | μА       | V <sub>IN</sub> = V <sub>CC</sub><br>or GND  |  |
| lozt    | Maximum I/O<br>Leakage Current      | 5.5                    | iput Edg<br>vices<br>0.8V to | ±0.6      | Am 08 ± ± 11.0                    | ±6.0                            | μА       | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I} = V_{CC}$ , GND<br>$V_{O} = V_{CC}$ , GND           |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.
I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## **DC Characteristics for 'ACT Family Devices**

|                                 |                                       |                        | 74                     | ACT          | 54ACT                             | 74ACT                           | sol luqnik | ndino hora festiva endo  |  |            |            |     |            |     |   |  |
|---------------------------------|---------------------------------------|------------------------|------------------------|--------------|-----------------------------------|---------------------------------|------------|--|--|------------|------------|-----|------------|-----|---|--|
| Symbol                          | Parameter                             | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units      | Conditions   |  |            |            |     |            |     |   |  |
|                                 |                                       |                        | Тур                    |              | Guaranteed Li                     | imits                           | 10110      | 9910119 95   |  |            |            |     |            |     |   |  |
| V <sub>IH</sub>                 | Minimum High Level<br>Input Voltage   |                        |                        |              |                                   |                                 |            |  |  | 4.5<br>5.5 | 1.5<br>1.5 | 2.0 | 2.0<br>2.0 | 2.0 | ٧ | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$ |
| V <sub>IL</sub>                 | Maximum Low Level Input Voltage       | 4.5<br>5.5             | 1.5<br>1.5             | 0.8          | 0.8<br>0.8                        | 0.8                             | ٧          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |            |            |     |            |     |   |  |
| V <sub>OH</sub> <sub>V1.0</sub> | Minimum High Level<br>Output Voltage  | 4.5<br>5.5             | 4.49<br>5.49           | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ul Vale    | $I_{OUT} = -50 \mu\text{A}$  |  |            |            |     |            |     |   |  |
|                                 | = 100V                                | 4.5<br>5.5             |                        | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | N. Vo.     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |            |            |     |            |     |   |  |
| V <sub>OL</sub>                 | Maximum Low Level<br>Output Voltage   | 4.5<br>5.5             | 0.001<br>0.001         | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1                             | V          | I <sub>OUT</sub> = 50 μA   |  |            |            |     |            |     |   |  |
|                                 | = ruol V                              | 4.5<br>5.5             |                        | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44                            | V          | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |  |            |            |     |            |     |   |  |
| IN TO JA                        | Maximum Input<br>Leakage Current      | 5.5                    |                        | ±0.1         | ±1.0                              | ±1.0                            | μА         | $V_{I} = V_{CC}$ , GND   |  |            |            |     |            |     |   |  |
| loz                             | Maximum TRI-STATE®<br>Leakage Current | 5.5                    |                        | ±0.5         | ±10.0                             | ±5.0                            | μΑ         | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |            |            |     |            |     |   |  |
| ГССТ                            | Maximum<br>I <sub>CC</sub> /Input     | 5.5                    | 0.6                    | t.i          | 1.6                               | 1.5.8 lev                       | mA         | $V_I = V_{CC} - 2.1V$  |  |            |            |     |            |     |   |  |
| IOLD                            | †Minimum Dynamic                      | 5.5                    |                        | 1.5          | 50                                | 100.0 75.2                      | mA         | V <sub>OLD</sub> = 1.65V Max   |  |            |            |     |            |     |   |  |
| IOHD                            | Output Current                        | 5.5                    |                        |              | -50                               | -75                             | mA         | V <sub>OHD</sub> = 3.85V Min   |  |            |            |     |            |     |   |  |
| Icc                             | Maximum Quiescent<br>Supply Current   | 5.5                    |                        | 8.0          | 160.0                             | 80.0                            | μА         | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |            |            |     |            |     |   |  |
| lozt                            | Maximum I/O<br>Leakage Current        | 5.5                    |                        | ±0.6         | ±11.0<br>± 1.0±                   | ±6.0                            | μА         | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND   |  |            |            |     |            |     |   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

WOU to HOIH

| Symbol           | Parameters Ct = 50 pF  | (V)        | 10 T       | C <sub>L</sub> = 50 p | Foa = j      |            | 125°C<br>50 pF | to +85°C<br>C <sub>L</sub> = 50 pF | Units   | No.    |
|------------------|--|------------|------------|-----------------------|--------------|------------|----------------|------------------------------------|---------|--------|
|                  | Mile Max   | tolá       | Min        | Тур                   | Max          | Min        | Max            | Min Max                            | (       |        |
| t <sub>PLH</sub> | Propagation Delay<br>Clock to Bus  | 3.3<br>5.0 | 4.0<br>2.5 | 10.5<br>7.5           | 16.5<br>12.0 | 1.0<br>1.0 | 20.0<br>14.0   | 3.0 18.5<br>2.0 13.0               | ne      | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>Clock to Bus  | 3.3<br>5.0 | 3.0<br>2.0 | 9.5<br>6.5            | 14.5<br>10.5 | 1.0        | 17.5<br>12.0   | 2.5 16.0<br>1.5 11.5               | ne      | 2-3, 4 |
| tpLH             | Propagation Delay<br>Bus to Bus  | 3.3<br>5.0 | 2.5<br>1.5 | 7.5<br>5.0            | 12.0<br>8.0  | 1.0        | 15.0<br>10.0   | 2.0 13.5<br>1.0 9.0                | ne      | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>Bus to Bus  | 3.3<br>5.0 | 1.5<br>1.5 | 7.5<br>5.0            | 12.5<br>9.0  | 1.0        | 14.5<br>9.5    | 1.5 13.5<br>1.0 9.5                | ne      | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay<br>SBA or SAB to A <sub>n</sub> or B <sub>n</sub><br>(w/ A <sub>n</sub> or B <sub>n</sub> HIGH or LOW) | 3.3<br>5.0 | 2.0<br>1.5 | 8.5<br>6.0            | 13.5<br>10.0 | 1.0        | 17.0<br>12.0   | 1.5 A 01 (11.0                     | ns      | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>SBA or SAB to A <sub>n</sub> or B <sub>n</sub><br>(w/ A <sub>n</sub> or B <sub>n</sub> HIGH or LOW) | 3.3<br>5.0 | 1.5<br>1.5 | 8.5<br>6.0            | 13.5<br>10.0 | 1.0        | 17.0<br>12.0   | 1.5 15.0<br>1.5 11.0               | ns      | 2-3, 4 |
| t <sub>PZH</sub> | Enable Time<br>G to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0 | 2.5<br>1.5 | 7.0<br>5.0            | 11.5<br>8.5  | 1.0<br>1.0 | 13.0<br>9.5    | 2.0 12.5<br>1.5 9.0                |         | 2-5    |
| tpzL             | Enable Time<br>G to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0 | 2.5<br>1.5 | 7.5<br>5.5            | 12.5<br>9.0  | 1.0        | 15.5<br>11.0   | 2.0 14.0<br>1.5 10.0               | ne      | 2-6    |
| t <sub>PHZ</sub> | Disable Time<br>G to A <sub>n</sub> or B <sub>n</sub>  | 3.3<br>5.0 | 3.0<br>2.0 | 8.0<br>6.5            | 12.5<br>10.0 | 1.0        | 14.0<br>11.5   | 2.5 13.5<br>2.0 11.0               | ne      | 2-5    |
| t <sub>PLZ</sub> | Disable Time<br>G to A <sub>n</sub> or B <sub>n</sub>  | 3.3<br>5.0 | 2.0<br>1.5 | 7.5<br>6.0            | 12.0<br>9.5  | 1.0        | 13.5<br>11.0   | 2.0 13.5<br>1.5 10.5               | ne      | 2-6    |
| tPZH             | Enable Time<br>DIR to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0 | 2.0<br>1.5 | 6.5<br>5.0            | 11.0<br>7.5  | 1.0<br>1.0 | 14.5<br>10.5   | 1.5 12.0<br>1.0 8.5                | ne      | 2-5    |
| tPZL             | Enable Time<br>DIR to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0 | 2.5<br>1.5 | 7.0<br>5.0            | 11.5<br>8.0  | 1.0        | 16.0<br>12.5   | 2.0 13.0<br>1.0 9.0                | ne      | 2-6    |
| t <sub>PHZ</sub> | Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0 | 2.5<br>1.5 | 7.5<br>5.5            | 11.5<br>9.5  | 1.0        | 14.5<br>12.0   | 1.5 12.5<br>1.5 10.0               |         | 2-5    |
| t <sub>PLZ</sub> | Disable Time DIR to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0 | 1.5<br>1.5 | 7.5<br>5.5            | 12.0<br>9.5  | 1.0        | 16.5<br>12.0   | 1.5 13.5<br>1.5 10.5               | ne      | 2-6    |
| *Voltage         | Range 3.3 is 3.3V ±0.3V  |            |            |                       |              |            |                | Time                               | Oisable | ₹ (0)  |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                |   | 80                | 74.          | AC              | 54AC   | 74AC   | stedn | VA   |
|----------------|---|-------------------|--------------|-----------------|--|--|-------|------|
| Symbol         | Parameter of                            | V <sub>CC</sub> * |              | + 25°C<br>50 pF | $T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$ | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 \text{ pF}$ | Units | Fig. |
| No.            | F Ct = 60 pF                            | CL - 3d p         | Тур          | 8 = 10          | Guaranteed Min   | imum   |       | F    |
| ts             | Setup Time, HIGH or LOW<br>Bus to Clock | 3.3<br>5.0        | 2.0          | 5.0<br>4.0      | 6.0<br>4.5   | 5.5<br>4.5   | ns    | 2-7  |
| th             | Hold Time, HIGH or LOW<br>Bus to Clock  | 3.3<br>5.0        | -1.5<br>-0.5 | 0<br>0.5        | 1.5<br>2.0   | 1.0  | ns    | 2-7  |
| t <sub>w</sub> | Clock Pulse Width<br>HIGH or LOW        | 3.3<br>5.0        | 2.0          | 3.5<br>3.5      | 5.0<br>5.0   | 4.5<br>3.5   | ns    | 2-3  |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

## AC Electrical Characteristics: See Section 2 for Waveforms Management | See Section 2 for Waveforms | Management | Management | See Section 2 for Waveforms | Management | Ma

|                  |             |   | 0.4               | 5-6                | 74ACT   | TAAC | 54         | ACT                       | 74/      | ACT                    |               |             |
|------------------|-------------|---|-------------------|--------------------|---|------|------------|---------------------------|----------|------------------------|---------------|-------------|
| Symbol           | ellaU       | Parameter   | V <sub>CC</sub> * | TA = 10 + 1   CL = | T <sub>A</sub> = +25<br>C <sub>L</sub> = 50 p |      | to +       | −55°C<br>125°C<br>= 50 pF | to +     | -40°C<br>85°C<br>50 pF | Units         | Fig.<br>No. |
|                  |             | xsM alM   | xeM               | Min                | Тур   | Max  | Min        | Max                       | Min      | Max                    |               |             |
| t <sub>PLH</sub> | COLUMN TO   | pagation Delay<br>ok to Bus   | 5.0               | 6.0                | 12.0  | 14.5 | 4.0<br>2.5 | 9.3                       | 3.0      | 16.0                   | ns            | 2-3, 4      |
| t <sub>PHL</sub> | 1011        | pagation Delay<br>ok to Bus   | 5.0               | 6.0                | 12.0  | 14.5 | 3.0<br>2.0 | 3,3                       | 3.5      | 16.0                   | ns            | 2-3, 4      |
| t <sub>PLH</sub> | COLUMN TO   | pagation Delay<br>to Bus  | 5.0               | 4.5                | 8.5   | 10.5 | 2.5        | 8.8                       | 2.5      | 11.5                   | ns<br>of ello | 2-3, 4      |
| t <sub>PHL</sub> | 185.4       | pagation Delay<br>to Bus  | 5.0               | 5.0                | 8.5   | 10.5 | 1.5        | 3.3<br>6.0                | 2.0      | 11.5                   | ns            | 2-3, 4      |
| t <sub>PLH</sub> | SBA<br>(w/A | pagation Delay<br>or SAB to A <sub>n</sub> to B <sub>n</sub><br>A <sub>n</sub> or B <sub>n</sub><br>H or LOW) | 5.0               | 5.0                | 9.5   | 11.5 | 2.0        | 3.3<br>6.0<br>V)          | Sinn I   | 12.5                   | ns            | 2-3, 4      |
| t <sub>PHL</sub> |             | pagation Delay  | 12.0              | 0.1                | 0.01  | 0.8  | 1.5        | 8.8                       | AB 10 nA | SAB to A               | SBA N         | Heen        |
|                  | (w/A        | or SAB to A <sub>n</sub> to B <sub>n</sub> A <sub>n</sub> or B <sub>n</sub> H or LOW)                         | 5.0               | 5.0                | 9.5   | 11.5 |            |                           | 2.5      | 12.5                   | ns            | 2-3, 4      |
| t <sub>PZH</sub> |             | ble Time<br>A <sub>n</sub> or B <sub>n</sub>  | 5.0               | 6.0                | 9.0   | 11.0 | 2.5        | 3.8                       | 1.5      | 12.0                   | ns            | 2-5         |
| t <sub>PZL</sub> | Enat        | ble Time<br>A <sub>n</sub> or B <sub>n</sub>  | 5.0               | 5.0                | 9.0   | 11.0 | 0.6        | 3.3                       | 3.0      | 12.0                   | ns            | 2-6         |
| t <sub>PHZ</sub> |             | ble Time<br>A <sub>n</sub> or B <sub>n</sub>  | 5.0               | 7.5                | 10.5  | 13.0 | 2.0        | 2.3                       | 4.5      | 14.5                   | ns            | 2-5         |
| t <sub>PLZ</sub> |             | ble Time<br>A <sub>n</sub> or B <sub>n</sub>  | 5.0               | 5.5                | 10.0  | 12.5 | 0.8        | 3.3                       | 3.0      | 14.0                   | ns            | 2-6         |
| t <sub>PZH</sub> |             | ble Time<br>to A <sub>n</sub> or B <sub>n</sub>   | 5.0               | 5.5                | 6.5   | 10.5 | 2.5        | 8.8                       | 1.5      | 11.5                   | ns            | 2-5         |
| t <sub>PZL</sub> |             | ble Time<br>to A <sub>n</sub> or B <sub>n</sub>   | 5.0               | 4.0                | 6.5   | 10.5 | 2.5        | 8.8                       | 3.0      | 11.5                   | ns            | 2-6         |
| t <sub>PHZ</sub> |             | ble Time<br>to A <sub>n</sub> or B <sub>n</sub>   | 5.0               | 5.5                | 8.5   | 12.5 | 1.5        | 8,8                       | 4.5      | 13.5                   | ns            | 2-5         |
| t <sub>PLZ</sub> | 10000000    | ble Time<br>to A <sub>n</sub> or B <sub>n</sub>   | 5.0               | 4.0                | 8.5   | 12.5 |            |                           | 3.0 V8.0 | 13.5                   | ns            | 2-6         |

\*Voltage Range 5.0 is 5.0V ±0.5V

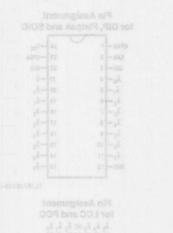
## AC Operating Requirements: See Section 2 for Waveforms

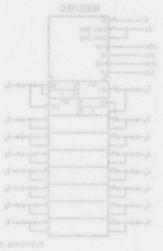
| Symbol         |                     |                                | 5°6                  | 1- = AT           | 74ACT  |     | 54ACT   | 74ACT                             |       |             |
|----------------|---------------------|--------------------------------|----------------------|-------------------|--|-----|---|-----------------------------------|-------|-------------|
|                | Parameter Parameter |                                | Tig<br>Tig<br>IniM b | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | to +85°C                          | Units | Fig.<br>No. |
|                | 1000                |                                |                      | 0.8               | Тур  | 0.8 | Guaranteed N  | Time, HIG muminil                 | Jie3  | n)          |
| ts             |                     | up Time, HIGH or L<br>to Clock | .ow                  | 5.0               | 2.5  | 7.0 | 3,3   | to Clock  0.8 Time, High or LOW   | ns    | 2-7         |
| th             | 10000000            | Time, HIGH or LO               | W                    | 5.0               | 8.0<br>0<br>8.8                                  | 2.5 | 0.8   | to Clock<br>2.5<br>http://www.nin | ns    | 2-7         |
| t <sub>w</sub> |                     | k Pulse Width<br>H or LOW      |                      | 5.0               | 4.5  | 7.0 | 1 68 1  | 8.0 ve.s                          | ns    | 2-3         |

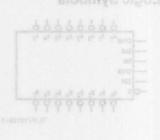
#### Capacitance

| Symbol           | Parameter                     | Тур  | Units | Conditions             |           |
|------------------|-------------------------------|------|-------|------------------------|-----------|
| C <sub>IN</sub>  | Input Capacitance             | 4.5  | pF    | V <sub>CC</sub> = 5.0V |           |
| C <sub>1/O</sub> | Input/Output Capacitance      | 15.0 | pF    | $V_{CC} = 5.0V$        |           |
| C <sub>PD</sub>  | Power Dissipation Capacitance | 60.0 | pF    | $V_{CC} = 5.0V$        | tal Trans |

m 300 mil slim dual-in-line package









# 54AC/74AC648 Octal Transceiver/Register with TRI-STATE® Outputs

#### **General Description**

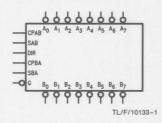
The 'AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA). The four fundamental data handling functions available are illustrated in *Figures 1* thru 4 (See Page 2).

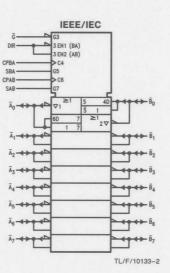
#### **Features**

- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- TRI-STATE outputs
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Inverted data to output

#### Ordering Code: See Section 8

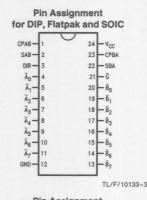
#### **Logic Symbols**

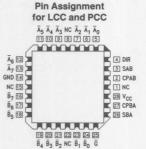




| Pin Names                         | Description                       |
|-----------------------------------|-----------------------------------|
| $\overline{A}_0 - \overline{A}_7$ | Data Register A Inputs,           |
|                                   | Data Register A TRI-STATE Outputs |
| $\overline{B}_0 - \overline{B}_7$ | Data Register B Inputs,           |
|                                   | Data Register B TRI-STATE Outputs |
| CPAB, CPBA                        | Clock Pulse Inputs                |
| SAB, SBA                          | Transmit/Receive Inputs           |
| DIR, G                            | Output Enable Inputs              |

#### **Connection Diagrams**





TL/F/10133-4

#### **Function Table**

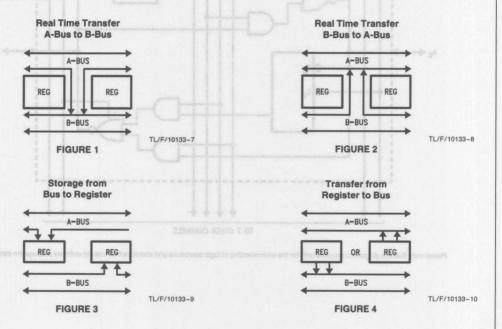
| Inputs |     |        |        |     |     |                                | 1/0*                           | Function   |   |       |       |        |                                |
|--------|-----|--------|--------|-----|-----|--------------------------------|--------------------------------|--|---|-------|-------|--------|--------------------------------|
| G      | DIR | СРАВ   | СРВА   | SAB | SBA | A <sub>0</sub> -A <sub>7</sub> | B <sub>0</sub> -B <sub>7</sub> | Tulcton  |   |       |       |        |                                |
| Н      | X   | H or L | H or L | X   | X   |                                |                                | Isolation  |   |       |       |        |                                |
| Н      | X   | _      | X      | X   | X   | Input                          | Input                          | Clock An Data into A Register                                  |   |       |       |        |                                |
| Н      | X   | X      | _      | X   | X   |                                | Impat                          |  | Clock B <sub>n</sub> Data into B Register |       |       |        |                                |
| L      | Н   | X      | X      | L   | X   | J. A.                          | -1                             | An to Bn—Real Time (Transparent Mode)                          |   |       |       |        |                                |
| L      | Н   | _      | X      | L   | X   | land.                          | 0.1.1                          | Clock An Data into A Register                                  |   |       |       |        |                                |
| L      | Н   | HorL   | X      | Н   | X   | input                          | input                          | Input  | input                                     | Input | input | Output | A Register to Bn (Stored Mode) |
| L      | Н   | _      | X      | Н   | X   | 100                            | Clores                         | Clock An Data into A Register and Output to B                  |   |       |       |        |                                |
| L      | L   | X      | X      | X   | L   |                                | p                              | B <sub>n</sub> to A <sub>n</sub> —Real Time (Transparent Mode) |   |       |       |        |                                |
| L      | L   | X      | 5      | X   | L   |                                |                                | Clock Bn Data into B Register                                  |   |       |       |        |                                |
| L      | L   | X      | HorL   | X   | Н   | Output                         | Input                          | B Register to An (Stored Mode)                                 |   |       |       |        |                                |
| L      | L   | X      | 5      | X   | Н   | 111                            |                                | Clock Bn Data into B Register and Output to A                  |   |       |       |        |                                |

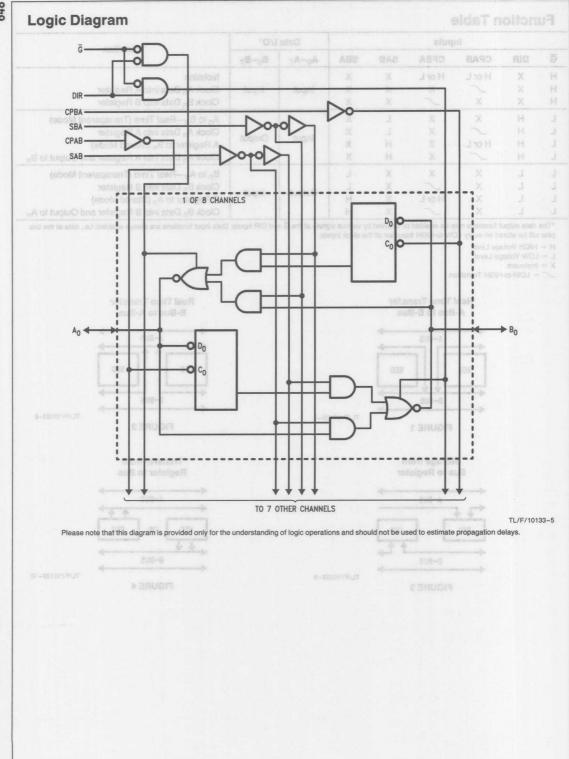
\*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level

X = Irrelevant

= LOW-to-HIGH Transition





#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )  | 0-38 + of 0.040. | 5V to +7.0V            |
|--|------------------|------------------------|
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$<br>$V_I = V_{CC} + 0.5V$    |                  | -20 mA<br>+20 mA       |
| DC Input Voltage (V <sub>I</sub> )   | -0.5V to         | V <sub>CC</sub> + 0.5V |
| DC Output Diode Current ( $I_{OI}$<br>$V_{O} = -0.5V$<br>$V_{O} = V_{CC} + 0.5V$ | 0.08             | -20 mA<br>+20 mA       |
| DC Output Voltage (V <sub>O</sub> ) DC Output Source                             | -0.5V to to      | V <sub>CC</sub> + 0.5V |

DC V<sub>CC</sub> or Ground Current per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>)

or Sink Current (IO)

Storage Temperature (T<sub>STG</sub>) Junction Temperature (T<sub>J</sub>) CDIP

PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### Recommended Operating Conditions

| AU   | Vec<br>(V)          | 2.0V to 6.0V<br>4.5V to 5.5V                     |
|--|---------------------|--|
| Input Voltage (V <sub>I</sub> )  |                     | 0V to V <sub>CC</sub>                            |
| Output Voltage (V <sub>O</sub> )   |                     | Owner Over Over                                  |
| Operating Temperature 74AC/ACT 54AC/ACT  | e (T <sub>A</sub> ) | -40°C to +85°C                                   |
| Minimum Input Edge F 'AC Devices V <sub>IN</sub> from 30% to 70 V <sub>CC</sub> @ 3.3V, 4.5V, 5. | % of                | ON municald rec                                  |
| Minimum Input Edge F 'ACT Devices  | Rate (A             | ΔV/Δt)  And outgoins loaded; thresholds on legal |

V<sub>CC</sub> @ 4.5V, 5.5V

V<sub>IN</sub> from 0.8V to 2.0V and to see sem 0.2 reliands tael must

### **DC Characteristics for 'AC Family Devices**

|                 | 1.5 14.5                            |  | 74                  | AC                  | 54AC                              | 74AC                            | velaG no                    | ten Propagat   |  |
|-----------------|-------------------------------------|--|---------------------|---------------------|-----------------------------------|---------------------------------|-----------------------------|--|--|
| Symbol          | Parameter                           | V <sub>CC</sub> T <sub>A</sub> = +25°C |                     | + 25°C              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                       | Conditions   |  |
| 2-3, 4          | 1.0 7.5 ns                          |  | Тур                 | 0.                  | Guaranteed L                      | imits                           | 81                          | Bus to Bu  |  |
| VIH             | Minimum High Level<br>Input Voltage | 3.0<br>4.5<br>5.5                      | 1.5<br>2.25<br>2.75 | 2.1<br>3.15<br>3.85 | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>8.6 3.85         | on Delay<br>s v<br>on Delay | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                             |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage  | 3.0<br>4.5<br>5.5                      | 1.5<br>2.25<br>2.75 | 0.9<br>1.35<br>1.65 | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | E B. HICO                   | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                             |  |
| V <sub>OH</sub> | Minimum High Level                  | 3.0                                    | 2.99                | 2.9                 | 2.9                               | 2.9/OJ 10 H                     | BIH OB N                    | $I_{OUT} = -50 \mu A$  |  |
|                 | Output Voltage                      | 4.5<br>5.5                             | 4.49<br>5.49        | 4.4<br>5.4          | 5.4 a f                           | 4.4<br>5.4                      | V <sub>em</sub>             | tpzji Enable T   |  |
|                 | 1.0 12.6 rs                         | 3.0                                    |                     | 2.56                | 7.6 7.0                           | 0.8 2.46                        | em<br>r B <sub>rh</sub>     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$<br>-12 mA                                  |  |
|                 | 1.0 13.0 76                         | 4.5<br>5.5                             |                     | 3.86<br>4.86        | 3.7                               | 3.76<br>4.76                    | Vomi                        | OH 20 -24 mA<br>-24 mA   |  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage    | 3.0<br>4.5                             | 0.002<br>0.001      | 0.1                 | 0.0.1                             | 8.8 0.1<br>0.3 0.1              |                             | $I_{OUT} = 50 \mu\text{A}$   |  |
|                 | 1.0 14.0 ns                         | 5.5                                    | 0.001               | 0.1                 | 1.5 1.0 1                         | 0.8 0.1                         | rne<br>or Bn                | Teldan3 word   |  |
|                 | 1.5 14.5 ns                         | 3.0<br>4.5                             |                     | 0.36<br>0.36        | 0.50                              | 0.44<br>0.44                    | W 10                        | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |  |
| 8.0             | 1.0 13.5                            | 5.5                                    |                     | 0.36                | 0.50                              | 8.8 0.44                        | emi                         | adasio 24 mA   |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current    | 5.5                                    |                     | ±0.1                | ±1.0                              | 0.8<br>±1.0                     | μА                          | $V_{I} = V_{CC}$ , GND   |  |

±50 mA

±50 mA

175°C

140°C

-65°C to +150°C

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'AC Family Devices (Continued) and a mumiks M shulped A

| Symbol<br>Valid of | /0.S Parameter                      |                        | 74AC                       |           | 54AC                              | 74AC                            | eqs -sos    | toetno angan   |  |
|--------------------|-------------------------------------|------------------------|----------------------------|-----------|-----------------------------------|---------------------------------|-------------|--|--|
|                    |                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> =           | + 25°C    | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units       | Conditions   |  |
|                    |                                     |                        | Тур                        | ut Voltag | Guaranteed L                      | imits                           | bull) finer | DC Input Diode Ou  |  |
| IOLD               | †Minimum Dynamic                    | 5.5                    | (0V) at                    | put Volta | 50 50                             | 75                              | mA          | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD               | Output Current                      | 5.5                    | JE10QITH                   | Prating F | -50.0 + 50                        | V at V8.0−75                    | mA          | V <sub>OHD</sub> = 3.85V Min   |  |
| lcc                | Maximum Quiescent<br>Supply Current | 5.5                    | f<br>lut Edge              | 8.0       | 160.0                             | 80.0                            | μΑ          | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |
| lozt<br>an\Vm      | Maximum I/O<br>Leakage Current      | 5.5                    | 98<br>10% to 7<br>V, 4.5V, | ±0.6      | V8.0 + 30<br>±11.0                | √ of of V8.0—<br>±6.0           | μΑ          | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## AC Electrical Characteristics: See Section 2 for Waveforms

|                    |  |                   |  | 74AC        | n damage     | 544  | C          | 74   | AC           | stulcedA: | Hote        |
|--------------------|--|-------------------|--|-------------|--------------|--|------------|--|--------------|-----------|-------------|
| Symbol             | Parameter  | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |             |              | $T_A = -55^{\circ}C$<br>$to + 125^{\circ}C$<br>$C_L = 50 pF$ |            | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |              | Units     | Fig.<br>No. |
|                    |  |                   | Min  | Тур         | Max          | Min  | Max        | Min  | Max          |           |             |
| t <sub>PLH</sub>   | Propagation Delay<br>Clock to Bus  | 3.3<br>5.0        | 1.5<br>1.5                                       | 10.0<br>7.0 | 15.5<br>11.0 | C Fam  | A' 101     | 1.5<br>1.5   | 17.0<br>12.0 | ns        | 2-3, 4      |
| t <sub>PHL</sub>   | Propagation Delay<br>Clock to Bus  | 3.3<br>5.0        | 1.5<br>1.5                                       | 8.5<br>6.0  | 13.5<br>10.5 | OAF)   | Vec        | 1.5<br>1.5   | 14.5<br>11.5 | ns        | 2-3, 4      |
| t <sub>PLH</sub>   | Propagation Delay<br>Bus to Bus  | 3.3<br>5.0        | 1.5  | 6.0<br>4.0  | 10.0<br>7.0  | gyT  | (A)        | 1.5<br>1.0   | 11.0<br>7.5  | ns        | 2-3, 4      |
| t <sub>PHLV</sub>  | Propagation Delay<br>Bus to Bus  | 3.3<br>5.0        | 1.5<br>1.5                                       | 5.5<br>3.5  | 9.0<br>7.5   | 1.5  | 8,0        | 1.5  | 10.0<br>8.0  | ns        | 2-3, 4      |
| t <sub>PLH</sub>   | Propagation Delay<br>SBA or SAB to A <sub>n</sub> or B <sub>n</sub><br>(with A <sub>n</sub> or B <sub>n</sub> HIGH or LOW) | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.5<br>5.5  | 12.5<br>9.0  | 2.75   | 5.5<br>3.0 | 1.5<br>1.5   | 14.0<br>10.0 | ns        | 2-3, 4      |
| t <sub>PHL</sub>   | Propagation Delay<br>SBA or SAB to A <sub>n</sub> or B <sub>n</sub><br>(with A <sub>n</sub> or B <sub>n</sub> HIGH or LOW) | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.5<br>5.5  | 12.5<br>9.5  | 2.75   | 8.5<br>3.0 | 1.5<br>1.5   | 14.0<br>10.5 | ns        | 2-3, 4      |
| t <sub>PZH</sub>   | Enable Time<br>G to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0        | 1.5<br>1.5                                       | 6.5<br>5.0  | 11.0<br>8.0  | 4,48<br>5.48   | 4,5<br>5,6 | 1.0  | 11.5<br>9.0  | ns        | 2-5         |
| tpzL               | Enable Time<br>G to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.0  | 11.0<br>8.0  | 3  | 3.0        | 1.0<br>1.0   | 12.5<br>9.0  | ns        | 2-6         |
| t <sub>PHZ</sub>   | Disable Time<br>G to A <sub>n</sub> or B <sub>n</sub>  | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.5<br>6.0  | 12.0<br>10.0 |  | 4.5<br>5.5 | 1.0<br>1.0   | 13.0<br>11.0 | ns        | 2-5         |
| t <sub>PLZ</sub> 0 | Disable Time<br>G to A <sub>n</sub> or B <sub>n</sub>  | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.5  | 11.5<br>9.0  | \$00.0<br>1 00.0   |            | 1.0  | 12.5         | ns        | 2-6         |
| t <sub>PZH</sub>   | Enable Time<br>DIR to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0        | 1.5<br>1.5                                       | 6.0<br>4.5  | 12.5<br>9.5  | 1 100.0  | 5.5        | 1.0<br>1.0   | 14.0<br>10.5 | ns        | 2-5         |
| t <sub>PZL</sub> S | Enable Time<br>DIR to A <sub>n</sub> or B <sub>n</sub>   | 3.3<br>5.0        | 1.5<br>1.5                                       | 6.5<br>4.5  | 13.0<br>9.0  | 3  | 3.0<br>4.5 | 1.5<br>1.0   | 14.5<br>10.5 | ns        | 2-6         |
| t <sub>PHZ</sub>   | Disable Time<br>DIR to A <sub>n</sub> or B <sub>n</sub>  | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.5  | 11.5<br>9.0  | 0  | 8.5        | 1.0  | 13.5<br>10.0 | ns        | 2-5         |
| t <sub>PLZ</sub>   | Disable Time<br>DIR to A <sub>n</sub> or B <sub>n</sub>  | 3.3<br>5.0        | 1.5<br>1.5                                       | 7.0<br>5.0  | 13.5<br>9.5  | to transfer elli-  | d.6        | 1.5  | 15.0<br>10.0 | ns        | 2-6         |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

LegatioNES

\$ 84-pin, PCC, CPGA

u 'ACT705 has TTL-compatible inputs

at High throughput achieved with high degree of parallel-

#### AC Operating Requirements: See Section 2 for Waveforms

|                |      |  |                   | 74   | AC         | 54AC  | 74AC   | Supple G. S. |      |
|----------------|------|--|-------------------|--|------------|---|--|--------------|------|
| Symbol         |      | Parameter                                | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units        | Fig. |
|                |      |  |                   | Тур  | HIQQA      | Guaranteed Mini   | mum  | ital S       | giQ  |
| ts             | olta | Setup Time, HIGH or LOW,<br>Bus to Clock | 3.3               | 2.0  | 3.0        |   | 3.5<br>2.0   | ns           | 2-7  |
| th             | -mo  | Hold Time, HIGH or LOW,<br>Bus to Clock  | 3.3<br>5.0        | -1.5<br>-0.5                                     | 0          | -pin teadless chip of that provide data                     | 3 ns ni 0 geloeg   | ns           | 2-7  |
| t <sub>w</sub> | noit | Clock Pulse Width HIGH or LOW            | 3.3<br>5.0        | 2.0  | 3.5<br>3.0 | single-cycle 16-bil<br>er/accumulator.                      | 4.0<br>3.0   | asboo no     | 2-3  |

\*Voltage Range 3.3 is 3.3V  $\pm 0.3$ V Voltage Range 5.0 is 5.0V  $\pm 0.5$ V voltage 8.0V  $\pm 0.5$ V voltage 6.0V  $\pm 0.5$ V voltage 8.0V  $\pm 0.5$ V voltage 8.0V  $\pm 0.5$ V voltage 8.0V  $\pm 0.5$ V voltage 6.0V  $\pm 0.5$ V voltage 8.0V  $\pm 0.5$ V voltage 6.0V  $\pm 0.5$ V voltage 8.0V  $\pm 0.5$ V voltage 6.0V  tag{2} \tag

#### Capacitance

| Symbol          | Parameter                     | Тур  | Units           | Conditions      |
|-----------------|-------------------------------|------|-----------------|-----------------|
| CIN             | Input Capacitance             | 4.5  | pF              | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 65.0 | O PER STATES OF | $V_{CC} = 5.0V$ |
| C1/0            | Input/Output Capacitance      | 15.0 | pF              | $V_{CC} = 5.0V$ |

## **Digital Signal Processing Applications**

#### **General Description**

The 'ACT705 is a high-speed arithmetic processing integrated circuit which is packaged in an 84-pin leadless chip carrier. It features separate input buses that provide data and instruction codes to a high-speed single-cycle 16-bit ALU and an 8-bit by 8-bit parallel multiplier/accumulator.

The ALU is a 16-bit parallel design which supports sixteen arithmetic and logic functions, as well as carry-in/out and borrow-in/out. The multiplier/accumulator, which offers a full 16-bit product, provides for unsigned, signed, mixed mode and imaginary number multiplication. Product accumulation with sum and difference arithmetic is available in each multiplier operating mode.

The 16-bit results of the ALU and multiplier/accumulator are multiplexed to a single set of TRI-STATE® output buffers. The two ALU and multiplier/accumulator carry-out bits, as well as the 4-bit status field indicating ALU and multiplier/accumulator error conditions make up the remaining six bits of the entire 22-bit output.

#### **Features**

- 84-pin, PCC, CPGA
- Outputs source/sink 8 mA
- 'ACT705 has TTL-compatible inputs
- High throughput achieved with high degree of parallelism in the architecture
- Pipelined stages
- High-speed 16-bit ALU and an 8 x 8 complex multiplier

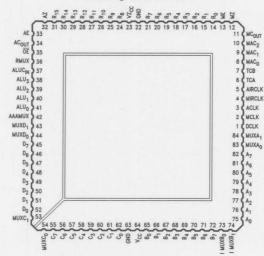
- 16-bit full ALU performs sixteen Boolean and arithmetic functions with carry-in and carry-out
- 8 x 8 parallel multiplier supports unsigned, signed, complex or mixed mode multiplications, produces 16-bit result with carry-out
- Separate data and instruction buses allow instruction fetches in parallel with execution—single cycle operation
- Accepts 8- or 16-bit data and delivers a 16-bit output
- Data register bank configured to accept a combination of 8- or 16-bit data
- Separate clocks for ALU instruction, multiplier instruction, data, ALU accumulator and multiplier accumulator registers
- Clustered clock pins for ease of board design
- 16-bit ALU/accumulator with feedback to ALU input
- Status of accumulator inputs is monitored: conditions monitored include twos complement overflow, underflow or equal-to-zero

#### **Applications**

- Voice-band signal processing
- Discrete Fourier transform applications
- FIR filters
- IIR filters
- Fast Fourier transform applications
  - Spectrum analysis
  - Speech recognition

#### **Connection Diagram**

#### Pin Assignment for PCC



TL/F/10135-1

## **Programmable Video Sync Generator**

### **General Description**

The 'ACT715/LM1882 is a 20-pin TTL-input compatible device capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The device is capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

The 'ACT715/LM1882 makes no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

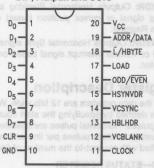
#### **Features**

- Maximum Input Clock Frequency > 100 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register program-
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into
- Orderable as linear device LM1882CN or LM1882CM

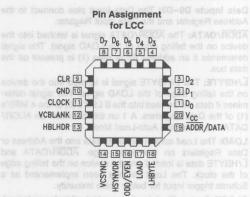
#### Ordering Code: See Section 8

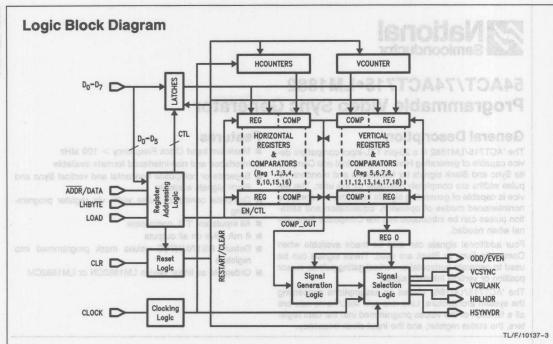
#### **Connection Diagrams**

Pin Assignment for DIP. Flatpak and SOIC



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#### **Pin Description**

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

**Data Inputs D0-D7:** The Data Input pins connect to the Address Register and the Data Input Register.

ADDR/DATA: The ADDR/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

L/HBYTE: The L/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

LOAD: The Load control pin loads data into the Address or Data Registers on the rising edge. ADDR/DATA and L/HBYTE data is loaded into the device on the falling edge of the clock. The Load pin has been implemented as a Schmitt trigger input for better noise immunity.

**CLOCK:** System Clock input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity.

**CLR:** The Clear pin is an asynchronous input that initializes the device when it is high. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The clear pin has been implemented as a Schmitt trigger for better noise immunity.

ODD/EVEN: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this input is always HIGH. Data can be serially scanned out on this pin during test mode.

**VCSYNC:** Outputs Vertical or Composite Sync signal based on value of the Status Register.

**VCBLANK:** Outputs Vertical or Composite Blanking signal based on value of the Status Register.

**HBLHDR:** Outputs Horizontal Blanking signal, Horizontal Gating signal or cursor position based on value of the Status Register.

**HSYNVDR:** Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

## **Register Description**

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

#### **REGO—STATUS REGISTER**

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs.

Bits 0-2

| B <sub>2</sub> | B <sub>1</sub> | B <sub>0</sub> | VCBLANK | VCSYNC | HBLHDR | HSYNVDR |
|----------------|----------------|----------------|---------|--------|--------|---------|
| 0              | 0              | 0              | CBLANK  | CSYNC  | HGATE  | VGATE   |
| 0              | 0              | 1              | VBLANK  | CSYNC  | HBLANK | VGATE   |
| 0              | 1              | 0              | CBLANK  | VSYNC  | HGATE  | HSYNC   |
| 0              | 1              | 1              | VBLANK  | VSYNC  | HBLANK | HSYNC   |
| 1              | 0              | 0              | CBLANK  | CSYNC  | CURSOR | VINT    |
| 1              | 0              | 1              | VBLANK  | CSYNC  | HBLANK | VINT    |
| 1              | 1              | 0              | CBLANK  | VSYNC  | CURSOR | HSYNC   |
| 1              | 1              | 1              | VBLANK  | VSYNC  | HBLANK | HSYNC   |

#### Register Description (Continued)

Bits 3-4

| B <sub>4</sub>          | B <sub>3</sub>                     | Mode of Operation                                |
|-------------------------|------------------------------------|--|
| of 10 he                |                                    | Interlaced Double Serration and Equalization     |
| 0                       | ed. Ind si                         | Non Interlaced Double Serration                  |
| WO4 svi                 | 0 80                               | Illegal State                                    |
| generate<br>entical In- | use <mark>d for</mark><br>s. The V | Non Interlaced Single Serration and Equalization |

#### Bits 5-8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates a pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity (1) SSRI = Albumosau Charles

B6— VCSYNC Polarity (1) 03H) = dtatW loument leather

**B7— HBLHDR Polarity** 

**B8**— HSYNVDR Polarity

#### Bits 9-11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0) Enable System Clock (1)

B11— Disable Counter Test Mode (0) Enable Counter Test Mode (1)

#### **HORIZONTAL INTERVAL REGISTERS**

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1- Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3- Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

#### **VERTICAL INTERVAL REGISTERS**

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7- Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

## EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10- Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical

Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

#### **CURSOR LOCATION REGISTERS**

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15- Horizontal Cursor Position Start Time

REG16- Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

#### Signal Specification

## HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at  $2\times$  the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) = REG(4)  $\times$  ckper

Horizontal Blanking Width = [REG(3) - 1]  $\times$  ckper

Horizontal Sync Width = [REG(2) - REG(1)] × ckper

Horizontal Front Porch  $= [REG(1) - 1] \times ckper$ 

#### VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC.

Vertical Frame Period (VPER) = REG(8) × hper

Vertical Field Period (VPER/n) = REG(8) × hper/n

Vertical Blanking Width =  $[REG(7) - 1] \times hper/n$ 

Vertical Syncing Width =  $[REG(6) - REG(5)] \times hper/n$ 

Vertical Front Porch =  $[REG(5) - 1] \times hper/n$ 

where n = 1 for noninterlaced

n = 2 for interlaced

#### COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The serration pulse interval occurs in place of the Vertical Sync interval. Equalization pulse

Where n = 1 for noninterlaced single serration/equalization

n = 2 for noninterlaced double serration/equalization

n = 2 for interlaced operation

#### **HORIZONTAL AND VERTICAL GATING SIGNALS**

Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of bit 2 of the status register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) - REG(15)] × ckper

= [REG(18) - REG(17)]  $\times$ Vertical Gating Signal Width hper

able when Composite Sync and Blank signals are selected and bit 2 of the Status Register is set to the value of 1. The cursor position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking sig-

Horizontal Cursor Width = [REG(16) - REG(15)] × ckper Vertical Cursor Width = [REG(18) - REG(17)] × hper Vertical Interrupt Width = [REG(14) − REG(13)] × hper

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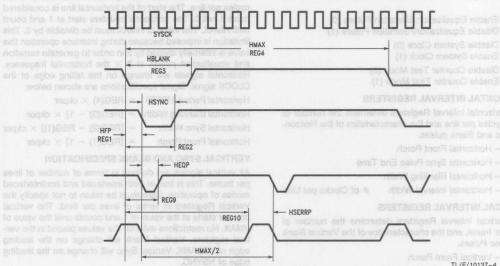


FIGURE 1. Horizontal Waveform Specification

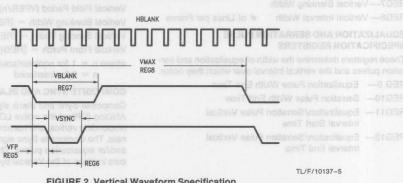
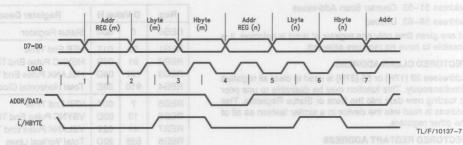


FIGURE 2. Vertical Waveform Specification

#### ADDRCNTR LOGIC

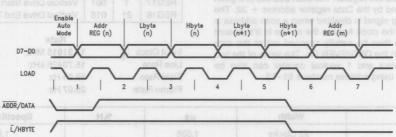
Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 Load cycles (19 Address and 38 Data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 Load cycles to completely program all registers (1 Address and 38 Data). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High

was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of load when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of load after ADDRDATA and LHBYTE goes low.



Manual Addressing Mode

| Cycle #           | Load Falling Edge        | Load Rising Edge |
|-------------------|--------------------------|------------------|
| Pulse Interval So | Enable Manual Addressing | Load Address m   |
| 2                 | Enable Lbyte Data Load   | Load Lbyte m     |
| Idimetal 3 ninev  | Enable Hbyte Data Load   | Load Hbyte m     |
| Igunetal 4 outeV  | Enable Manual Addressing | Load Address n   |
| Honzotal Drive    | Enable Lbyte Data Load   | Load Lbyte n     |
| Horno I a 6 shold | Enable Hbyte Data Load   | Load Hbyte n     |



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|         | Auto Addressing Mode     |                               |  |  |  |  |  |  |  |  |
|---------|--------------------------|-------------------------------|--|--|--|--|--|--|--|--|
| Cycle # | Load Falling Edge        | Load Rising Edge              |  |  |  |  |  |  |  |  |
| 5.6 1   | Enable Auto Addressing   | Load Start Address n          |  |  |  |  |  |  |  |  |
| 2       | Enable Lbyte Data Load   | Load Lbyte (n)                |  |  |  |  |  |  |  |  |
| 3       | Enable Hbyte Data Load   | Load Hbyte (n); Inc Counter   |  |  |  |  |  |  |  |  |
| 4       | Enable Lbyte Data Load   | Load Lbyte (n+1)              |  |  |  |  |  |  |  |  |
| 5       | Enable Hbyte Data Load   | Load Hbyte (n+1); Inc Counter |  |  |  |  |  |  |  |  |
| 6       | Enable Manual Addressing | Load Address                  |  |  |  |  |  |  |  |  |

## Addressing Logic (Continued)

#### ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Since the data registers are disabled at this time any overlap of enable signals will not cause register data to change. The following Addresses are used by the device.

Address 0

Status Register REG0

Address 1-18 Data Registers REG1-REG18

Address 19-21 Unused

Address 22/54 Restart Vector (Restarts Device)

Address 23/55 Clear Vector (Zeros All Registers)

Address 24-31 Unused

Address 32-50 Register Scan Addresses

Address 51-53 Counter Scan Addresses

Address 56-63 Unused

At any given time only one register at most is selected. It is possible to have no registers selected.

#### **VECTORED CLEAR ADDRESS**

Addresses 23 (17H) or 55 (37H) is used to clear all registers simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers.

#### **VECTORED RESTART ADDRESS**

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the programming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence.

#### SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51–53.

Normal device operation can be resumed by latching in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

#### **RS170 Default Register Values**

The tables below show the values programmed for the RS170 Format and how they compare against the actual EIA RS170 Specifications. The default signals that will be displayed are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected a pulse indicating the active lines would be displayed.

| Reg   | D Va | lue H | Register Description               |
|-------|------|-------|------------------------------------|
| REG0  | 0    | 000   | Status Register                    |
| REG1  | 23   | 017   | HFP End Time                       |
| REG2  | 91   | 05B   | HSYNC Pulse End Time               |
| REG3  | 157  | 09D   | HBLANK Pulse End Time              |
| REG4  | 910  | 38E   | Total Horizontal Clocks            |
| REG5  | 7    | 007   | VFP End Time                       |
| REG6  | 13   | 00D   | VSYNC Pulse End Time               |
| REG7  | 41   | 029   | VBLANK Pulse End Time              |
| REG8  | 525  | 20D   | Total Vertical Lines               |
| REG9  | 57   | 038   | Equalization Pulse End Time        |
| REG10 | 410  | 19A   | Serration Pulse Start Time         |
| REG11 | 1    | 001   | Pulse Interval Start Time          |
| REG12 | 19   | 013   | Pulse Interval End Time            |
| REG13 | 41   | 029   | Vertical Interrupt Activate Time   |
| REG14 | 526  | 20E   | Vertical Interrupt Deactivate Time |
| REG15 | 911  | 38F   | Horizontal Drive Start Time (1)    |
| REG16 | 92   | 05C   | Horizontal Drive End Time          |
| REG17 | 1    | 001   | Vertical Drive Start Time          |
| REG18 | 21   | 015   | Vertical Drive End Time            |

|             | Rate         | Period    |
|-------------|--------------|-----------|
| Input Clock | 14.31818 MHz | 69.841 ns |
| Line Rate   | 15.73426 kHz | 63.556 µs |
| Field Rate  | 59.94 Hz     | 16.683 ms |
| Frame Rate  | 29.97 Hz     | 33.367 ms |

| Signal       | Width      | μs     | %H             | Specification (μs) |
|--------------|------------|--------|----------------|--------------------|
| HFP          | 22 Clocks  | 1.536  |                | 1.5 ±0.1           |
| HSYNC Width  | 68 Clocks  | 4.749  | 7.47           | 4.7 ± 0.1          |
| HBLANK Width | 156 Clocks | 10.895 | 17.15          | 10.9 ± 0.2         |
| HDRIVE Width | 91 Clocks  | 6.356  | 10.00          | 0.1H ± 0.005H      |
| HEQP Width   | 34 Clocks  | 2.375  | 3.74           | 2.3 ±0.1           |
| HSERR Width  | 68 Clocks  | 4.749  | phuA elden7.47 | 4.7 ± 0.1          |
| HPER IOD     | 910 Clocks | 63.556 | red J eld 100  | 2                  |

#### RS170 Default Register Values (Continued)

| Signal             | Width              | μs               | %V       | Specification                      |
|--------------------|--------------------|------------------|----------|------------------------------------|
| VFP<br>VSYNC Width | 3 Lines<br>3 Lines | 190.67<br>190.67 | - AT DOV | 6 EQP Pulses<br>6 Serration Pulses |
| VBLANK Width       | 20 Lines           | 1271.12          | 7.62     | $0.075V \pm 0.005V$                |
| VDRIVE Width       | 11.0 Lines         | 699.12           | 4.20     | $0.04V \pm 0.006V$                 |
| VEQP IntrvI        | 9 Lines            | Guaran           | 3.63     | 9 Lines/Field                      |
| VPERIOD (field)    | 262.5 Lines        | 16.683 ms        |          | 16.683 ms/Field                    |
| VPERIOD (frame)    | 525 Lines          | 33.367 ms        | 5.5      | 33.367 ms/Frame                    |

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| ,   |  |
|---|--|
| Supply Voltage (V <sub>CC</sub> ) DC Input Diode Current (I <sub>IK</sub> )   | -0.5V to +7.0V                                     |
| $V_I = -0.5V$<br>$V_I = V_{CC} + 0.5V$  | -20 mA<br>+20 mA                                   |
| DC Input Voltage (V <sub>I</sub> )  | $-0.5$ V to $V_{CC} + 0.5$ V                       |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$<br>DC Output Voltage ( $V_O$ )<br>DC Output Source | -20 mA<br>+20 mA<br>-0.5V to V <sub>CC</sub> +0.5V |
| or Sink Current (I <sub>O</sub> )   | ± 15 mA  |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )  | ± 20 mA  |
| Storage Temperature (T <sub>STG</sub> )   | -65°C to +150°C                                    |
| Junction Temperature (T <sub>J</sub> )  CDIP  PDIP  | 175°C<br>140°C                                     |
| 4,8-3, 1, 30, 1, 6,81, , 86   | university and subject descriptions                |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

# Recommended Operating Conditions

|      | ply Voltage (V <sub>CC</sub> )<br>CT/LM1882 |        |            | 4.5V to 5.5V          |
|------|---|--------|------------|-----------------------|
| Inpu | it Voltage (V <sub>I</sub> )                |        |            | OV to V <sub>CC</sub> |
| Out  | put Voltage (V <sub>O</sub> )               |        |            | OV to VCC             |
|      | erating Temperature<br>4ACT/LM1882          | (AT) € | A-cal Char |                       |

-54 ACT/LM1882  $-55^{\circ}$  C to  $+125^{\circ}$  C Minimum Input Edge Rate ( $\Delta V/\Delta t)$  'AC Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt) 'ACT/LM1882 Devices

V<sub>IN</sub> from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

| Symbol           | Parameter                            |                     | 74ACT/   | LM1882       | 54ACT/LM1882   | 74ACT/LM1882                       | 90     | Capacitán  |
|------------------|--------------------------------------|---------------------|--|--------------|--|------------------------------------|--------|--|
|                  |                                      | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C | Units  | Conditions   |
|                  |                                      |                     | Тур  |              | Guaranteed Li  | mits                               | Pow    | GeD.   |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49                                     | 4.4<br>5.4   |  | 4.4<br>5.4                         | V      | $I_{OUT} = -50 \mu A$                                |
|                  |                                      | 4.5<br>5.5          |  | 3.86<br>4.86 |  | 3.76<br>4.76                       | V<br>V | $V_{IN} = V_{IL}/V_{IH}$<br>$I_{OH} = -8 \text{ mA}$ |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5          | 0.001<br>0.001                                   | 0.1<br>0.1   |  | 0.1<br>0.1                         | V      | $I_{OUT} = 50 \mu A$                                 |
|                  |                                      | 4.5<br>5.5          |  | 0.36<br>0.36 |  | 0.44<br>0.44                       | V      | $V_{IN} = V_{IL}/V_{IH}$<br>$I_{OH} = +8 \text{ mA}$ |
| I <sub>OLD</sub> | Minimum Dynamic<br>Output Current    | 5.5                 |  |              |  | 32.0                               | mA     | V <sub>OLD</sub> = 1.65V                             |

<sup>\*</sup>All outputs loaded; thresholds on input associated with input under test.

#### **DC Characteristics**

For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified) (Continued)

| Symbol          | asetu 9 909 0<br>y 9 notismo 2 3<br>0.0 Parameter<br>100.0 ± V+0.0<br>ble 19 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ |                     |                      |                 | 54ACT/LM1882  | 74ACT/LM1882   |       | ggy                      |
|-----------------|--|---------------------|----------------------|-----------------|---|--|-------|--------------------------|
|                 |  | V <sub>CC</sub> (V) |                      |                 | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ | T <sub>A</sub> = -40°C<br>to +85°C   | Units | Conditions               |
|                 |  | - 83                | Тур                  |                 | Guaranteed Li   | mits   |       | VEQP latest              |
| IOHD            | Minimum Dynamic<br>Output Current  | 5.5                 |                      | am til<br>em Vi | 18.68<br>18.68  | and -32.0  | mA    | V <sub>OHD</sub> = 3.85V |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current   | 5.5                 | ±0.1                 |                 | Note 1)<br>e required.                                      | 3011±1.0   | μА    | $V_{I} = V_{CC}$ , GND   |
| Icc<br>Va.a or  | Supply Current<br>Quiescent  | 5.5                 | (00V) oper by 8.0 18 |                 | otor Sales  | briodine3 (should specific spe | μA    | $V_{IN} = V_{CC}$ , GND  |
| ICCT            | Maximum I <sub>CC</sub> /Input   | 5.5                 | 0.6                  | Input Volta     | VQ,Y + or Ve  | 1.5  | mA    | $V_{IN} = V_{CC} - 2.1V$ |

Note 1: Test Load 50 pF,  $500\Omega$  to Ground.

#### AC Electrical Characteristics: See Section 2 for Waveforms

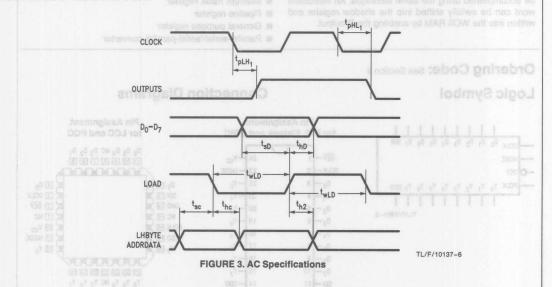
| Symbol            | Parameter OOV                                       | etaFl e             | 74A                                | CT/LM1 | 882  | 54ACT/LM1882   |  | 74ACT/LM1882   |   | DO Output Diod |                           |
|-------------------|---|---------------------|------------------------------------|--------|------|--|--|--|---|----------------|---------------------------|
|                   |   | V <sub>CC</sub> (V) | $T_{A}=+25^{\circ}C$ $C_{L}=50$ pF |        |      | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ |  | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |   | Units          | Fig.                      |
|                   |   | e Rate (            | Min                                | Тур    | Max  | Min  | Max  | Min  | Max   | nk Cura        |                           |
| f <sub>MAXI</sub> | Interlaced f <sub>MAX</sub><br>(HMAX/2 is ODD)      | 5.0                 | 170                                | 190    |      | Am 0S±   |  | 150  | und Ourrent<br>1 (loc or lawn               | MHz            | DC V <sub>C</sub><br>peri |
| f <sub>MAX</sub>  | Non-Interlaced f <sub>MAX</sub><br>(HMAX/2 is EVEN) | 5.0                 | 190                                | 220    |      | D4524  | 1 O de   | 175  | rature (1.57g)<br>yrature (T <sub>J</sub> ) | MHz            | Junetic                   |
| t <sub>PLH1</sub> | Clock to Any Output                                 | 5.0                 | 4.0                                | 13.0   | 15.5 | 140°C<br>egenab date                                   | w brownd seu   | 3.5  | 18.5  | ns             | 2-3, 4                    |
| t <sub>PLH2</sub> | Clock to ODDEVEN<br>(Scan Mode)                     | 5.0                 | 4.5                                | 15.0   | 17.0 | wwer sustply, and recome                               | State and the parties of the parties | 3.5  | 20.5  | ns             | 2-3, 4                    |
| t <sub>PLH3</sub> | Load to Outputs                                     | 5.0                 | 4.0                                | 11.5   | 16.0 |  |  | 3.0  | 19.5  | ns             | 2-3, 4                    |

#### Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions      |  |
|-----------------|-------------------------------|------|-------|-----------------|--|
| CIN             | Input Capacitance             | 7.0  | of pF | $V_{CC} = 5.0V$ |  |
| C <sub>PD</sub> | Power Dissipation Capacitance | 17.0 | pF    | $V_{CC} = 5.0V$ |  |

| Symbol             | Parameter  Control Setup Time ADDR/DATA to LOAD — L/HBYTE to LOAD — | Vcc<br>(V) | T <sub>A</sub> = +25°C |            | $T_A = -55^{\circ}C$<br>to + 125°C  | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$ | Units    | Fig.       |
|--------------------|---|------------|------------------------|------------|---|---|----------|------------|
|                    |   |            | Тур                    |            | Guaranteed Minimums   |   |          |            |
| t <sub>sc</sub>    |   |            | 3.0<br>3.0             | 4.0<br>4.0 | agister   | 4.5<br>4.5                                | ns<br>ns | 2-7<br>2-7 |
| t <sub>sd</sub>    | Data Setup Time<br>D7-D0 to LOAD+                                   | 5.0        | 2.0                    | 4.0        | ourpose pipeline reg-<br>er for performing se-                                    | danemen books fig                         | s al STS | 2-7        |
| thc                | Control Hold Time<br>LOAD – to ADDR/DATA<br>LOAD – to L/HBYTE       | 5.0        | 0 0                    | 1.0        | store foading. let data path pipeline ine diagnostic regis- pipeline cesteres and | 1.0<br>1.0                                | ns<br>ns | 2-7<br>2-7 |
| t <sub>hd</sub>    | Data Hold Time<br>LOAD+ to D7-D0                                    | 5.0        | d beneggin<br>\ear1.0  | 2.0        | ort (as in WCS load-  | ough the D Input p<br>2.0                 | ns       | 2-7        |
| t <sub>rec</sub>   | LOAD+ to CL- (Note 1)   | 5.0        | 5.5                    | 7.0        | llexer inputs that se-  | 8.0                                       | ns       | 2-3,       |
| t <sub>wld</sub> - | Pulse Width<br>Load Low<br>Load High                                | 5.0<br>5.0 | 3.0<br>3.0             | 5.5<br>5.0 | ht-shift-only register<br>enal loop throughouts, status and contro                | 5.5 7.5 7.5                               | ns<br>ns | 2-3<br>2-3 |
| t <sub>wclr</sub>  | CLR Pulse Width HIGH  | 5.0        | 5.5                    | 6.5        | grosio piperne rag  | 9.5                                       | ns       | 2-3        |
| t <sub>wck</sub>   | CLOCK Width<br>(High or Low)  | 5.0        | 2.5                    | 3.0        | etc.). Then after a<br>scene out the results                                      | 3.5                                       | ns       | 2-3        |

Note 1: Removal of Vectored Reset to Clock.





## 54ACT/74ACT818 8-Bit Diagnostic Register

#### **General Description**

The 'ACT818 is a high-speed, general-purpose pipeline register with an on-board diagnostic register for performing serial diagnostics and/or writable control store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the diagnostic register to operate as a right-shift-only register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with 'ACT818 diagnostic pipeline registers. The loop can be used to scan in a complete test routine starting point (Data, Address, etc.). Then after a specified number of machine cycles it scans out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

#### **Features**

- On-line and off-line system diagnostics
- Swaps the contents of diagnostic register and output register
- Diagnostic register and diagnostic testing
- Cascadable for wide control words as used in microprogramming
- Edge-triggered D registers
- Outputs source/sink 24 mA
- 'ACT818 has TTL-compatible inputs
- 'ACT818 is functionally- and pin-compatible to AMD Am29818 and MMI 74S818

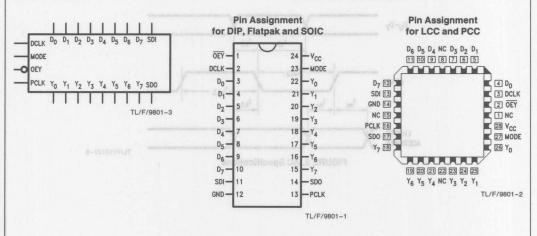
#### **Applications**

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/serial-parallel converter

Ordering Code: See Section 8

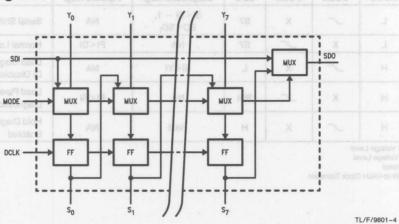
## **Logic Symbol**

## **Connection Diagrams**

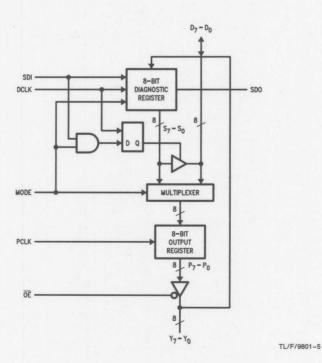


| Pin Names                      | Description             |
|--------------------------------|-------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs             |
| SDI                            | Serial Data Input       |
| DCLK                           | Diagnostics Clock       |
| MODE                           | Control Input           |
| PCLK                           | Pipeline Register Clock |
| <del>OEY</del>                 | Output Enable Input     |
| SDO                            | Serial Data Output      |
| Y0-Y7                          | Data Outputs            |

## **Diagnostic Register**



## **Block Diagram**



Functional Description
Data transfers into the diagnostic register occur on the LOW-to-HIGH transition of DCLK. Mode and SDI determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. Mode selects whether the data source is the data input or the diag-

nostic register output. Because of the independence of the clock inputs, data can be shifted in the diagnostic register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously, as long as no setup or hold times are violated. This simultaneous operation is legal.

**Function Table** 

|     | Inputs |      |      |     | Outputs   | Operation  |   |
|-----|--------|------|------|-----|---|--|---|
| SDI | MODE   | DCLK | PCLK | SDO | Diagnostic Reg.   | Pipeline Reg.  | netalgeri SusangaiO                                   |
| X   | L      | 5    | ×    | S7  | SI <si -="" 1,<br="">SO<sd<sub>I</sd<sub></si>  | NA NA  | Serial Shift; D <sub>7</sub> -D <sub>0</sub> Disabled |
| Х   | L      | X    | _    | S7  | NA  | PI <di< td=""><td>Normal Load Pipeline Register</td></di<>                       | Normal Load Pipeline Register                         |
| L   | Н      | 7    | X    | L L | SI <yi< td=""><td>NA</td><td>Load Diagnostic Register from Y<br/>DI Disabled</td></yi<> | NA   | Load Diagnostic Register from Y<br>DI Disabled        |
| Х   | Н      | X    | 5    | SDI | NA  | PI <si< td=""><td>Load Pipeline Register from<br/>Diagnostic Register</td></si<> | Load Pipeline Register from<br>Diagnostic Register    |
| Н   | Н      | 1    | X    | Н   | Hold  | NA   | Hold Diagnostic Register; DI<br>Enabled               |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

✓ = LOW-to-HIGH Clock Transition

| 14 |  |  |  |
|----|--|--|--|
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|    |  |  |  |
| -  |  |  |  |
|    |  |  |  |
|    |  |  |  |

| Supply Voltage (V <sub>CC</sub> )   | -0.5V to +7.0V                                     | 'AC 'ACT   | 2.0V to 6.0V<br>4.5V to 5.5V  |
|---|--|--|---|
| DC Input Diode Current ( $I_{IK}$ ) $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ DC Input Voltage ( $V_I$ ) $DC Output Diode Current (I_{OK}) V_O = -0.5V$ | -20 mA<br>+20 mA<br>-0.5V to V <sub>CC</sub> +0.5V | Input Voltage (V <sub>I</sub> ) Output Voltage (V <sub>O</sub> ) Operating Temperature (T <sub>A</sub> ) 74AC/ACT 54AC/ACT Minimum Input Edge Rate (ΔV/Δt) | 0V to V <sub>CC</sub><br>0V to V <sub>CC</sub><br>-40°C to +85°C<br>-55°C to +125°C |
| V <sub>O</sub> = V <sub>CC</sub> + 0.5V DC Output Voltage (V <sub>O</sub> ) DC Output Source  | +20 mA<br>-0.5V to V <sub>CC</sub> + 0.5V          | 'AC Devices V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V  | 125 mV/ns   |
| or Sink Current (I <sub>O</sub> ) DC V <sub>CC</sub> or Ground Current  | ±50 mA   | Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices   |   |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) Storage Temperature (T <sub>STG</sub> ) Junction Temperature (T <sub>J</sub> ) CDIP PDIP    | ±50 mA<br>-65°C to +150°C<br>175°C                 |  | 125 mV/ns   |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## **DC Characteristics for 'ACT Family Devices**

|                     | an 8.8 a.s  | 1                      | or 74            | ACT          | 54ACT                            | 74ACT                           | (alsCl no  | PHIL Propagate   |
|---------------------|---|------------------------|------------------|--------------|----------------------------------|---------------------------------|------------|--|
| Symbol              | Parameter   | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C |            |  |
|                     |   |                        | Тур              |              | Guaranteed L                     | imits                           |            | POLKTO   |
| V <sub>IH</sub> -S  | Minimum High Level Input Voltage  | 4.5<br>5.5             | 1.5              | 2.0          | 0.11 2.0 0.8<br>2.0              | 2.0                             | V GS       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub> O-S | Maximum Low Level Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8 G.8<br>0.8                   | 0.8                             | SDD<br>COS | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| I <sub>IN</sub> E-S | Maximum Input<br>Leakage Current  | 5.5                    | 12.1             | ±0.1         | ±10.0                            | ± 1.0                           | μА         | $V_{IN} = V_{CC}$  |
| loz                 | Maximum TRI-STATE Leakage Current   | 5.5                    | 13.              | ±0.5         | 8.01 ±10.0 T                     | ±5.0                            | μА         | $\overline{OE} = V_{IH}$<br>$V_{OUT} = 0V, V_{CC}$   |
| Icc -               | Maximum Quiescent<br>Supply Current   | 5.5                    | lar .            | 1.0          | 8.0 12.5                         | 5.0 4.5                         | mA         | $V_{IN} = V_{CC}$ or GND   |
| ICCT S              | Maximum Additional I <sub>CC</sub> /Input   | 5.5                    | 1.81             | 1.5          | 1.6 3.0                          | 1.5                             | mA         | $V_{IN} = V_{CC} - 2.1V$<br>$V_{CC} = 5.5V$  |
| V <sub>OH</sub>     | Minimum HIGH<br>Level Output Voltage,<br>Y <sub>0</sub> -Y <sub>7</sub> Outputs       | 4.5<br>5.5             | 11.              | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V          | $V_{IN} = V_{IL} \text{ or } V_{IH}$<br>$I_{OH} = -24 \text{ mA}$<br>$I_{OH} = -24 \text{ mA}$ |
|                     | Minimum HIGH<br>Level Output Voltage,<br>D <sub>0</sub> -D <sub>7</sub> , SDO Outputs | 4.5<br>5.5             | 151              | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V          | $I_{OH} = -8 \text{ mA}$<br>$I_{OH} = -8 \text{ mA}$   |
| V <sub>OL</sub>     | Maximum LOW Level Output Voltage, Y0-Y7 Outputs                                       | 4.5<br>5.5             | 18.              | 0.36<br>0.36 | 0.50 1.8<br>0.50                 | 0.44<br>0.44                    | V          | $V_{IN} = V_{IL} \text{ or } V_{IH}$<br>$I_{OL} = 24 \text{ mA}$<br>$I_{OL} = 24 \text{ mA}$   |
|                     | Maximum LOW Level Output Voltage, D0-D7, SDO Outputs                                  | 4.5<br>5.5             | 12               | 0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44                    | V          | I <sub>OL</sub> = 8 mA<br>I <sub>OL</sub> = 8 mA   |
| lo <sub>LD</sub>    | Minimum Dynamic Output Current, Y0-Y7 Outputs   | <i></i>                | NI NI            | 8.1          | 50                               | 75 8                            | mA         | $V_{OLD} = 1.65 \text{V Max}$  |

\*All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'ACT Family Devices (Continued)

|                     |  |                        | 74                | ACT   |            | 54ACT                           | 74ACT                           | laki eri  | please contact  |  |
|---------------------|--|------------------------|-------------------|---|------------|---------------------------------|---------------------------------|-----------|---|--|
| Symbol              | Parameter  | V <sub>CC</sub><br>(V) | T <sub>A</sub> =  | T <sub>A</sub> = +25°C                          |            | T <sub>A</sub> = 0°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions  |  |
|                     | (0   |                        | Тур               | annitel/ tu                                     | eneral .   | <b>Guaranteed Li</b>            | mits                            | bull iner | DC Input Dinde Cur  |  |
| IOHD                | Minimum Dynamic<br>Output Current,<br>Y <sub>0</sub> -Y <sub>7</sub> Outputs                   | 5.5                    | re (Vo)<br>mperas | put Voltar<br>arating Te                        | вО<br>gO   | Am 0S<br>-50 0S +<br>V2.0 + sol | -75                             | mA        | V <sub>OHD</sub> = 3.85V Min  |  |
| I <sub>OLD</sub>    | Minimum Dynamic<br>Output Current,<br>D <sub>0</sub> -D <sub>7</sub> , SDO Outputs<br>(Note 1) | 5.5                    | ut Edge<br>s      | AAC/AGT<br>imum Inp<br>AC Device                | viNi.      | 32 m 02<br>Am 03 +              | 32                              | mA        | V <sub>OLD</sub> = 1.65V Max<br>V <sub>0.0</sub> = 0V<br>0.0 + 00V = 0V |  |
| I <sub>OHD</sub> /m | Minimum Dynamic<br>Output Current,<br>D <sub>0</sub> -D <sub>7</sub> , SDO Outputs<br>(Note 1) | 5.5                    | at Edge           | in from 3<br>CC & 3.3t<br>Imum Inp<br>ACT Devic | r<br>eller | -32 <sub>+08±</sub>             | -32                             | mA (      | V <sub>OHD</sub> = 3.85V Min  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Test load 50 pF,  $500\Omega$  to ground.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                         |                                   |                       |     | 74ACT  | 54   | ACT  | 74   | ACT   | Apacitute no | Notine de   |
|-------------------------|-----------------------------------|-----------------------|-----|--|--|------|--|-------|--------------|-------------|
| Symbol                  | Parameter                         | V <sub>CC</sub> * (V) |     | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |       | Units        | Fig.<br>No. |
|                         |                                   |                       | Min | Тур Мах  | Min  | Max  | Min  | Max   | Chara        | DC          |
| tPHL                    | Propagation Delay<br>PCLK to Y    | 5.0                   | 3.0 | 6.0 9.0  | 1.5  | 10.5 | 2.5  | 9.5   | ns           | 2-3, 4      |
| tpLH                    | Propagation Delay<br>PCLK to Y    | 5.0                   | 3.0 | 6.5 9.0  | 1.5  | 11.0 | 2.5  | 10.0  | ns           | 2-3, 4      |
| tphL VI                 | Propagation Delay<br>MODE to SDO  | 5.0                   | 4.0 | 8.0 0.8 11.0                                     | 1.5  | 13.0 | 3.5 eve  | 12.0  | ns           | 2-3, 4      |
| tPLH VI                 | Propagation Delay<br>MODE to SDO  | 5.0                   | 4.0 | 8.0 8.0 11.5                                     | 1.5  | 14.0 | 4.0  | 12.5  | ns           | 2-3, 4      |
| t <sub>PHL</sub>        | Propagation Delay<br>SDI to SDO   | 5.0                   | 3.5 | 7.5 10.5   | 1.5  | 12.5 | 3.0  | 12.0  | ns           | 2-3, 4      |
| t <sub>PLH</sub>        | Propagation Delay<br>SDI to SDO   | 5.0                   | 3.5 | 7.5 10.5   | 1.5  | 13.0 | 3.5  | 12.0  | ns           | 2-3, 4      |
| t <sub>PHL</sub> 10 5   | Propagation Delay<br>DCLK to SDO  | 5.0                   | 4.5 | 9.0 12.5   | 1.5  | 15.5 | 4.0  | 14.0  | ns           | 2-3, 4      |
| tpih.                   | Propagation Delay<br>DCLK to SDO  | 5.0                   | 4.5 | 9.5 8.7 13.0                                     | 1.5  | 16.0 | 4.0  | 14.5  | ns           | 2-3, 4      |
| t <sub>PZL</sub> / 10 J | Output Enable Time                | 5.0                   | 2.5 | 6.0 9.0  | 1.5  | 11.0 | 2.5  | 10.0  | ns           | 2-6         |
| t <sub>PLZ</sub>        | Output Disable Time               | 5.0                   | 1.5 | 5.5 8.0  | 1.5  | 9.5  | 1.0  | 9.0   | ns           | 2-6         |
| t <sub>PZL</sub> Am     | Output Enable Time<br>DCLK to Dn  | 5.0                   | 3.0 | 8.0 12.0   | 1.5  | 15.0 | 3.0  | 13.5  | ns           | 2-6         |
| t <sub>PLZ</sub>        | Output Disable Time<br>DCLK to Dn | 5.0                   | 2.0 | 8.508.0 11.0                                     | 01.5   | 13.0 | 1.5  | 12.0  | ns           | 2-6         |
| t <sub>PZH</sub>        | Output Enable Time                | 5.0                   | 3.0 | 8.0 10.0   | 1.5  | 12.0 | 2.5  | W11.0 | ns           | 2-5         |
| t <sub>PHZ</sub> A      | Output Disable Time<br>OEY to Yn  | 5.0                   | 2.5 | 9.0 11.0   | 1.5  | 13.0 | 2.0  | 11.5  | ns           | 2-5         |
| t <sub>PZH</sub>        | Output Enable Time<br>DCLK to Dn  | 5.0                   | 3.0 | 6.5 08 11.5                                      | 1.5  | 14.0 | 3.0  | 13.0  | ns           | 2-5         |
| t <sub>PHZ</sub>        | Output Disable Time<br>DCLK to Dn | 5.0                   | 3.0 | 7.5 12.0   | 1.5  | 14.0 | 2.0  | 13.0  | ns           | 2-5         |

|                      |                                 |                   | 74                | ACT  | 54ACT   | 74ACT  | sima2 |      |
|----------------------|---------------------------------|-------------------|-------------------|------|---|--|-------|------|
| Symbol               | Parameter                       | V <sub>CC</sub> * |                   |      | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|                      |                                 | ejuci             | Тур               | TATE | Guaranteed Mini   | mum  | I Q m | 1-0  |
| t <sub>s</sub>       | Setup Time<br>D to PCLK         | 5.0               | 1.0               | 4.0  | 6.0   | 5.0  | ns    | 2-7  |
| th                   | Hold Time Dolos Teams           |                   | STATE out         |      | WITH THE STATE of 1.5   | a 10-bit D flip-flop<br>troadalo. placut                     |       | 2-   |
| ts                   | Setup Time<br>MODE to PCLK      | 5.0               | 7 a 2.5           |      | 6.5   | 5.5  | ns    | 2-   |
| th                   | Hold Time<br>MODE to PCLK       | 82-88705<br>0.5   | 28 TS8TOW<br>-1.0 | 0.0  | 0.5   | 0.0  | ns    | 2-   |
| t <sub>s</sub>       | Setup Time<br>Y to DCLK         | 5.0               | 0.5               | 2.5  | 3.5   | 2.5 200 C  | ns ns | 2-   |
| t <sub>h</sub>       | Hold Time<br>Y to DCLK          | 5.0               | 0                 | 1.0  | 2.0   | 1.5  | ns    | 2-   |
| t <sub>s</sub>       | Setup Time<br>MODE to DCLK      | 5.0               | 2.0               | 4.0  | 5.0   | 4.0  | ns    | 2-   |
| th                   | Hold Time<br>MODE to DCLK       | 5.0               | -0.5              | 1.0  | 1.5   | 1.0  | ns    | 2-   |
| t <sub>s</sub>       | Setup Time<br>SDI to DCLK       | 5.0               | 2.0               | 3.5  | 5.5   | 4.5  | ns o  | 2-   |
| t <sub>h</sub>       | Hold Time<br>SDI to DCLK        | 5.0               | -0.5              | 1.0  | 1,5   | -acron 1.0   | ns    | 2-7  |
| t <sub>s</sub>       | Setup Time<br>DCLK to PCLK      | 5.0               | 6.0               | 9.0  | 12.0  | 10.5   | ns    | 2-   |
| t <sub>s</sub>       | Setup Time<br>PCLK to DCLK      | 5.0               | 6.0               | 11.0 | 12.5  | 11.5   | ns    | 2-   |
| t <sub>w</sub>       | Pulse Width<br>PCLK HIGH or LOW | 5.0               | 2.0               | 3.0  | 4.5   | 3.0  | ns    | 2-3  |
| t <sub>w</sub> 8-981 | Pulse Width<br>DCLK HIGH or LOW | 5.0               | 2.0               | 3.0  | 4.5   | 3.0  | ns    | 2-3  |

Note 1: Test load 50 pF,  $500\Omega$  to ground. \*Voltage range 5.0 is  $5.0V \pm 0.5V$ .

## Capacitance

| Symbol  | Parameter 🔝                   | Тур | Units | Conditions             |
|---|-------------------------------|-----|-------|------------------------|
| CIN   | Input Capacitance             | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub>   | Power Dissipation Capacitance | 20  | pF    | V <sub>CC</sub> = 5.0V |
| 可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可<br>可 | 版 E go                        |     |       |                        |
|   | RANGE DE                      |     |       |                        |
|   |                               |     |       |                        |
|   |                               |     |       |                        |

## 54AC/74AC821 • 54ACT/74ACT821 10-Bit D Flip-Flop with TRI-STATE® Outputs

### **General Description**

The 'AC/'ACT821 is a 10-bit D flip-flop with TRI-STATE outputs arranged in a broadside pinout.

The 'AC/'ACT821 is functionally identical to the AM29821.

#### **Features**

- TRI-STATE outputs for bus interfacing
- Noninverting outputs
- Outputs source/sink 24 mA
- 'ACT821 has TTL-compatible inputs
- Standard Military Drawing (SMD)

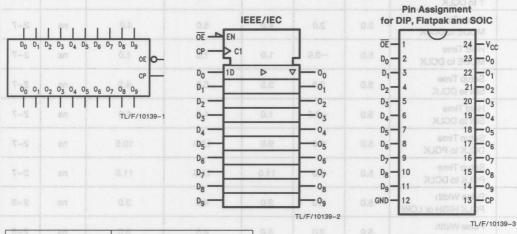
- 'ACT821: 5962-88705

## Ordering Code: See Section 8

## **Logic Symbols**

### **Connection Diagrams**

Symbol



 Pin Names
 Description

 D0-D9
 Data Inputs

 O0-O9
 Data Outputs

 OE
 Output Enable Input

 CP
 Clock Input

For LCC

D7 D6 D5 NC D4 D3 D2

11 [0] [3] [5] [5]

D8 [2]

D9 [3]

GND [4]

NC [5]

CP [6]

Q9 [7]

O8 [8]

D8 [2] [22 [24 [25]

O7 O6 O5 NC O4 O3 O2

**Pin Assignment** 

TL/F/10139-4

hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{\text{OE}}$  LOW the contents of the flip-flops are available at

the AM29821.

**Function Table** 

|            | V0/5 & |       | · arrower rans | Contractor to the second |          |
|------------|--------|-------|----------------|--------------------------|----------|
| 19 + 125°C | Inputs |       | Internal       | Outputs                  | Function |
| ŌĒ         | СР     | (IDVA | put Ergo Rate  | 1 mumlo                  | Am 08.+  |
| Н          | _      | Last  | 6 NOT LE 2008  | Z                        | High Z   |
| n\\H 351   | _      | Н     | AS'8 HS'7 'A   | Z                        | High Z   |
| L          | _      | (IN)  | Sulf Edge Hale | ACT DA                   | Load     |
| L          | _      | Н     | V0.SH// V8.6   | H'ny frant               | Load     |

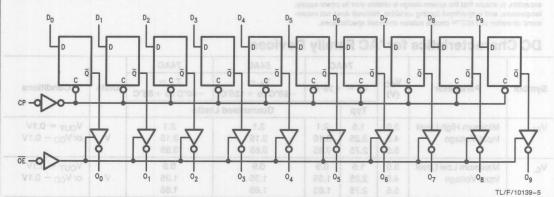
H = HIGH Voltage Level

L = LOW Voltage Level

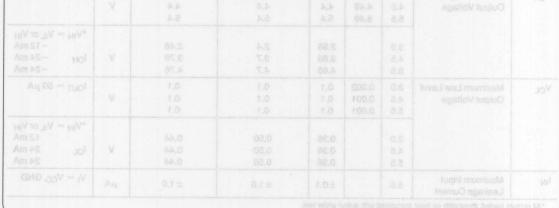
Z = HIGH Impedance

✓ = LOW-to-HIGH Clock Transition

### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



PDIP

### **Absolute Maximum Rating (Note 1)**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| U  | ttice/Distributors for availab                        | ility and specifications.       |
|----|---|---------------------------------|
| S  | upply Voltage (V <sub>CC</sub> )                      | -0.5V to $+7.0V$                |
| D  | C Input Diode Current (IIK)                           |                                 |
|    | $V_1 = -0.5V$   | -20 mA                          |
|    | $V_I = V_{CC} + 0.5V$                                 | + 20 mA                         |
| D  | C Input Voltage (V <sub>I</sub> )                     | $-0.5V$ to $V_{CC} + 0.5V$      |
| D  | C Output Diode Current (IOK)                          |                                 |
|    | $V_0 = -0.5V$   | -20 mA                          |
|    | $V_O = V_{CC} + 0.5V$                                 | + 20 mA                         |
| D  | C Output Voltage (V <sub>O</sub> )                    | $-0.5$ V to to $V_{CC} + 0.5$ V |
| D  | C Output Source                                       |                                 |
|    | or Sink Current (I <sub>O</sub> )                     | ±50 mA                          |
| D  | C V <sub>CC</sub> or Ground Current                   |                                 |
|    | per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                          |
| S  | torage Temperature (T <sub>STG</sub> )                | -65°C to +150°C                 |
| Ji | unction Temperature (T,I)                             |                                 |
|    | CDIP  | 175°C                           |
|    |   |                                 |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Recommended Operating and San Conditions

| Supply Voltage (V <sub>CC</sub> )      |        |      |                       |
|--|--------|------|-----------------------|
| 'AC                                    |        |      | 2.0V to 6.0V          |
| ACT and form fact a                    |        |      | 4.5V to 5.5V          |
| Input Voltage (V <sub>I</sub> )        |        |      | 01/ to 1/00           |
| Output Voltage (V <sub>O</sub> )       |        |      | 0V to V <sub>CC</sub> |
| Operating Temperature (TA              | )      |      |                       |
| 74AC/ACT                               |        | -40  | °C to +85°C           |
| 54AC/ACT                               |        | -55° | C to +125°C           |
| Minimum Input Edge Rate ( 'AC Devices  | ΔV/Δt) |      |                       |
| V <sub>IN</sub> from 30% to 70% of     | Vcc    |      |                       |
| V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V     | H      |      | 125 mV/ns             |
| Minimum Input Edge Rate ( 'ACT Devices | ΔV/Δt) |      |                       |
| V <sub>IN</sub> from 0.8V to 2.0V      |        |      |                       |
| V <sub>CC</sub> @ 4.5V, 5.5V           |        |      | 125 mV/ns             |

## **DC Characteristics for 'AC Family Devices**

|                 |                                      |                        | 74                      | AC                   | 54AC                             | 74AC                            |                |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|----------------------------------|---------------------------------|----------------|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units          | Conditions   |
|                 |                                      |                        | Тур                     |                      | Guaranteed Limits                |                                 |                | -+-0 <b-10< th=""></b-10<>   |
| VIH             | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | v              | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | Vo             | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | sib airlt fart | $I_{OUT} = -50 \mu\text{A}$  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | V              | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL}  or  V_{IH} \\ &- 12  mA \\ I_{OH} &- 24  mA \\ &- 24  mA \end{split}$ |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V              | $I_{OUT} = 50 \mu A$   |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | V              | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $V_{IOL}$ 24 mA   |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                             | ±1.0                            | μА             | $V_I = V_{CC}$ , GND   |

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'AC Family Devices (Continued)

|        |                            | 74AC             | 1                      | 74                     | AC   | 54AC                              |            | 74AC                            |    |  |  |
|--------|----------------------------|------------------|------------------------|------------------------|------|-----------------------------------|------------|---------------------------------|----|--|--|
| Symbol | winU                       | Parameter Age 20 | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |      | T <sub>A</sub> = -55°C to + 125°C | -40        | T <sub>A</sub> = -40°C to +85°C |    | Conditions   |  |
|        |                            |                  |                        | Тур                    | 10   | Guaranteed                        | Limits     |                                 |    |  |  |
| loz    | Maximum TRI-STATE® Current |                  | 5.5                    | ol .                   | ±0.5 | ±10.0                             | 07†<br>0S† | ±5.0                            |    | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I} = V_{CC}$ , GND<br>$V_{O} = V_{CC}$ , GND |  |
| IOLD   | †Min                       | imum Dynamic     | 5.5                    |                        | 3.7  | 50                                | 0.6        | 75                              | mA | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD   | Output Current             |                  | 5.5                    |                        | 2.7  | -50 A                             | 0.6        | -75                             | mA | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc    | 1111                       | mum Quiescent    | 5.5                    | t t                    | 8.0  | 160.0                             | 2.5        | 80.0                            | μА | $V_{IN} = V_{CC}$ or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## **DC Characteristics for 'ACT Family Devices**

| 8-5              | an 0.01 d.s                          | 0.8                    | 744               | ACT          | 54ACT                            | 74ACT                           | Sable III | %0 of 30  |  |
|------------------|--------------------------------------|------------------------|-------------------|--------------|----------------------------------|---------------------------------|-----------|---|--|
| Symbol           | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =  | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions  |  |
|                  |                                      |                        | Тур               | randever     | Guaranteed L                     | imits a marine                  | a# nr     | idenenO OA  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5        | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                      |  |
| VIL              | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5        | 0.8          | 308 + 0.8<br>30 08 - 0.8         | 0.8<br>(V) 0.8                  | Val       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                      |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49      | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V         | $I_{OUT} = -50 \mu\text{A}$   |  |
|                  | 1.5 ns 4.0 ns 4.0                    | 4.5<br>5.5             | 0.5<br>2.5<br>4.0 | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | OI-Ver    | $^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001    | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1<br>0.1                      | W S       | $I_{OUT} = 50 \mu A$  |  |
|                  |                                      | 4.5<br>5.5             |                   | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | VE.O.E VE | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $24 \text{ mA}$ $10L$ $24 \text{ mA}$ |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     | 5.5                    |                   | ±0.1         | ±1.0                             | ±1.0                            | μΑ        | $V_{I} = V_{CC}$ , GND  |  |
| loz              | Maximum TRI-STATE® Current           | 5.5                    |                   | ±0.5         | ±10.0                            | ±5.0                            | μА        | $V_{I} = V_{IL}, V_{IH}$<br>$V_{O} = V_{CC}, GND$                           |  |
| ICCT             | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6               |              | 1.6                              | 1.5                             | mA        | $V_I = V_{CC} - 2.1V$   |  |
| I <sub>OLD</sub> | †Minimum Dynamic                     | 5.5                    |                   |              | 50                               | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub> | Output Current                       | 5.5                    |                   |              | -50                              | -75                             | mA        | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc              | Maximum Quiescent<br>Supply Current  | 5.5                    |                   | 8.0          | 160.0                            | 80.0                            | μА        | V <sub>IN</sub> = V <sub>CC</sub> or GND                                    |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note:  $I_{\mbox{\footnotesize CC}}$  for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol           | Parameter                     | V <sub>CC</sub> * | ros-       | T <sub>A</sub> = +25°<br>C <sub>L</sub> = 50 pl | C           | to +       | -55°C<br>125°C<br>50 pF | to +       | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|------------------|-------------------------------|-------------------|------------|---|-------------|------------|-------------------------|------------|------------------------|-------|-------------|
|                  |                               |                   | Min        | Тур   | Max         | Min        | Max                     | Min        | Max                    |       |             |
| f <sub>max</sub> | Maximum Clock<br>Frequency    | 3.3<br>5.0        | 110<br>120 | 145<br>160                                      | £           | 95<br>100  | 6,6                     | 100<br>110 | tn                     | MHz   | 20          |
| t <sub>PLH</sub> | Propagation Delay<br>CP to On | 3.3<br>5.0        | 3.0<br>2.0 | 8.0<br>6.0                                      | 13.0<br>9.5 | 1.0<br>1.0 | 16.0<br>11.5            | 3.0<br>2.0 | 15.0<br>10.5           | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay<br>CP to On | 3.3<br>5.0        | 3.0<br>2.0 | 8.0<br>5.5                                      | 13.0<br>9.5 | 1.0<br>1.0 | 16.0<br>11.5            | 3.0        | 15.0<br>10.5           | ns    | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time            | 3.3<br>5.0        | 2.5<br>1.5 | 6.0<br>4.5                                      | 11.0        | 1.0        | 13.0<br>10.0            | 2.5        | 12.0<br>9.0            | ns    | 2-5         |
| t <sub>PZL</sub> | Output Enable Time            | 3.3<br>5.0        | 2.5<br>1.5 | 6.5<br>5.0                                      | 11.0<br>8.0 | 1.0        | 13.5<br>10.0            | 2.5<br>1.5 | 12.0<br>9.0            | ns    | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time           | 3.3<br>5.0        | 2.5<br>1.5 | 6.5<br>5.0                                      | 10.5<br>8.0 | 1.0        | 12.0<br>10.0            | 2.5<br>1.5 | 11.0<br>8.5            | ns    | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time           | 3.3<br>5.0        | 2.5        | 6.0<br>4.5                                      | 10.5<br>8.0 | 1.0<br>1.0 | 12.0<br>10.0            | 2.5<br>1.5 | 11.0<br>8.5            | ns    | 2-6         |

\*Voltage Range 3.3 is 3.3V ±0.3V Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                   | 2.0 V erVoc                                     |                   | 74.  | AC               | 54AC   | 74AC   | D hand | 1-83        |
|-------------------|---|-------------------|--|------------------|--|--|--------|-------------|
| Symbol            | Parameter 8.0                                   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |                  | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units  | Fig.<br>No. |
| - 50 jaA          | = ruol V  |                   | Тур  | Guaranteed Minir |  | mum  |        |             |
| ts<br>JajV to JaV | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 3.3<br>5.0        | -1.0<br>-1.0                                     | 1.5<br>1.5       | 2.5<br>2.5   | 1.5<br>1.5   | ns     | 2-7         |
| th                | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 3.3<br>5.0        | -1.0<br>-1.0                                     | 3.5<br>3.5       | 4.0<br>4.0   | 4.0<br>4.0   | ns     | 2-7         |
| t <sub>w</sub>    | CP Pulse Width<br>HIGH or LOW                   | 3.3<br>5.0        | 3.5<br>2.5                                       | 5.0<br>4.0       | 6.0<br>5.0   | 5.5<br>4.0   | ug ns  | 2-3         |

\*Voltage Range 3.3 is 3.3V  $\pm$ 0.3V Voltage Range 5.0 is 5.0V  $\pm$ 0.5V

| B |   |    |   | 1 |  |
|---|---|----|---|---|--|
|   |   |    |   |   |  |
|   |   | 9  | r | 1 |  |
|   |   | ۲, | t | 1 |  |
|   | r | a  | ۰ | , |  |
|   |   |    |   |   |  |

| Symbol           | Parameter                                 | (V) |     | C <sub>L</sub> = 50 p | F    | -   | 125°C<br>50 pF | to come to the discountry of | 85°C<br>50 pF | Units | No.    |
|------------------|---|-----|-----|-----------------------|------|-----|----------------|------------------------------|---------------|-------|--------|
|                  |   |     | Min | Тур                   | Max  | Min | Max            | Min                          | Max           | 01    | 18.0   |
| f <sub>max</sub> | Maximum Clock<br>Frequency                | 5.0 | 120 | 150                   |      | 85  |                | 110                          | eluner        | MHz   |        |
| t <sub>PLH</sub> | Propagation Delay<br>CP to O <sub>n</sub> | 5.0 | 2.0 | 6.0                   | 9.5  | 1.0 | 11.5           | 1.5                          | 10.5          | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>CP to On             | 5.0 | 2.5 | 6.0                   | 9.5  | 1.0 | 11.5           | 2.0                          | 10.5          | ns    | 2-3, 4 |
| tpzH             | Output Enable Time  OE to On              | 5.0 | 2.5 | 7.0                   | 10.5 | 1.0 | 12.5           | 2.0                          | 11.5          | ns    | 2-5    |
| t <sub>PZL</sub> | Output Enable Time OE to On               | 5.0 | 2.5 | 7.0                   | 10.5 | 1.0 | 13.0           | 2.0                          | 12.0          | ns    | 2-6    |
| t <sub>PHZ</sub> | Output Disable Time OE to On              | 5.0 | 1.5 | 7.5                   | 12.0 | 1.0 | 13.5           | 1.0                          | 13.0          | ns    | 2-5    |
| t <sub>PLZ</sub> | Output Disable Time OE to On              | 5.0 | 1.5 | 7.0                   | 10.5 | 1.0 | 12.5           | 1.0                          | 11.5          | ns    | 2-6    |

\*Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                | 10-422 51-10                                    |                       |      |     | 54ACT  | 74ACT   | 0,020,0 | 00   |
|----------------|---|-----------------------|------|-----|--|---|---------|------|
| Symbol         | Parameter B - 20                                | V <sub>CC</sub> * (V) |      |     | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to +85°C<br>$C_L = 50 \text{ pF}$ | Units   | Fig. |
|                |   |                       | Тур  |     | Guaranteed Min   | imum  |         |      |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0                   | 2.5  | 2.0 | 4.0  | 2.5   | ns      | 2-7  |
| t <sub>h</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 5.0                   | -0.5 | 2.0 | 3.0  | 2.5   | ns      | 2-7  |
| t <sub>w</sub> | CP Pulse Width<br>HIGH or LOW                   | 5.0                   | 3.0  | 4.5 | 6.0  | 5.5   | ns      | 2-3  |

\*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions                 |
|-----------------|----------------------------------|------|-------|----------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$            |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 35.0 | pF    | V <sub>CC</sub> = 5.0V     |
| 30回发            | M, IFO CINS                      |      |       |                            |
|                 |                                  |      |       |                            |
|                 |                                  |      |       | Data Inputs<br>Data Outper |



## 54ACT/74ACT823 9-Bit D Flip-Flop

### **General Description**

The 'ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The 'ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

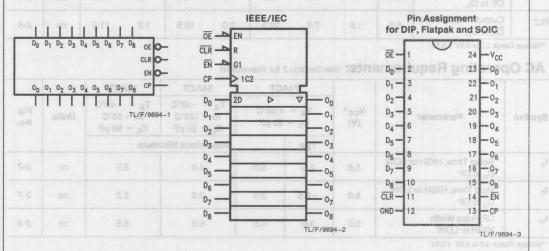
#### **Features**

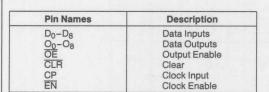
- Outputs source/sink 24 mA
- TRI-STATE® outputs for bus interfacing
- Inputs and outputs are on opposite sides
- 'ACT823 has TTL-compatible inputs

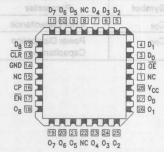
Ordering Code: See Section 8

#### **Logic Symbols**

## **Connection Diagrams**







Pin Assignment for LCC

TL/F/9894-4

## Functional Description

The 'ACT823 consists of nine D-type edge-triggered flipflops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ( $\overline{\text{OE}}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{\text{OE}}$  LOW, the contents of the flip-flops are available at the outputs. When  $\overline{\text{OE}}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{\text{OE}}$  input does not affect

the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear (CLR) and Clock Enable (EN) pins. These devices are ideal for parity bus interfacing in high performance systems.

When  $\overline{\text{CLR}}$  is LOW and  $\overline{\text{OE}}$  is LOW, the outputs are LOW. When  $\overline{\text{CLR}}$  is HIGH, data can be entered into the flip-flops. When  $\overline{\text{EN}}$  is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the  $\overline{\text{EN}}$  is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

**Function Table** 

|            |     | Inputs |        | (m from 30%) | Intern | al       | Output           | Function        | OV) egatloV tuqtuO OC   |
|------------|-----|--------|--------|--------------|--------|----------|------------------|-----------------|---|
| ŌĒ         | CLR | EN     | СР     | D            | Q      | Pun      | 0                | (Qualitation) X | OC Output Source er Sin<br>OC Voc. or Ground Cur                    |
| Н          | X   | L      | 5      | ACT Devices  | L      | Am       | Da ± Z           | High Z          | par Output Pin (log of  |
| Н          | X   | L      | V05/01 | / IrHn 0.8V  | Н      | 0.0      | 1 - Z            | High Z          | Storage Temperature (T  |
| 125 rHV/0s | L   | X      | X      | X            | L      |          | Z                | Clear           | Janutereame Tinoconst   |
| L          | L   | X      | X      | X            | L      | orar     | L                | Clear           | 9100  |
| Н          | Н   | Н      | X      | X            | NC     | 0.00     | Z                | Hold            | 9109  |
| L          | Н   | Н      | X      | X            | NC     | egan     | NC               | Hold            | ter mumicam etiloedă il efoli                                       |
| Н          | Н   | L      | 5      | L            | L      | tuorti   | should Zo met, w | Load            | t eriT audoo yem ediveb eril ci                                     |
| Н          | Н   | L      | _      | н            | Н      | -driving | Z                | Load            | exception, to ensure that the element comparative, and output/input |
| L          | Н   | L      | 5      | L            | L      |          | a rota Toega     | Load            | nand operation of FACTIN or   |
| L          | Н   | L      | 5      | н            | Н      |          | Н                | Load            |   |
|            |     |        |        |              |        |          | 6311             | ELISTUS IST     | OC Electrical C   |

H = HIGH Voltage Level

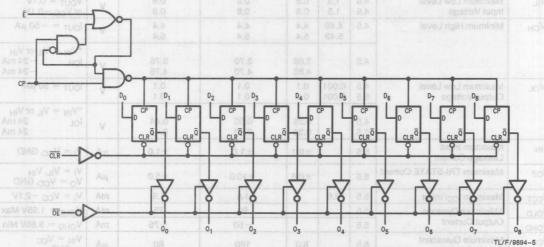
L = LOW Voltage Level

X = Immaterial

Z = High Impedance = LOW-to-HIGH Transition

NC = No Change

## **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| Supply Voltage (V <sub>CC</sub> )  |                       | -0.5                   | V to 7.0V | ACT                            |
|--|-----------------------|------------------------|-----------|--------------------------------|
| DC IIIput Diode Current (IIK)  |                       |                        |           | Input Volta                    |
| $V_1 = V_{CC} + 0.5V$  |                       |                        | + 20 mA   | Output Vo                      |
| DC Input Voltage (V <sub>I</sub> )   | HDIH-ot-              | 0.5V to V <sub>C</sub> | c + 0.5V  | Operating 74AC/A               |
| DC Output Diode Current (I <sub>OK</sub> )   |                       |                        | -20 mA    | 54AC/A                         |
| $V_{O} = -0.5V$<br>$V_{O} = V_{CC} + 0.5V$   |                       |                        | +20 mA    | Minimum 'AC Dev                |
| DC Output Voltage (V <sub>O</sub> )  | _                     | 0.5V to VC             | + 0.5V    | V <sub>IN</sub> from           |
| DC Output Source or Sink Curre   | ent (I <sub>O</sub> ) |                        | ±50 mA    | V <sub>CC</sub> @ 3            |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) |                       |                        | ±50 mA    | Minimum<br>'ACT De             |
|  |                       | -65°C to               | +150°C    | V <sub>IN</sub> from           |
| Junction Temperature (T,I)   |                       |                        |           | V <sub>CC</sub> @ <sup>2</sup> |
| CDIP   |                       |                        | 175°C     |                                |
| PDIP   |                       |                        | 140°C     |                                |
| Note 1: Absolute maximum ratings are   | those value           | es beyond whi          | ch damage |                                |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

| ACT (E) oldsnil furgio boneflur  | 4.5V IO 5.5V          |
|--|-----------------------|
| Input Voltage (V <sub>I</sub> )  | 0V to V <sub>CC</sub> |
| Output Voltage (Vo)  | 0V to V <sub>CC</sub> |
| Operating Temperature (T <sub>A</sub> ) 74AC/ACT 54AC/ACT                                | -40°C to +85°C        |
| Minimum Input Edge Rate (ΔV/Δt) 'AC Devices  |                       |
| V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub><br>V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V | 125 mV/ns             |
| Minimum Input Edge Rate (ΔV/Δt) 'ACT Devices   |                       |
| V <sub>IN</sub> from 0.8V to 2.0V  |                       |
| V <sub>CC</sub> @ 4.5V, 5.5V   | 125 mV/ns             |
|  |                       |

### **DC Electrical Characteristics**

|                 | Parameter                           |                        | 74               | ACT          | 54ACT                            | 74ACT                           |       | L = LOW Voltage Levi   |
|-----------------|-------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|-------|--|
| Symbol          |                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | 25°C         | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |
|                 |                                     |                        | Тур              |              | Guaranteed L                     | imits                           |       | NC - No Change   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage  | 4.5<br>4.5             | 1.5<br>1.5       | 0.8<br>0.8   | 0.8<br>0.8                       | 0.8<br>0.8                      | ٧     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> -0.1V  |
| V <sub>OH</sub> | Minimum High Level                  | 4.5                    | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V     | $I_{OUT} = -50 \mu\text{A}$  |
|                 |                                     | 4.5                    |                  | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| V <sub>OL</sub> | Maximum Low Level Output Voltage    | 4.5<br>5.5             | 0.001<br>0.001   | 0.1          | 0.1<br>0.1                       | 0.1<br>0.1                      | ٧     | $I_{OUT} = 50 \mu A$   |
|                 |                                     | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | ٧     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current    | 5.5                    | -                | ±0.1         | ±1.0                             | ±1.0                            | μА    | $V_I = V_{CC}$ , GND   |
| loz             | Maximum TRI-STATE Current           | 5.5                    | cl <sub>Z</sub>  | ±0.5         | ± 10.0                           | ±5.0                            | μΑ    | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |
| ICCT            | Maximum I <sub>CC</sub> /Input      | 5.5                    | 0.6              | 8            | 1.6                              | 1.5                             | mA    | $V_I = V_{CC} - 2.1V$  |
| IOLD            | †Minimum Dynamic                    | 5.5                    |                  | -            | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max   |
| IOHD            | Output Current                      | 5.5                    | 10               | 10           | -50                              | <del>-</del> 75                 | mA    | V <sub>OHD</sub> = 3.85V Min   |
| Icc see         | Maximum Quiescent<br>Supply Current | 5.5                    | and site         | 8.0          | 160                              | 80                              | μΑ    | V <sub>IN</sub> = V <sub>CC</sub> or GND   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Symbol           | Parameter                      | V <sub>CC</sub> * |     | C <sub>L</sub> = 50p |      |     | 125°C<br>50 pF |     | 85°C<br>50 pF | Units   | Fig.   |
|------------------|--------------------------------|-------------------|-----|----------------------|------|-----|----------------|-----|---------------|---------|--------|
|                  |                                |                   | Min | Тур                  | Max  | Min | Max            | Min | Max           | A 1 300 | D-02   |
| f <sub>max</sub> | Maximum Clock<br>Frequency     | 5.0               | 120 | 158                  |      | 95  |                | 109 | m-qu          | MHz     | 101-0  |
| t <sub>PLH</sub> | Propagation Delay<br>CP to On  | 5.0               | 1.5 | 5.5                  | 9.5  | 1.0 | 12.0           | 1.5 | 10.5          | ns      | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>CP to On  | 5.0               | 2.0 | 5.5                  | 9.5  | 1.0 | 12.0           | 1.5 | 10.5          | ns      | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>CLR to On | 5.0               | 2.5 | 8.0                  | 13.5 | 1.0 | 18.0           | 2.0 | 15.5          | ns      | 2-3, 4 |
| t <sub>PZH</sub> | Output Enable Time OE to On    | 5.0               | 1.5 | 6.0                  | 10.5 | 1.0 | 11.5           | 1.5 | 11.5          | ns      | 2-5    |
| t <sub>PZL</sub> | Output Enable Time             | 5.0               | 2.0 | 6.5                  | 11.0 | 1.0 | 12.0           | 1.5 | 12.0          | ns      | 2-6    |
| t <sub>PHZ</sub> | Output Disable Time            | 5.0               | 1.5 | 6.5                  | 11.0 | 1.0 | 13.5           | 1.5 | 12.0          | ns      | 2-5    |
| t <sub>PLZ</sub> | Output Disable Time OE to On   | 5.0               | 1.5 | 6.0                  | 10.5 | 1.0 | 12.0           | 1.5 | 11.5          | ns      | 2-6    |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                  | 062-12 23-063                                  |                   | 744  | СТ  | 54ACT  | 74ACT  |           | 230 3- |
|------------------|--|-------------------|--|-----|--|--|-----------|--------|
| Symbol           | Parameter Parameter                            | V <sub>CC</sub> * | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |     | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units     | Fig.   |
|                  | 20 -07   |                   | Тур  |     | Guaranteed Min   | imum   | 0 10 10 0 |        |
| t <sub>S</sub>   | Setup Time, HIGH or LOW<br>D to CP             | 5.0               | 0.5  | 2.5 | 4.0  | 2.5  | ns        | 2-7    |
| t <sub>h</sub>   | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0               | 0  | 2.5 | 3.0  | 2.5  | ns        | 2-7    |
| t <sub>s</sub>   | Setup Time, HIGH or LOW<br>EN to CP            | 5.0               | 0  | 2.0 | 4.0  | 2.5  | ns        | 2-7    |
| t <sub>h</sub>   | Hold Time, HIGH or LOW<br>EN to CP             | 5.0               | 0  | 1.0 | 3.0  | 1.0  | ns        | 2-7    |
| t <sub>w</sub>   | CP Pulse Width<br>HIGH or LOW                  | 5.0               | 2.5  | 4.5 | 6.0  | 5.5  | ns        | 2-3    |
| t <sub>w</sub>   | CLR Pulse Width, LOW                           | 5.0               | 3.0  | 5.5 | 7.0  | 5.5  | ns        | 2-3    |
| t <sub>rec</sub> | CLR to CP<br>Recovery Time                     | 5.0               | 1.5  | 3.5 | 4.5  | 4.0  | ns        | 2-3, 7 |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol          | Parameter                        | Тур | Units | Conditions             |
|-----------------|----------------------------------|-----|-------|------------------------|
| CIN             | Input Capacitance                | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 44  | pF    | V <sub>CC</sub> = 5.0V |



## 54ACT/74ACT825 8-Bit D Flip-Flop

## **General Description**

The 'ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The 'ACT825 has noninverting outputs and is fully compatible with AMD's Am29825.

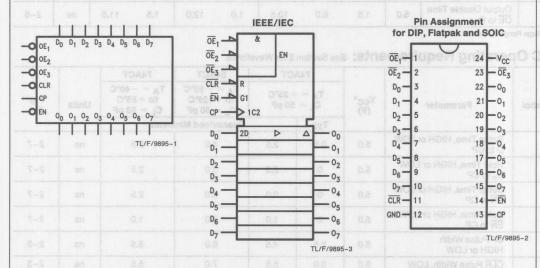
#### **Features**

- Outputs source/sink 24 mA
- Inputs and outputs are on opposite sides
  - 'ACT825 has TTL-compatible inputs

Ordering Code: See Section 8

## **Logic Symbols**

#### **Connection Diagrams**



| Pin Names   | Description                             |  |                                     | Pin Assignment for LCC  | UO I  |
|---|---|--|-------------------------------------|---|---|
| $D_0-D_7$ $O_0-O_7$ $\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$ | Data Inputs Data Outputs Output Enables |  |                                     | D <sub>6</sub> D <sub>5</sub> D <sub>4</sub> NC D <sub>3</sub> D <sub>2</sub> D <sub>1</sub> 11 10 9 8 7 6 5      | age Renge 5.5   |
| EN  | Clock Enable                            |  | D <sub>7</sub> 12                   | 900   | 4 D <sub>0</sub>  |
| CLR   | Clear                                   |  | CLR 13 GND 14                       | manus   | 3 OE <sub>2</sub>   |
| CP  | Clock Input                             |  | NC 15                               | Input Capu  | 2 0E <sub>1</sub>   |
|   |   |  | CP 16<br>EN 17<br>0 <sub>7</sub> 18 | Power Dis<br>Capacitan  | 28 V <sub>CC</sub><br>27 OE <sub>3</sub><br>26 O <sub>0</sub> |
|   |   |  | 7/2                                 | 19 20 21 22 23 24 25 0 <sub>6</sub> 0 <sub>5</sub> 0 <sub>4</sub> NC 0 <sub>3</sub> 0 <sub>2</sub> 0 <sub>1</sub> |   |
|   |   |  |                                     | Т   | L/F/9895-4  |

## Functional Description

The 'ACT825 consists of eight D-type edge-triggered flipflops. These devices have TRI-STATE® outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{OE}_1$ ,  $\overline{OE}_2$  and  $\overline{OE}_3$  LOW, the contents of the flip-flops are available at the outputs. When one of  $\overline{OE}_1$ ,  $\overline{OE}_2$  or  $\overline{OE}_3$  is HIGH, the outputs go to the high impedance state.

Operation of the  $\overline{\text{OE}}$  input does not affect the state of the flip-flops. The 'ACT825 has Clear ( $\overline{\text{CLR}}$ ) and Clock Enable ( $\overline{\text{EN}}$ ) pins. These pins are ideal for parity bus interfacing in high performance systems.

When CLR is LOW and OE is LOW, the outputs are LOW. When CLR is HIGH, data can be entered into the flip-flops. When EN is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When EN is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

**Function Table** 

|            |     | Inputs | 4.5V, 5.5V | Ve.s m as    | Internal | Output   | Function |
|------------|-----|--------|------------|--------------|----------|----------|----------|
| ŌĒ         | CLR | EN 4   | СР         | Dn           | Q Q      | 0        | runction |
| Н          | X   | L      | VO SEV     | B.O. nLmt.us | L con    | Z        | High-Z   |
| 125 rH//ns | X   | L      | -√a.a      | Va H         | H        | Z        | High-Z   |
| H          | L   | X      | X          | X            | L one    | Z        | Clear    |
| L          | L   | X      | X          | X            | L on     | L        | Clear    |
| Н          | Н   | Н      | X          | X            | NC       | Z        | Hold     |
| L          | Н   | Н      | X          | X            | NC       | NC       | Hold     |
| Н          | Н   | L      | _          | L            | L viga   | Z 1840 8 | Load     |
| Н          | Н   | L      | _          | H            | Н        | Z        | Load     |
| L          | Н   | L      | _          | L            | L        | L        | Load     |
| L          | Н   | L      | _          | Н            | Н        | Holte    | Load     |

H = HIGH Voltage Level L = LOW Voltage Level

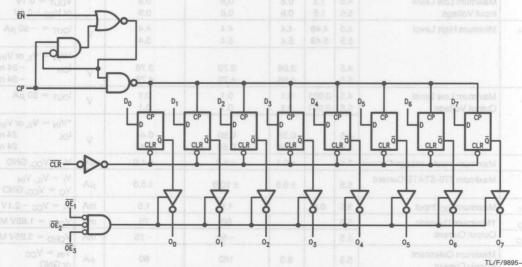
X = Immaterial

Z = High Impedance

= LOW-to-HIGH Transition

NC = No Change

## **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

4-305

| Do Input Diode Current (IIK)                          |                                |
|---|--------------------------------|
| $V_1 = -0.5V$   | -20 mA                         |
| $V_1 = V_{CC} + 0.5V$                                 | + 20 mA                        |
| DC Input Voltage (V <sub>I</sub> )                    | -0.5V to V <sub>CC</sub> +0.5V |
| DC Output Diada Current (1-1)                         |                                |
| $V_0 = -0.5V$   | -20 mA                         |
| $V_O = V_{CC} + 0.5V$                                 | + 20 mA                        |
| DC Output Voltage (V <sub>O</sub> )                   | +0.5V                          |
| DC Output Source or Sink Current (IO)                 | ± 50 mA                        |
| DC V <sub>CC</sub> or Ground Current                  |                                |
| Per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                         |
| Storage Temperature (T <sub>STG</sub> )               | -65°C to +150°C                |
| Junction Temperature (T <sub>.j</sub> )               |                                |
| CDIP  | 175°C                          |
| PDIP  | 140°C                          |
| Note 1: Absolute maximum ratings are those value      | ies hevond which damage        |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

| No.1   | KILLO YELEN | 4.5V to 5.5V                |
|--|-------------|-----------------------------|
| Input Voltage (V <sub>I</sub> )  |             | OV to V <sub>CC</sub>       |
| Output Voltage (V <sub>O</sub> )   |             | OV to Vcc                   |
| Operating Temperature (T <sub>A</sub> )<br>74AC/ACT<br>54AC/ACT  | -40<br>-55° | 0°C to +85°C<br>C to +125°C |
| Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'AC Devices $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @ 3.3V, 4.5V, 5.5V |             | 125 mV/ns                   |
| Minimum Input Edge Rate (ΔV/Δt)  |             |                             |
| 'ACT Devices V <sub>IN</sub> from 0.8V to 2.0V V <sub>CC</sub> @ 4.5V, 5.5V  |             | 125 mV/ns                   |
|  |             |                             |

## **DC Electrical Characteristics**

|                  | Parameter                           | 9.19                   | 74               | ACT          | 54ACT                             | 74ACT                           | lei<br>le       | au apaliov HOH = H  |
|------------------|-------------------------------------|------------------------|------------------|--------------|-----------------------------------|---------------------------------|-----------------|---|
| Symbol           |                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | 25°C         | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units           | Conditions  |
|                  |                                     |                        | Тур              |              | Guaranteed Li                     | mits                            | *1,002131111111 | NC - No Change  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage | 4.5<br>5.5             | 1.5<br>1.5       | 2.0          | 2.0<br>2.0                        | 2.0<br>2.0                      | ٧               | $V_{OUT} = 0.1V$<br>or $V_{CC} = 0.1V$  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8<br>0.8                        | 0.8                             | and the same of | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub>  | Minimum High Level                  | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧               | $I_{OUT} = -50 \mu\text{A}$   |
|                  |                                     | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | V               | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $_{OH} -24 \text{ mA}$ $_{-24 \text{ mA}}$   |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage    | 4.5<br>5.5             | 0.001<br>0.001   | 0.1          | 0.1<br>0.1                        | 0.1<br>0.1                      | ٧               | $I_{OUT} = 50 \mu A$  |
|                  | - Cap   Cap   Cap                   | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | V               | $\label{eq:VIN} \begin{split} ^*\text{V}_{\text{IN}} &= \text{V}_{\text{IL}}  \text{or}  \text{V}_{\text{IH}} \\ \text{I}_{\text{OL}} & 24  \text{mA} \\ & 24  \text{mA} \end{split}$ |
| I <sub>IN</sub>  | Maximum Input Leakage Current       | 5.5                    |                  | ±0.1         | ±1.0                              | ±1.0                            | μΑ              | $V_I = V_{CC}$ , GND  |
| loz              | Maximum TRI-STATE Current           | 5.5                    | 4                | ± 0.5        | ± 10.0                            | ±5.0                            | μΑ              | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |
| ГССТ             | Maximum I <sub>CC</sub> /Input      | 5.5                    | 0.6              |              | 1.6                               | 1.5                             | mA              | $V_I = V_{CC} - 2.1V$   |
| IOLD             | †Minimum Dynamic                    | 5.5                    |                  | 1            | 50                                | 75                              | mA              | V <sub>OLD</sub> = 1.65V Max  |
| I <sub>OHD</sub> | Output Current                      | 5.5                    | 10               |              | -50                               | -75                             | mA              | V <sub>OHD</sub> = 3.85V Min  |
| Icc              | Maximum Quiescent<br>Supply Current | 5.5                    |                  | 8.0          | 160                               | 80                              | μΑ              | $V_{IN} = V_{CC}$ or GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>CC</sub> limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|   | л   |
|---|-----|
| W | -   |
|   | - 4 |

| Symbol           | Parameter                     | V <sub>CC</sub> * |     | r <sub>A</sub> = +25°<br>C <sub>L</sub> = 50 p |       | to + | −55°C<br>125°C<br>50 pF | to + | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|------------------|-------------------------------|-------------------|-----|--|-------|------|-------------------------|------|------------------------|-------|-------------|
| atue             | aturati                       | 10 6              | Min | Тур  | Max   | Min  | Max                     | Min  | Max                    | T HIS | 3-01        |
| f <sub>max</sub> | Maximum Clock<br>Frequency    | 5.0               | 120 | 158  | na li | 95   |                         | 109  | telena                 | MHz   | anat        |
| t <sub>PLH</sub> | Propagation Delay<br>CP to On | 5.0               | 1.5 | 5.5  | 9.5   | 1.0  | 11.5                    | 1.5  | 10.5                   | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay CP to On    | 5.0               | 2.0 | 5.5  | 9.5   | 1.0  | 11.5                    | 1.5  | 10.5                   | ns    | 2-3, 4      |
| t <sub>PHL</sub> | Propagation Delay CLR to On   | 5.0               | 2.5 | 8.0  | 13.5  | 1.0  | 18.0                    | 2.0  | 15.5                   | ns    | 2-3, 4      |
| t <sub>PZH</sub> | Output Enable Time            | 5.0               | 1.5 | 6.0  | 10.5  | 1.0  | 11.5                    | 1.5  | 11.5                   | ns    | 2-5         |
| t <sub>PZL</sub> | Output Enable Time            | 5.0               | 2.0 | 6.5  | 11.0  | 1.0  | 12.5                    | 1.5  | 12.0                   | ns    | 2-6         |
| t <sub>PHZ</sub> | Output Disable Time OE to On  | 5.0               | 1.5 | 6.5  | 11.0  | 1.0  | 13.5                    | 1.5  | 12.0                   | ns    | 2-5         |
| t <sub>PLZ</sub> | Output Disable Time           | 5.0               | 1.5 | 6.0  | 10.5  | 1.0  | 13.0                    | 1.5  | 11.5                   | ns    | 2-6         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements: See Section 2 for Waveforms

|                  | 03-3 20-03                                       |                          | 744 | CT              | 54ACT   | 74ACT  | Units | The second  |
|------------------|--|--------------------------|-----|-----------------|---|--|-------|-------------|
| Symbol           | 80-81 Parameter 7-88<br>80-71 8-80<br>70-81 8-80 | V <sub>CC</sub> *<br>(V) |     | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |       | Fig.<br>No. |
|                  |  |                          | Тур |                 | Guaranteed Min  | imum   |       |             |
| t <sub>s</sub>   | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 5.0                      | 0.5 | 2.5             | 4.0   | 2.5  | ns    | 2-7         |
| th               | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP   | 5.0                      | 0   | 2.5             | 3.0   | 2.5  | ns    | 2-7         |
| ts               | Setup Time, HIGH or LOW<br>EN to CP              | 5.0                      | 0   | 2.0             | 4.0   | BinG 2.5   | ns    | 2-7         |
| th               | Hold Time, HIGH or LOW<br>EN to CP               | 5.0                      | 0   | 1.0             | 3.0   | gtuO 1.0   | ns    | 2-7         |
| t <sub>w</sub>   | CP Pulse Width<br>HIGH or LOW                    | 5.0                      | 2.5 | 4.5             | 6.0   | 5.5  | ns    | 2-3         |
| tw               | CLR Pulse Width, LOW                             | 5.0                      | 3.0 | 5.5             | 7.0   | 5.5  | ns    | 2-3         |
| t <sub>rec</sub> | CLR to CP<br>Recovery Time                       | 5.0                      | 1.5 | 3.5             | 4.5   | 4.0  | ns    | 2-3, 7      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol          | Parameter                        | Тур | Units | Conditions             |
|-----------------|----------------------------------|-----|-------|------------------------|
| CIN             | Input Capacitance                | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 44  | pF    | V <sub>CC</sub> = 5.0V |



# 54ACT/74ACT841 10-Bit Transparent Latch with TRI-STATE® Outputs

#### **General Description**

The 'ACT841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'ACT373.

#### **Features**

■ 'ACT841 has TTL-compatible inputs

AC Electrical Characteristics: See Section 2 for Waveforms

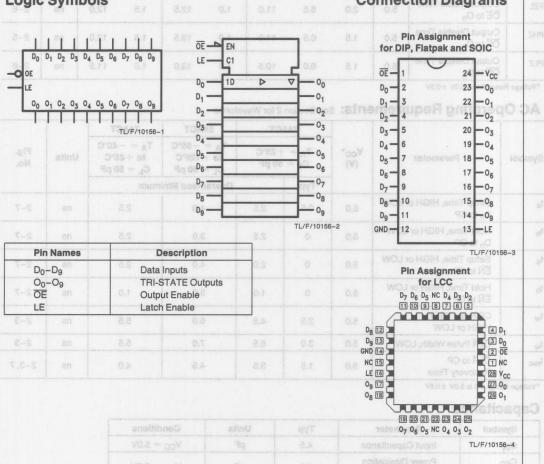
- Outputs source/sink 24 mA
- Non-inverting TRI-STATE outputs

Ordering Code: See Section 8

### **Logic Symbols**

#### **Connection Diagrams**

Symbol



## **Functional Description**

The ACT841 consists of ten D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition.

On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable  $(\overline{OE})$  is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state.

#### **Function Table**

|           | Inputs |      | Internal         | Output        | Function    |  |  |
|-----------|--------|------|------------------|---------------|-------------|--|--|
| OE OF     | LE D   |      | Q                | OALD/OY       | Tunotion    |  |  |
| X         | X      | X    | X                | Z             | High Z      |  |  |
| Н         | Н      | E    | it sieu Sabatina | Z             | High Z      |  |  |
| Н         | Н      | H    | to sepHot sept   | Z             | High Z      |  |  |
| 125 tH//m | L      | X    | ALC:             | S O Z         | Latched     |  |  |
| L         | Н      | 6LAV | Later Links to   | int munuLesta | Transparent |  |  |
| L         | Н      | Н    | H 283            | ved THV       | Transparent |  |  |
| L         | L      | X    | VINC VE          | NC NC         | Latched     |  |  |

H = HIGH Voltage Level

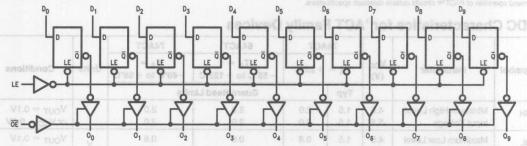
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

## **Logic Diagram**



TL/F/10156-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays.

|  |   |      | 8,4          | 6.4  |     | Output Voltage                       |  |
|--|---|------|--------------|------|-----|--------------------------------------|--|
| $^{*}V_{IM} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$ | v |      | 3.70<br>4.70 |      |     |                                      |  |
|  |   |      |              | 1.0  | 4.5 |                                      |  |
| $^{\circ}V_{IIV} = V_{II}.$ or $V_{IIH}$ 24 mA $^{\circ}O_{L}$ 24 mA       |   | 0.44 |              |      | 4.6 | Output Voltage                       |  |
|  |   |      | 0.f±         |      |     |                                      |  |
| $V_0 = V_{1L}, V_{1H}$   |   |      |              | 8.0± |     | Maximum TRI-STATE<br>Leakage Current |  |
| $V_{i} = V_{GO} - 2.1V$  |   | 1.5  |              |      |     |                                      |  |

Ar outputs loaded; stresholds on input associated with output to Marylmann test duration 2.0 ms one output travial at a line. CDIP

**PDIP** 

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office, Distributors for availability                 |                                |
|---|--------------------------------|
| Supply Voltage (V <sub>CC</sub> )                     | -0.5V to +7.0V                 |
| DC Input Diode Current (I <sub>IK</sub> )             |                                |
| $V_1 = -0.5V$   | -20 mA                         |
| $V_I = V_{CC} + 0.5V$                                 | + 20 mA                        |
| DC Input Voltage (V <sub>I</sub> )                    | $-0.5$ V to $V_{CC}$ + $0.5$ V |
| DC Output Diode Current (IOK)                         |                                |
| $V_0 = -0.5V$   | -20 mA                         |
| $V_O = V_{CC} + 0.5V$                                 | + 20 mA                        |
| DC Output Voltage (V <sub>O</sub> )                   | $-0.5$ V to $V_{CC}$ + $0.5$ V |
| DC Output Source                                      |                                |
| or Sink Current (IO)                                  | ±50 mA                         |
| DC V <sub>CC</sub> or Ground Current                  |                                |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                         |
| Storage Temperature (T <sub>STG</sub> )               | -65°C to +150°C                |
| Junction Temperature (T <sub>.i</sub> )               |                                |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Recommended Operating and Joseph Conditions

| Supply Voltage (V <sub>CC</sub> ) 'AC   |                 | Hei (El) e | 2.0V to 6.0V          |
|---|-----------------|------------|-----------------------|
| ACT at at also out ewello               |                 |            | 4.5V to 5.5V          |
| Input Voltage (V <sub>I</sub> )         |                 |            | 0V to V <sub>CC</sub> |
| Output Voltage (V <sub>O</sub> )        |                 |            | OV to VCC             |
| Operating Temperature (T <sub>A</sub> ) |                 | stugal     |                       |
| 74AC/ACT                                |                 | -40°       | C to +85°C            |
| 54AC/ACT                                |                 | -55°C      | to + 125°C            |
| Minimum Input Edge Rate (Δ 'AC Devices  | V/Δt)           | H          | Ĥ                     |
| V <sub>IN</sub> from 30% to 70% of V    | CC              |            | H                     |
| V <sub>CC</sub> @ 3.3V, 4.5V, 5.5V      | OO X            |            | 125 mV/ns             |
| Minimum Input Edge Rate (Δ              | V/ $\Delta t$ ) |            | 1 1                   |
| 'ACT Devices                            | H               |            | 1 4                   |
| V <sub>IN</sub> from 0.8V to 2.0V       | X               |            |                       |
| V <sub>CC</sub> @ 4.5V, 5.5V            |                 |            | 125 mV/ns             |
|   |                 |            |                       |

Z - High Impedance NC - No Change

## DC Characteristics for 'ACT Family Devices

|                 | Parameter                            |                        | 74               | ACT          | 54ACT                            | 74ACT                           |       |   |  |
|-----------------|--------------------------------------|------------------------|------------------|--------------|----------------------------------|---------------------------------|-------|---|--|
| Symbol          |                                      | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |  |
| Å               |                                      | 1                      | Тур              |              | Guaranteed Lin                   | nits                            | T.    | 4-0< -1   |  |
| V <sub>IH</sub> | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   | 2.0<br>2.0                       | 2.0<br>2.0                      | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| VIT so          | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8<br>0.8                       | 0.8                             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | ٧     | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 |                                      | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1<br>0.1                      | ٧     | $I_{OUT} = 50 \mu A$  |  |
|                 |                                      | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OL}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | ±1.0                             | ±1.0                            | μА    | $V_I = V_{CC}$ , GND  |  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                  | ±0.5         | ±10.0                            | ±5.0                            | μА    | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| ГССТ            | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |              | 1.6                              | 1.5                             | μΑ    | $V_{\rm I} = V_{\rm CC} - 2.1V$   |  |

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Capacitance

## DC Characteristics for 'ACT Family Devices (Continued) Manual Devices (Continued)

|        | 74ACT                               |                        | 74ACT T <sub>A</sub> = +25°C |       | 54ACT  T <sub>A</sub> = -55°C to +125°C |               | 74ACT |                              |       |  |  |
|--------|-------------------------------------|------------------------|------------------------------|-------|---|---------------|-------|------------------------------|-------|--|--|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) |                              |       |   |               | -40   | T <sub>A</sub> = °C to +85°C | Units | Conditions                               |  |
|        |                                     |                        | Тур                          | 79    |   | Guaranteed Li | mits  |                              |       |  |  |
| IOLD   | †Minimum Dynamic                    | 5.5                    | boolms                       | tisuD |   | 50            |       | 75                           | mA    | V <sub>OLD</sub> = 1.65V Max             |  |
| IOHD   | Output Current                      | 5.5                    | 0.8                          |       | 8.0                                     | -50           | 5.0   | -75 TO HE                    | mA    | V <sub>OHD</sub> = 3.85V Min             |  |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | 2.0                          | 8.0   | 2.0                                     | 160.0         | 5.0   | 80.0 DJ to P                 | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

### AC Electrical Characteristics: See Section 2 for Waveforms

|                  | Blone   | Const             |  | 74ACT | 1    | 54.   | ACT  | 74   | ACT  | Iodm  | 18          |
|------------------|---|-------------------|--|-------|------|---|------|--|------|-------|-------------|
| Symbol           | Parameter <sub>/0.8</sub> = V0.8 =                    | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       |      | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |      | $T_A = -40^{\circ}C$<br>$to +85^{\circ}C$<br>$C_L = 50 pF$ |      | Units | Fig.<br>No. |
|                  |   | 00V               | Min  | Тур   | Max  | Min   | Max  | Min  | Max  |       | 30          |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 5.0               | 2.0  | 5.5   | 9.5  | 1.0   | 11.0 | 2.0  | 10.0 | ns    | 2-3,        |
| t <sub>PHL</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 5.0               | 2.0  | 5.5   | 9.5  | 1.0   | 11.0 | 2.0  | 10.0 | ns    | 2-3, 4      |
| t <sub>PLH</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0               | 2.0  | 5.5   | 9.0  | 1.0   | 11.0 | 2.0  | 10.0 | ns    | 2-3,        |
| t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0               | 2.0  | 5.5   | 9.0  | 1.0   | 11.0 | 2.0  | 10.0 | ns    | 2-3,        |
| t <sub>PZH</sub> | Output Enable Time<br>OE to On                        | 5.0               | 2.0  | 5.5   | 9.5  | 1.0   | 11.0 | 2.0  | 10.5 | ns    | 2-5,        |
| t <sub>PZL</sub> | Output Enable Time<br>OE to On                        | 5.0               | 2.0  | 5.5   | 9.5  | 1.0   | 11.0 | 2.0  | 10.5 | ns    | 2-5,        |
| <sup>t</sup> PHZ | Output Disable Time<br>OE to On                       | 5.0               | 2.0  | 6.0   | 10.5 | 1.0   | 12.0 | 2.0  | 11.0 | ns    | 2-5, (      |
| t <sub>PLZ</sub> | Output Disable Time<br>OE to On                       | 5.0               | 2.0  | 6.0   | 10.5 | 1.0   | 12.0 | 2.0  | 11.0 | ns    | 2-5, 6      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| 1 |  |
|---|--|
|   |  |
|   |  |
|   |  |

|                        | 1 1   | atimi.t | hoginara. | oo pr | C <sub>L</sub> = 50 pF | C <sub>L</sub> = 50 pF | OTHE     | No.   |
|------------------------|---|---------|-----------|-------|------------------------|------------------------|----------|-------|
| vel/17/88 F            | ZS WA Vous                                      |         | Тур       |       | Guaranteed Mini        | mum                    | nielbit? | 20.10 |
| t <sub>s / Vaa.8</sub> | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0     | -0.5      | 0.5   | 3.0                    | 1.0 nemuO              | ns ns    | 2-7   |
| t <sub>h</sub>         | Hold Time, HIGH or LOW Dn to LE                 | 5.0     | 0.5       | 2.0   | 2.0                    | 2.0 1010               | ns       | 2-7   |
| t <sub>w</sub>         | LE Pluse Width, HIGH                            | 5.0     | 2.0       | 3.5   | 5.0                    | 3.5                    | ns       | 2-3   |

\*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| AC Ele |   |                 |           |      |      |       |       |                          | ce                       | citan  | Capa            |
|--------|---|-----------------|-----------|------|------|-------|-------|--------------------------|--------------------------|--------|-----------------|
|        | ditions   | Con             |           | Unit | Т    | AC/AC | T     | Parameter                | тор                      | mbol   | Svi             |
|        | uniona  | COIN            |           |      |      | Тур   | 0.488 |                          | -40°C                    |        | J. Co.          |
|        | = 5.0V  | $V_{CC} = 5.0V$ |           | pF   |      | 4.5   | nce   | ıt Capacita              | Inpu                     | etintl | CIN             |
|        | = 5.0V  | Vcc             | gyipF min |      | 2083 | 44    | tion  | ver Dissipat<br>acitance | The state of the late of |        | C <sub>Pl</sub> |
|        | Propagation Dalay  D <sub>B</sub> to O <sub>B</sub> | 6,0             | 2.0       | 8.5  | 9.6  | 1.0   | 11.0  | 0.3                      | 10.0                     | en     | 2-3,4           |
|        |   |                 |           |      |      |       |       | 2.0                      |                          |        |                 |
|        |   |                 |           |      |      |       |       |                          |                          |        |                 |
|        |   |                 |           |      |      |       |       |                          |                          |        |                 |
|        |   |                 |           |      |      |       |       |                          |                          |        |                 |
|        |   |                 |           |      |      |       |       |                          |                          |        |                 |
|        |   |                 |           |      |      |       |       |                          |                          |        |                 |
|        |   |                 |           |      |      |       |       |                          |                          |        |                 |

# 54AC/74AC843 • 54ACT/74ACT843

#### **General Description**

The 'AC/'ACT843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

The 'AC/'ACT843 is functionally and pin compatible with AMD's Am29843.

#### **Features**

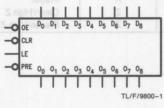
- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

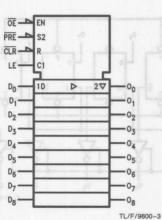
Ordering Code: See Section 8

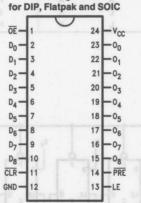
## **Logic Symbols**

## Connection Diagrams

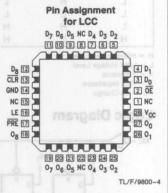
TL/F/9800-2







Pin Assignment



| Pin Names                      | Description   |
|--------------------------------|---------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs   |
| 00-07                          | Data Outputs  |
| ŌĒ                             | Output Enable |
| LE                             | Latch Enable  |
| CLR                            | Clear         |
| PRE                            | Preset        |

## **Functional Description**

The 'AC/'ACT843 consists of nine D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable  $(\overline{OE})$  is LOW. When  $\overline{OE}$  is HIGH, the bus output is in the high impedance state. In

addition to the LE and  $\overline{\text{OE}}$  pins, the 'AC/'ACT843 has a Clear ( $\overline{\text{CLR}}$ ) pin and a Preset ( $\overline{\text{PRE}}$ ) pin. These pins are ideal for parity bus interfacing in high performance systems. When  $\overline{\text{CLR}}$  is LOW, the outputs are LOW if  $\overline{\text{OE}}$  is LOW. When  $\overline{\text{CLR}}$  is HIGH, data can be entered into the latch. When  $\overline{\text{PRE}}$  is LOW, the outputs are HIGH if  $\overline{\text{OE}}$  is LOW. Preset overrides  $\overline{\text{CLR}}$ .

Function Tables

|           | nainainatal aur    | Inputs   | PETATRIET | s and      | Internal     | Outputs                | Function          |  |
|-----------|--------------------|----------|-----------|------------|--------------|------------------------|-------------------|--|
| CLR       | CLR PRE OE         |          | LE        | LE D artis |              | data wido for wider ad | and provide extra |  |
| Н         | Н                  | Н        | Н         | Lithiw     | n compatible | is functionally and pi | High Z            |  |
| Н         | Н                  | Н        | Н         | Н          | Н            | Z                      | High Z            |  |
| Н         | Н                  | Н        | L         | X          | NC           | Z                      | Latched           |  |
| Н         | Н                  | L        | Н         | L          | L            | Bridge dee Section 8   | Transparent       |  |
| Н         | Н                  | L        | Н         | Н          | Н            | Н                      | Transparent       |  |
| H         | Houses             | ositi no | Contacti  | X          | NC           | NC                     | Latched           |  |
| H         | L                  | L        | X         | X          | Н            | Н                      | Preset            |  |
| L         | Н                  | L        | X         | X          | L            | L                      | Clear             |  |
|           | anglesia nig       | L        | X mon     | ^          | Н            | Н                      | Preset            |  |
| L         | 30.3 10 H          | Н        | alos pue  | X          | 1101 101 L   | Z                      | Clear/High Z      |  |
| H STO FEE | OF DEPTH OF THE DA | Н        | L         | X          | Н            | 10 to Z 10 10          | Preset/High Z     |  |

H = HIGH Voltage Level

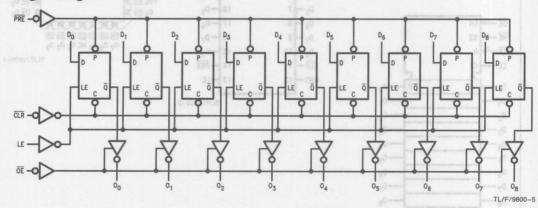
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

NC = No Change

#### **Logic Diagram**



|   |    | r | 1 |  |
|---|----|---|---|--|
|   | r, | ı | 1 |  |
| r | d  | ı | ı |  |
| Ŀ | i  | í | 4 |  |
|   |    | Ŀ | 4 |  |
|   |    |   |   |  |

| Supply Voltage (V <sub>CC</sub> )                                      | 28+0100-0.           | 5V to +7.0V                               | 'AC<br>'ACT   |             | 2.0V to 6.0V<br>4.5V to 5.5V           |
|--|----------------------|---|---|-------------|--|
| DC Input Diode Current (I <sub>IK</sub> )                              |                      |   | Input Voltage (V <sub>I</sub> )                             |             | 0V to V <sub>CC</sub>                  |
| $V_I = -0.5V$ $V_I = V_{CC} + 0.5V$ DC Input Voltage (V <sub>I</sub> ) | -0.5V to             | -20 mA<br>+20 mA<br>V <sub>CC</sub> +0.5V | Output Voltage (V <sub>C</sub> Operating Tempera 74AC/ACT   |             | 0V to V <sub>CC</sub> = -40°C to +85°C |
| DC Output Diode Current ( $I_{OK}$<br>$V_O = -0.5V$                    | 76 6                 | -20 mA                                    | 54AC/ACT  | 8.8         | -55°C to +125°C                        |
| $V_0 = V_{CC} + 0.5V$  |                      | + 20 mA                                   | Minimum Input Edg   | ge Rate (Δ  | V/Δt) memuO jugluO                     |
| DC Output Voltage (V <sub>O</sub> ) DC Output Source                   | -0.5V to             | V <sub>CC</sub> +0.5V                     | V <sub>IN</sub> from 30% to<br>V <sub>CC</sub> @ 3.3V, 4.5V |             | CC 125 mumber 125 mV/ns                |
| or Sink Current (I <sub>O</sub> ) DC V <sub>CC</sub> or Ground Current |                      | ±50 mA                                    | Minimum Input Edg<br>'ACT Devices                           | ge Rate (Δ  | V/Δt)                                  |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )                  |                      | ±50 mA                                    | V <sub>IN</sub> from 0.8V to                                |             | EMERGE ON VOE D CO 405 mV/no           |
| Storage Temperature (T <sub>STG</sub> )                                | -65°                 | C to +150°C                               | V <sub>CC</sub> @ 4.5V, 5.5\                                | TO TANG U D | 125 mV/ns                              |
| Junction Temperature (T <sub>J</sub> ) CDIP PDIP                       |                      | 175°C<br>140°C                            |   |             | DC Electrical Char                     |
| Note 1: Absolute maximum ratings as                                    | o those values heven | d which damage                            |   |             |  |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## **DC Electrical Characteristics for 'AC Family Devices**

|                                  | 30 7 10  | 10.7                   | 74                      | AC                   | 54AC                                 | 74AC                            | o tone 1 s                  | and the state of t |  |
|----------------------------------|--|------------------------|-------------------------|----------------------|--------------------------------------|---------------------------------|-----------------------------|--|--|
| Symbol                           | Parameter  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> =<br>-55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                       | Conditions   |  |
|                                  | TUO! V   | 5.4                    | Тур                     |                      | Guaranteed                           | Limits                          | epatio                      | V tuesuO   |  |
| L or VIHIV<br>- 24 mA<br>- 24 mA | Minimum High Level<br>Input Voltage                                    | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85                  | 2.1<br>3.15<br>3.85             | V                           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VIL AR                           | Maximum Low Level<br>Input Voltage                                     | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65                  | 0.9<br>1.35<br>1.65             | Lay Lay<br>Vello            | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub> s                | Minimum High Level<br>Output Voltage                                   | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                    | 2.9<br>4.4<br>5.4               | V                           | $I_{OUT} = -50 \mu\text{A}$  |  |
|                                  | $O_A = I_A$ $V_A = I_{AB}$ $V_B = V_{AB}$                              | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                    | 2.46<br>3.76<br>4.76            | Current<br>Current          | $^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $-12 \text{ mA}$ $I_{\text{OH}}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| V <sub>OL</sub>                  | Maximum Low Level<br>Output Voltage                                    | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                    | 0.1<br>0.1<br>0.1               | v Dynan                     | $I_{OUT} = 50 \mu A$   |  |
| niM V39.i                        | MA VOHD = 1  V <sub>IN</sub> = V <sub>O</sub> µA vini = V <sub>O</sub> | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50<br>0.50         | 0.44<br>0.44<br>0.44            | urent<br>o Gujesos<br>urent | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}OL$ $^{24} \text{ mA}$ $^{24} \text{ mA}$   |  |
| I <sub>IN</sub>                  | Maximum Input<br>Leakage Current                                       | 5.5                    |                         | ±0.1                 | ±1.0                                 | and a lie b±1.0 cono es         | μΑ                          | $V_I = V_{CC}$ , GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## DC Electrical Characteristics for 'AC Family Devices (Continued) The State of the S

|              |                                      |                        | 74                                      | C         | 54AC                              | 74AC                            | old savid | R SHURSTYFASTOSY<br>Gleana convince  |  |
|--------------|--------------------------------------|------------------------|---|-----------|-----------------------------------|---------------------------------|-----------|--|--|
| Symbol       | VO.S. Parameter                      | V <sub>CC</sub><br>(V) | T <sub>A</sub> = -                      | + 25°C    | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions   |  |
|              | /0                                   |                        | Тур                                     | BioV fugs | Guaranteed L                      | imits                           | Hil) Iner | DC Input Diode Cu  |  |
| lozoV of     | Maximum TRI-STATE<br>Leakage Current | 5.5                    | Itage (V <sub>D</sub><br>Tempers<br>(OT | ±0.5      | ±10.0                             | ±5.0                            | μА        | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I} = V_{CC}$ , GND<br>$V_{O} = V_{CC}$ , GND |  |
| IOLD         | †Minimum Dynamic                     | 5.5                    | 10)                                     | SANCA     | 50                                | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD         | Output Current                       | 5.5                    | and mount                               | FAC Da    | -50                               | -75                             | mA        | V <sub>OHD</sub> = 3.85V Min   |  |
| lcc<br>an\vm | Maximum Quiescent Supply Current     | 5.5                    | n 30% tu<br>LGV, 4.51                   | 8.0       | 160.0                             | 80.0                            | μА        | V <sub>IN</sub> = V <sub>CC</sub> or GND   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

## **DC Electrical Characteristics for 'ACT Family Devices**

|                 |                                      |                        | 74               | ACT          | 544      | CT                 | 74ACT                          | an rallegs are | Mose it Absolute maxim  |
|-----------------|--------------------------------------|------------------------|------------------|--------------|----------|--------------------|--------------------------------|----------------|---|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | -55°C to | =<br>+ 125°C       | T <sub>A</sub> = -40°C to +85° | -              | Conditions  |
|                 |                                      |                        | Тур              |              | Gua      | ranteed L          | imits                          | uo isluorio Mi | " mend operation of FAC   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5              | 2.0          | 2 2      |                    | 2.0                            |                | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0 0      | .8 27764           | 0.8                            | V              | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                    |
| V <sub>OH</sub> | Minimum High Level Output Voltage    | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4 5      | .4                 | 4.4<br>5.4                     | V              | $I_{OUT} = -50 \mu\text{A}$   |
|                 | - YouY<br>- 00 Voc                   | 4.5<br>5.5             |                  | 3.86<br>4.86 | 10.00    | 70 38.8<br>70 38.8 | 3.76<br>4.76                   | ige V          | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001            | 0.1<br>0.1   | 0 0      | 71.00              | 8.1 0.1 8<br>8.8 0.1           | Low Level      | Ι <sub>ΟυΤ</sub> = 50 μΑ  |
|                 | = Tool y                             | 4.5<br>5.5             |                  | 0.36<br>0.36 | S 0.     |                    | 0.44<br>0.44                   | figh Level     | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 24 mA 10L 24 mA   |
| IN NIT          | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | ±.       | 1.0                | ±1.0                           | μΑ             | V <sub>I</sub> = V <sub>CC</sub> , GND                                  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                  | ±0.5         | £ ±1     | 0.0                | ±5.0                           | μΑ             | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$                           |
| ICCT            | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |              | .0 1.    | 6 1.0              | 3.6.1 0.002                    | mA             | $V_I = V_{CC} - 2.1V$   |
| IOLD            | †Minimum Dynamic                     | 5.5                    |                  |              | .0 5     | 0.1 0              | 100.0 751.8                    | mA             | V <sub>OLD</sub> = 1.65V Max  |
| IOHD            | Output Current                       | 5.5                    |                  |              | _        | 50                 | -75                            | mA             | V <sub>OHD</sub> = 3.85V Min  |
| Icc             | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0          | 16       | 0.0 00.0           | 80.0                           | μА             | V <sub>IN</sub> = V <sub>CC</sub><br>or GND                             |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| <b>AC Electrical Characteristics:</b> | See Section 2 for Waveforms |
|---------------------------------------|-----------------------------|
|---------------------------------------|-----------------------------|

|                  | ZAAC  | 01                | 66  | 74AC   |              | 54A   | C            | 74           | AC                    |       |        |
|------------------|---|-------------------|---|--|--------------|---|--------------|--------------|-----------------------|-------|--------|
| Symbol           | Parameter of  | V <sub>CC</sub> * | 7 <sub>A</sub> = to + to + C <sub>L</sub> = | T <sub>A</sub> = +25°<br>C <sub>L</sub> = 50 p |              | T <sub>A</sub> = -<br>to + 12<br>C <sub>L</sub> = 5 | 25°C         | 1            | 40°C<br>85°C<br>50 pF | Units | Fig.   |
|                  | m   | iminiM be         | Min   | Тур  | Max          | Min   | Max          | Min          | Max                   |       |        |
| tpLH             | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.3 8<br>5.0 0    | 3.5<br>2.0                                  | 6.5<br>4.5                                     | 12.0         | 1.0 8.8   | 14.0<br>10.0 | 1.5          | 13.0                  | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay                                     | 3.3<br>5.0        | 4.0   | 7.0<br>5.0                                     | 12.0<br>8.5  | 1.0 8.8   | 14.0<br>10.0 | 3.0          | 13.0                  | ns    | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay<br>LE to On                         | 3.3<br>5.0        | 3.5   | 6.5<br>4.5                                     | 12.0         | 1.0 8.8<br>1.0 0.3                                  | 14.0<br>10.0 | 2.5          | 13.0                  | ns    | 2-3, 4 |
| t <sub>PHL</sub> | Propagation Delay<br>LE to On                         | 3.3 °<br>5.0 °    | 4.0   | 7.0<br>5.0                                     | 12.0         | 1.0 8.8<br>1.0 0.8                                  | 14.0<br>10.0 | 3.0          | 13.0<br>9.0           | ns    | 2-3, 4 |
| t <sub>PLH</sub> | Propagation Delay                                     | 3.3<br>5.0        | 5.5<br>3.5                                  | 8.5<br>6.0                                     | 19.0<br>13.0 | 1.0 8.8   | 23.5<br>16.0 | 4.5<br>2.5   | 21.5<br>14.5          | ns    | 2-3, 4 |
| tPHL             | Propagation Delay                                     | 3.3<br>5.0        | 7.5<br>5.0                                  | 11.0<br>7.5                                    | 21.5         | 1.0 8.8<br>1.0 0.8                                  | 26.5<br>19.0 | 6.0<br>4.0   | 24.0<br>17.0          | ns    | 2-3, 4 |
| t <sub>PZH</sub> | Output Enable Time                                    | 3.3<br>5.0        | 3.5   | 6.0<br>4.5                                     | 11.0         | 1.0 8.8   | 13.0<br>10.0 | 3.0 V<br>1.5 | 12.0<br>9.0           | ns    | 2-5, 6 |
| tPZL             | Output Enable Time                                    | 3.3<br>5.0        | 4.0<br>2.0                                  | 6.5<br>5.0                                     | 11.0<br>8.0  | 1.0   | 13.0<br>10.0 | 2.5          | 12.0                  | ns    | 2-5, 6 |
| t <sub>PHZ</sub> | Output Disable Time<br>OE to On                       | 3.3<br>5.0        | 4.0<br>3.0                                  | 6.5<br>5.0                                     | 10.5<br>8.0  | 1.0<br>1.0  | 12.0<br>9.0  | 3.5<br>2.5   | 11.0<br>8.5           | ns    | 2-5, 6 |
| t <sub>PLZ</sub> | Output Disable Time                                   | 3.3<br>5.0        | 3.0<br>2.0                                  | 6.0<br>4.5                                     | 10.5<br>8.0  | 1.0<br>1.0  | 12.0<br>9.0  | 2.5<br>1.5   | 11.0<br>8.5           | ns    | 2-5, 6 |
| t <sub>PHL</sub> | Propagation Delay PRE to On                           | 3.3<br>5.0        | 4.5<br>3.0                                  | 7.0<br>5.0                                     | 12.5<br>9.0  | 1.0<br>1.0  | 15.0<br>10.5 | 3.5<br>2.0   | 13.5<br>9.5           | ns    | 2-3, 4 |
| <sup>t</sup> PLH | Propagation Delay                                     | 3.3<br>5.0        | 4.5<br>3.0                                  | 7.0<br>5.0                                     | 12.5<br>9.0  | 1.0<br>1.0  | 15.0<br>10.5 | 3.5<br>2.0   | 13.5<br>9.5           | ns    | 2-3, 4 |

<sup>\*</sup>Voltage Range 3.3 is 3.3V  $\pm 0.3$ V

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

|                  |       |                              |           |      | SAAG              | 74        | AC              |            | 54AC                          | 74AC   |                 |      |
|------------------|-------|------------------------------|-----------|------|-------------------|-----------|-----------------|------------|-------------------------------|--|-----------------|------|
| Symbol           | dieU  | Paran                        | neter     | 0 0  | V <sub>CC</sub> * |           | + 25°C<br>50 pF | to         | = -55°C<br>+ 125°C<br>= 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units           | Fig. |
|                  |       | xets                         | nttit     | ico) | iš niši           | Тур       | gyT C           | auaran     | teed Minim                    | num  |                 |      |
| ts               | 51.79 | up Time, H<br>o LE           | HIGH or L | OW   | 3.3<br>5.0        | 0<br>-0.5 | 3.0<br>1.5      | 3.5        | 3.5 8.8<br>2.0 0.3            | 2.0  | ns              | 2-7  |
| t <sub>h</sub>   | 53478 | d Time, HI<br>o LE           | GH or LO  | Wos  | 3.3               | -0.5.8    | 2.0<br>2.5      | 4.0<br>2.5 | 2.0                           | 2.0 notis  | ns              | 2-7  |
| tw               | LEF   | Pulse Wid                    | th, HIGH  | 4.0  | 3.3<br>5.0        | 1.5       | 3.0<br>3.0      | 3.5        | 3.5 8.8                       | 3.0  | ns              | 2-3  |
| t <sub>w</sub>   | PRE   | Pulse W                      | idth, LOW | 0.0  | 3.3               | 5.0       | 12.0<br>8.5     | 4.0        | 16.0 a 8<br>11.0 a 8          | 14.5   | ns              | 2-3  |
| tw               | CLR   | Pulse Wi                     | idth, LOW | 8.8  | 3.3               | 5.5       | 14.0<br>10.0    | 5.6        | 18.5                          | 16.5   | ns              | 2-3  |
| t <sub>rec</sub> | PRE   | Recover                      | y Time    | 8,6  | 3.3               | 1.0       | 3.0<br>1.5      | 7.5        | 3.5<br>1.5                    | 3.0  | ns              | 2-3, |
| t <sub>rec</sub> | CLR   | Recover                      | y Time    | 0.8  | 3.3               | 0<br>-0.5 | 1.5<br>0.5      | 3.5<br>2.0 | 2.5 a.a 1.5 a.a               | 0.5  | ns              | 2-3, |
| A CHARLES        | 1071  | 3 is 3.3V ±0<br>0 is 5.0V ±0 |           | 0.0  |                   | 11.0      | 6,6             | 4.0        | 8.8<br>6.8                    | Enable Time  | Output<br>OE to | PZL  |
|                  |       |                              |           |      |                   |           |                 | 4.0        |                               |  |                 |      |
|                  |       |                              |           |      |                   |           |                 |            |                               |  |                 |      |
|                  |       |                              |           |      |                   |           | 7.0             | 4.6        |                               |  |                 |      |

## 4

#### AC Electrical Characteristics: See Section 2 for Waveforms 74ACT 54ACT 74ACT $T_A = -55^{\circ}C$ $T_A = -40^{\circ}C$ TA = +25°C Vcc\* Fig. to + 125°C to +85°C Units Symbol **Parameter** $C_L = 50 pF$ No. (V) $C_L = 50 pF$ CL = 50 pF Min Тур Max Min Max Min Max Propagation Delay **tPLH** 11.0 5.0 2.5 5.5 9.5 1.0 2.0 10.0 2-3,4 D<sub>n</sub> to O<sub>n</sub> Propagation Delay **tPHL** 5.5 10.0 2-3, 4 5.0 2.5 9.5 1.0 11.0 2.0 ns D<sub>n</sub> to O<sub>n</sub> Propagation Delay **tPLH** 5.0 5.5 1.0 2.0 10.0 2-3, 4 2.5 9.0 11.0 ns LE to On Propagation Delay **t**PHL 5.0 2.5 5.5 9.0 1.0 11.0 2.0 10.0 ns 2 - 3, 4LE to On Propagation Delay **t**PLH 5.0 2.5 6.5 1.0 17.5 2.0 16.0 2-3,4 14.0 PRE to On Propagation Delay t<sub>PHL</sub> 5.0 2.5 7.5 15.5 1.0 19.0 2.0 17.5 2 - 3, 4CLR to On Output Enable Time **t**PZH 5.0 2.5 5.5 9.5 1.0 11.0 2.0 10.5 2-5,6 OE to On Output Enable Time **tPZL** 5.0 2.5 5.5 9.5 1.0 11.0 2.0 10.5 2-5,6 ns OE to On Output Disable Time **t**PHZ 5.0 2.5 6.0 10.5 1.0 12.0 2.0 11.0 2-5,6 ns OE to On Output Disable Time tPLZ 5.0 2.5 6.0 10.5 1.0 12.0 2.0 11.0 2-5, 6 ns OE to On Propagation Delay tPHL 5.0 2.5 6.0 10.5 1.0 12.5 2.0 11.0 2-3, 4 ns PRE to On

t<sub>PLH</sub>

Propagation Delay

## AC Operating Requirements: See Section 2 for Waveforms

5.0

2.5

5.5

9.5

1.0

11.5

2.0

10.5

ns

2-3,4

|                  |   |                   | 74   | ACT               | 54ACT  | 74ACT   |       |        |
|------------------|---|-------------------|------|-------------------|--|---|-------|--------|
| Symbol           | ymbol Parameter                                 | V <sub>CC</sub> * |      | + 25°C<br>= 50 pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$ to +85°C $C_L = 50 \text{ pF}$ | Units | Fig.   |
|                  |   |                   | Тур  |                   | Guaranteed Minin   | num   |       |        |
| ts               | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0               | -0.5 | 0.5               | 1.0  | 1.0   | ns    | 2-7    |
| th               | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 5.0               | 0.5  | 2.0               | 2.0  | 2.0   | ns    | 2-7    |
| t <sub>w</sub>   | LE Pulse Width, HIGH                            | 5.0               | 2.0  | 3.5               | 3.5  | 3.5   | ns    | 2-3    |
| t <sub>w</sub>   | PRE Pulse Width, LOW                            | 5.0               | 5.0  | 8.5               | 11.0   | 10.0  | ns    | 2-3    |
| t <sub>w</sub>   | CLR Pulse Width, LOW                            | 5.0               | 5.5  | 9.5               | 12.5   | 11.0  | ns    | 2-3    |
| t <sub>rec</sub> | PRE Recovery Time                               | 5.0               | 0.5  | 2.0               | 2.0  | 2.0   | ns    | 2-3, 7 |
| t <sub>rec</sub> | CLR Recovery Time                               | 5.0               | -0.5 | 1.0               | 1.0  | 1.0   | ns    | 2-3, 7 |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

| Parameter Vo. | pF V <sub>C</sub> |       | 44  | - 30<br>- 30 | Power Dissipation Capacitance |      |      |     |    | C <sub>PD</sub> |  |
|---------------|-------------------|-------|-----|--------------|-------------------------------|------|------|-----|----|-----------------|--|
|               |                   | CELEK | Typ | XXIII        | niss                          | XSM  | nila | Max |    |                 |  |
|               |                   |       |     |              |                               | 11.0 |      |     |    |                 |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |
|               |                   |       |     |              |                               | 11.0 |      |     | ns | 2-3,4           |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |
|               |                   |       |     |              |                               | 17.6 |      |     |    |                 |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |
|               |                   |       |     |              |                               | 12.5 |      |     |    |                 |  |
|               |                   |       |     |              |                               |      |      |     |    |                 |  |

Veloc Voic at 0.5 square enableM\*

AC Operating Requirements: see Section 2 for Wevelorms

|                                    |     |     |  | $T_A = -55^{\circ}C$ $to + 125^{\circ}C$ $C_L = 50 pF$ |    |     |  |
|------------------------------------|-----|-----|--|--|----|-----|--|
|                                    |     |     |  | Guaranteed Minim                                       |    |     |  |
|                                    |     |     |  |  |    |     |  |
| Hold Time, HIGH or LOW<br>Da to LE | 6.0 |     |  |  | 86 |     |  |
|                                    |     |     |  |  |    |     |  |
|                                    |     | 5.0 |  |  |    |     |  |
|                                    |     |     |  |  |    | 2-3 |  |
|                                    |     |     |  |  |    |     |  |
|                                    |     |     |  |  |    |     |  |

Voltage Range 5.0 is 5.0V ±0.5V

## 54ACT/74ACT845 8-Bit Transparent Latch with TRI-STATE® Outputs

## **General Description**

The 'ACT845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple  $\overline{\text{OE}}$  controls.

The 'ACT845 is functionally and pin compatible with AMD's Am29845.

#### **Features**

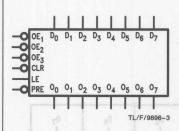
■ 'ACT845 has TTL-compatible inputs

Ordering Code: See Section 8

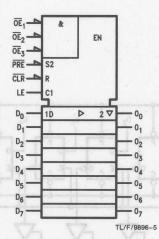
**Logic Symbols** 

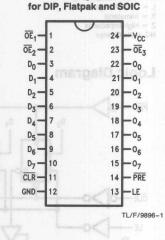
## **Connection Diagrams**

**Pin Assignment** 

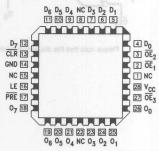


| Pin Names  | Description                 |
|--|-----------------------------|
| D <sub>0</sub> -D <sub>7</sub><br>O <sub>0</sub> -O <sub>7</sub> | Data Inputs<br>Data Outputs |
| OE <sub>1</sub> -OE <sub>3</sub>                                 | Output Enables              |
| LE<br>CLR  | Latch Enable<br>Clear       |
| PRE  | Preset                      |









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1

## **Functional Description**

The 'ACT845 consists of eight D latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

On the LE HIGH-to-LOW transition, the data that meets the setup times is latched Data appears on the bus when the Output Enables  $(\overline{OE}_1, \overline{OE}_2, \overline{OE}_3)$  are LOW. When any one of  $\overline{OE}_1, \overline{OE}_2$  or  $\overline{OE}_3$  is HIGH, the bus output is in the high impedance state.

Function Table

|        |          | Inputs        |      | Internal   | Output   | Function      |               |
|--------|----------|---------------|------|------------|----------|---------------|---------------|
| CLR    | PRE      | ŌĒn           | LE 8 | D          | Q        | 0             | nollqna       |
| Н      | H strick | domparible in | H as | ri dagi cu | L efanim | Z             | High Z        |
| Н      | H        | Н             | Н    | Н          | H        | Z             | High Z        |
| Н      | Н        | Н             | L    | X          | NC       | Z             | Latched       |
| Н      | Н        | L             | Н    | L          | S LINUA  | unan elosados | Transparent   |
| H      | Н        | L             | Н    | Н          | Н        | Н             | Transparent   |
| Н      | Н        | L             | L    | X          | NC       | NC            | Latched       |
| Н      | L        | L             | X    | X          | Н        | Н 0           | Preset        |
| L      | Н        | L             | X    | X          | L        | L             | Clear         |
| munael | Logit    | Cortnec       | X    | X          | Н        | Н             | Preset        |
| L      | Н        | Н             | L    | X          | L        | Z             | Clear/High Z  |
| Н      | L        | Н             | L    | X          | Н        | Z             | Preset/High Z |

H = HIGH Voltage Level

L = LOW Voltage Level

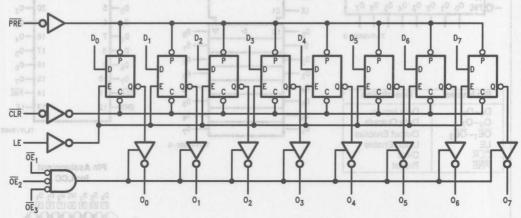
X = Immaterial

Z = High Impedance

NC = No Change

## **Logic Diagram**

THE REPORT OF THE PARTY.



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ ) -0.5V to +7.0V DC Input Diode Current ( $I_{IK}$ )  $V_I = -0.5V$  -20 mA  $V_I = V_{CC} + 0.5V$  +20 mA DC Input Voltage ( $V_I$ ) -0.5V to  $V_{CC} + 0.5V$  DC Output Diode Current ( $I_{OK}$ )

DC Output Source or Sink Current (I<sub>O</sub>) ±50 mA
DC V<sub>CC</sub> or Ground Current

Per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ± 50 mA
Storage Temperature (T<sub>STG</sub>) -65°C to +150°C
Junction Temperature (T<sub>J</sub>)

CDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 2.0V to 6.0V

 'AC
 2.0V to 6.0V

 'ACT
 4.5V to 5.5V

 Input Voltage (V<sub>I</sub>)
 0V to V<sub>CC</sub>

 Output Voltage (V<sub>O</sub>)
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 -40°C to +85°C

 74ACT
 -55°C to +125°C

Minimum Input Edge Rate ( $\Delta V/\Delta t$ ) 'AC Devices

 $\rm V_{IN}$  from 30% to 70% of  $\rm V_{CC}$   $\rm V_{CC}$  @ 3.3V, 4.5V, 5.5V  $\rm 125~mV/ns$ 

Minimum Input Edge Rate (ΔV/Δt)

2.0 6.5

'ACT Devices
V<sub>IN</sub> from 0.8V to 2.0V
V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

## DC Electrical Characteristics for 'ACT Family Devices

175°C 140°C

| Symbol           | 0.8 en 0.11<br>Parameter             | 744                   | ACT          | 54ACT                            | 74ACT                           | 977          | Carlolina  | Color Culture D   |
|------------------|--------------------------------------|-----------------------|--------------|----------------------------------|---------------------------------|--------------|------------|---|
|                  |                                      | T <sub>A</sub> = 25°C |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units<br>(V) | Vcc        | Conditions  |
|                  | 2-6                                  | 11.6 ns 5.0           | Тур          | 4                                | Guaranteed Li                   | mits 0.8 0.5 | 987        | eldes   |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage  | 1.5<br>1.5            | 2.0<br>2.0   | 2.0                              | 2.0<br>2.0                      | V            | 4.5<br>5.5 | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage   | 1.5<br>1.5            | 0.8          | 0.8<br>0.8                       | 0.8<br>0.8                      | ٧            | 4.5<br>5.5 | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub>  | Minimum High Level                   | 4.49<br>5.49          | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V            | 4.5<br>5.5 | $I_{OUT} = -50 \mu\text{A}$   |
|                  |                                      |                       | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | ٧            | 4.5<br>5.5 | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $-24 \text{ mA}$  |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage  | 0.001<br>0.001        | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1<br>0.1                      | ٧            | 4.5<br>5.5 | $I_{OUT} = 50 \mu A$  |
|                  |                                      |                       | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | V            | 4.5<br>5.5 | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current     |                       | ±0.1         | ±1.0                             | ±1.0                            | μΑ           | 5.5        | $V_I = V_{CC}$ , GND  |
| loz              | Maximum TRI-STATE<br>Leakage Current |                       | ±0.5         | ±10.0                            | ±5.0                            | μΑ           | 5.5        | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |
| Ісст             | Maximum I <sub>CC</sub> /Input       | 0.6                   |              | 1.6                              | 1.5                             | mA           | 5.5        | $V_I = V_{CC} - 2.1V$   |
| lold             | †Minimum Dynamic                     |                       |              | 50                               | 75                              | mA           | 5.5        | V <sub>OLD</sub> = 1.65V Max  |
| I <sub>OHD</sub> | Output Current                       |                       |              | -50                              | -75                             | mA           | 5.5        | V <sub>OHD</sub> = 3.85V Min  |
| Icc              | Maximum Quiescent<br>Supply Current  |                       | 8.0          | 160                              | 80                              | μΑ           | 5.5        | V <sub>IN</sub> = V <sub>CC</sub> or Ground   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

| <b>AC Electrical Characteristics</b> | S: See Section 2 for Waveforms |
|--------------------------------------|--------------------------------|
|--------------------------------------|--------------------------------|

|                                       |  |         |      |  | 74ACT        |      | 54A  | СТ   | 74   | CT     | pa soaqaola<br>Mari the M | 16A\Y16<br>63600         | Miller ti<br>Dessia |
|---------------------------------------|--|---------|------|--|--------------|------|--|--|--|--------|---------------------------|--------------------------|---------------------|
| Symbol                                | Parameter  |         |      | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              |      | $T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$ |  | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |        | Units                     | V <sub>CC</sub> *<br>(V) | Fig.<br>No.         |
| ooV of V                              | 0  |         |      | Min  | Тур          | Max  | Min  | Max  | Min  | Max    | 1.29                      | -0.5V                    | = 14                |
| t <sub>PLH</sub>                      | Propagat<br>D <sub>n</sub> to O <sub>n</sub>       | ion Del | ay   | 2.0  | 5.5          | 9.5  | V8.0 +   | DOV of N                                   | 2.0  | 10.0   | ns) e                     | 5.0                      | 2-3,                |
| t <sub>PHL</sub>                      | Propagation Delay D <sub>n</sub> to O <sub>n</sub> |         | ay   | 2.0  | 5.5          | 9.5  | Am 0s<br>Am 0s   |  | 2.0  | 10.0   | ns                        | 5.0                      | 2-3,                |
| t <sub>PLH</sub>                      | Propagation Delay<br>LE to On                      |         | ay   | 2.0  | 5.5          | 9.0  | V6.0 +<br>Am 08  | . 50 V of V                                | 2.0  | 10.0   | (O <sub>A</sub> ) and     | 5.0                      | 2-3,                |
| t <sub>PHL</sub>                      | Propagation Delay<br>LE to On                      |         | ay   | 2.0  | 5.5          | 9.0  | Am 08  | ± 65 0/8                                   | 2.0  | 10.0   | ns                        | 5.0                      | 2-3,                |
| tpLH                                  | Propagat<br>PRE to O                               |         | ay   | 2.0  | 6.5          | 14.0 | 178°C  |  | 2.0  | 16.0   | ns                        | 5.0                      | 2-3,                |
| t <sub>PHL</sub>                      | Propagat<br>CLR to O                               | ion Del | ay   | 2.0  | 7.5          | 15.5 | damage without   | doi/lw book                                | 2.0  | 17.5   | ns                        | 5.0                      | 2-3,                |
| t <sub>PZH</sub>                      | Output E   |         | ime  | 2.0  | 5.5          | 9.5  |  | er its power<br>at does not<br>antibations | 2.0  | 10.5   | ns                        | 5.0                      | 2-5                 |
| t <sub>PZL</sub>                      | Output E   |         | ime  | 2.0  | 5.5          | 9.5  | 'ACT   | cs for                                     | 2.0  | 10.5   | ns                        | 5.0                      | 2-6                 |
| t <sub>PHZ</sub>                      | Output Di  |         | Time | 2.0  | 6.0          | 10.5 | FAACT<br>TA=   | 09   | 2.0  | 11.0   | ns                        | 5.0                      | 2-5                 |
| t <sub>PLZ</sub>                      | Output Di  |         | Time | 2.0  | 6.0          | 10.5 | PierauD  |  | 2.0 (T   | 11.0   | ns                        | 5.0                      | 2-6                 |
| t <sub>PHL</sub> VII.0                | Propagat<br>PRE to O                               |         | ay   | 2.0  | 6.0          | 10.5 | 0.8  | 0.9  | 2.0  | 11.0   | ns                        | 5.0                      | 2-3,                |
| t <sub>PLH</sub><br>A <sub>4</sub> 08 | Propagati<br>CLR to O                              |         | ay   | 2.0  | 5.5          | 9.5  | 0.8  | 8.0  | 2.0  | 10.5   | ns                        | 5.0                      | 2-3,                |
| *Voltage F                            | Range 5.0 is 5                                     | TAG     | 5V   | 7  | 3.4          |      | 9.0  | 2.6  | EA.C   |        |                           |                          |                     |
|                                       |  |         | γ    |  | 3,76<br>4,76 |      |  |  |  |        |                           |                          |                     |
|                                       |  |         | ٧    |  |              |      | 0.1<br>0.1   |  | 0.001  |        | woul mus<br>epsticV t     |                          |                     |
|                                       |  |         | v    |  | 0.44         |      |  |  |  |        |                           |                          |                     |
|                                       |  |         |      |  |              |      |  |  |  |        |                           |                          |                     |
|                                       |  |         |      |  |              |      | ±10.0  |  |  |        |                           | nhaMa                    |                     |
|                                       |  |         |      |  |              |      | 1.6  |  |  |        |                           |                          |                     |
|                                       |  |         |      |  |              |      |  |  |  |        |                           |                          |                     |
|                                       |  |         |      |  |              |      |  |  |  |        | Culpu                     |                          |                     |
|                                       |  |         |      |  |              |      |  |  |  | triess | num Quie<br>y Current     |                          |                     |

4-324

# AC Operating Requirements: See Section 2 for Waveforms

|                     |   | 74/       | ACT             | 54ACT   | 74ACT  | a samu | nima2             | Fig.   |
|---------------------|---|-----------|-----------------|---|--|--------|-------------------|--------|
| Symbol              | Parameter                                       |           | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units  | V <sub>CC</sub> * |        |
|                     |   | Тур       |                 | <b>Guaranteed Min</b>   | ideria   | Late   | H8-8              |        |
| ts                  | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | -0.5      | 0.5             | Checker   | (1.01 <u>1.0</u> 1911  | ns     | 5.0               | 2-7    |
| t <sub>h</sub>      | Hold Time, HIGH or LOW                          | 0.5       | 2.0             | Film reviews  | 2.0<br>heat wined Ad-8 o                                     | ns     | 5.0               | 2-7    |
| t <sub>w</sub> -ber | LE Pulse Width, HIGH                            | 2.0       | 3.5             | as a feed- w  | 3.5  | ns     | 5.0               | 2-3    |
| t <sub>w</sub> -per | PRE Pulse Width, LOW                            | 5.0       | 8.5             | CTRS9 fea- m  | "\OA' 10.0 noiles  | ns     | 5.0               | 2-3    |
| t <sub>w</sub>      | CLR Pulse Width, LOW                            | 5.5       | 9.5             | bas nelsons   | 11.0   | ns     | 5.0               | 2-3    |
| t <sub>rec</sub>    | PRE Recovery Time                               | 0.5       | 2.0             | arity.  | grible 2.0 tol en  | nsol   | 5.0               | 2-3, 7 |
| t <sub>rec</sub>    | CLR Recovery Time                               | waerodlum | a of 1,0 kdA    | 8   | 1.0  | ns     | 5.0               | 2-3,7  |

\*Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance do of AVT epidedo of been on) EXE bis

| Symbol          | Parameter                     | Тур | Units | Conditions             |
|-----------------|-------------------------------|-----|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance             | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation Capacitance | 44  | pF    | V <sub>CC</sub> = 5.0V |

E 21 8993

a May be used in system applications in p

Pin Assignment for PCC

展問問題問題問

A993 E X

085' bns



# 54AC/74AC899 • 54ACT/74ACT899 9-Bit Latchable Transceiver with Parity Generator/Checker

# **General Description**

The 'AC/'ACT899 is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. The 'AC/'ACT899 features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/EVEN parity, and separate error signal output pins for checking parity.

#### **Features**

- Latchable transceiver with output sink of 24 mA
- Option to select generate parity and check or "feedthrough" data/parity in directions A-to-B or B-to-A

AC Operating Requirements: sees

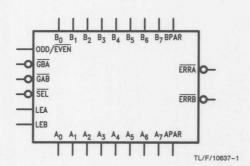
Symbol

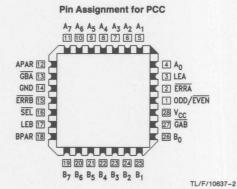
- Independent latch enable for A-to-B and B-to-A directions
- Select pin for ODD/EVEN parity
- ERRA and ERRB output pins for parity checking
- Ability to simultaneously generate and check parity
- May be used in system applications in place of the '534 and '280
- May be used in system applications in place of the '657 and '373 (no need to change T/R to check parity)
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

**Logic Symbol** 

# **Connection Diagram**





| A |  |  |  |
|---|--|--|--|
| A |  |  |  |
|   |  |  |  |
|   |  |  |  |
|   |  |  |  |
|   |  |  |  |

| Pin Names                      | Description   |
|--------------------------------|---|
| A <sub>0</sub> -A <sub>7</sub> | A Bus Data Inputs/Data Outputs  |
| B <sub>0</sub> -B <sub>7</sub> | B Bus Data Inputs/Data Outputs  |
| APAR, BPAR                     | A and B Bus Parity Inputs   |
| ODD/EVEN                       | ODD/EVEN Parity Select, Active LOW for EVEN Parity                              |
| GBA, GAB                       | Output Enables for A or B Bus,<br>Active LOW                                    |
| SEL                            | Select Pin for Feed-Through or<br>Generate Mode, LOW for Generate<br>Mode       |
| LEA, LEB                       | Latch Enables for A and B Latches,  |
|                                | HIGH for Transparent Mode   |
| ERRA, ERRB                     | Error Signals for Checking Generated Parity with Parity In, LOW if Error Occurs |

# Functional Description

The 'AC/'ACT899 has three principal modes of operation which are outlined below. These modes apply to both the Ato-B and B-to-A directions.

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select (SEL) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by ERRB (ERRA).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if SEL is HIGH. Parity is still generated and checked as ERRA and ERRB in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

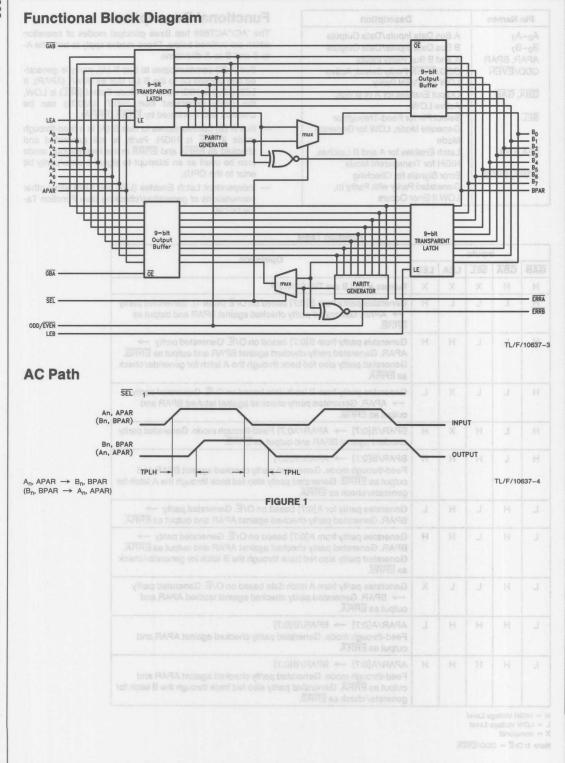
|            |               | Protection of the second | Ta2 | Heres<br>Harriage | Function Table   |
|------------|---------------|--------------------------|-----|-------------------|--|
|            | L             | nputs                    |     | HOTEL             | Operation  |
| GAB        | GBA           | SEL                      | LEA | LEB               |  |
| Н          | Н             | Х                        | Х   | Х                 | Busses A and B are TRI-STATE®.   |
| H          | L             | L                        | L   | Н                 | Generates parity from B[0:7] based on O/Ē (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as ERRB.   |
| Hor        | ac.           | L                        | Н   | Н                 | Generates parity from B[0:7] based on O/Ē. Generated parity → APAR. Generated parity checked against BPAR and output as ĒRRB. Generated parity also fed back through the A latch for generate/check as ĒRRA. |
| Н          | L             | L                        | Х   | L                 | Generates parity from B latch data based on O/Ē. Generated parity  → APAR. Generated parity checked against latched BPAR and output as ĒRRB.   |
| Н          | L             | Н                        | Х   | Н                 | BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as ERRB.  |
| H<br>5-788 | L<br>IO/\9\JY | Н                        | H   | Н                 | BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as ERRB. Generated parity also fed back through the A latch for generate/check as ERRA.                        |
| L          | Н             | L                        | Н   | L                 | Generates parity for A[0:7] based on O/Ē. Generated parity → BPAR. Generated parity checked against APAR and output as ĒRRĀ.   |
| L          | Н             | L                        | Н   | Н                 | Generates parity from A[0:7] based on O/Ē. Generated parity → BPAR. Generated parity checked against APAR and output as ĒRRĀ. Generated parity also fed back through the B latch for generate/check as ĒRRĒ. |
| L          | Н             | L                        | L   | X                 | Generates parity from A latch data based on O/Ē. Generated parity  → BPAR. Generated parity checked against latched APAR and output as ĒRRĀ.   |
| L          | Н             | Н                        | Н   | L                 | APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as ERRA.   |
| L          | Н             | Н                        | Н   | Н                 | APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as ERRA. Generated parity also fed back through the B latch for generate/check as ERRB.                        |

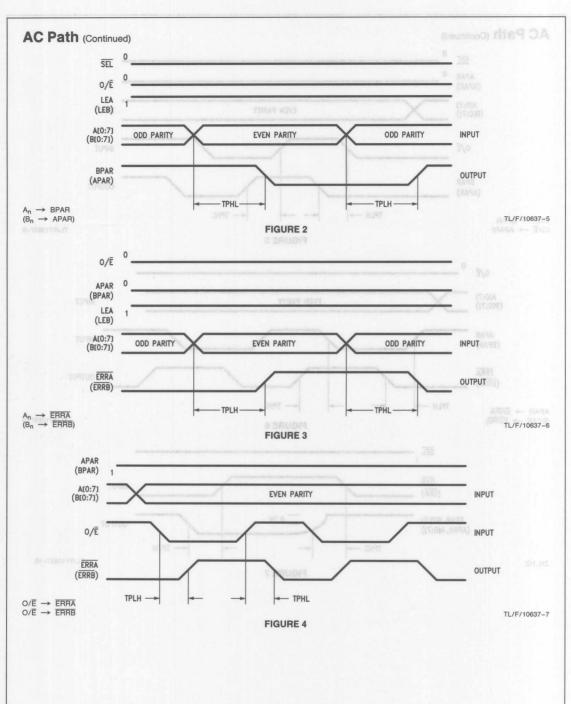
H = HIGH Voltage Level

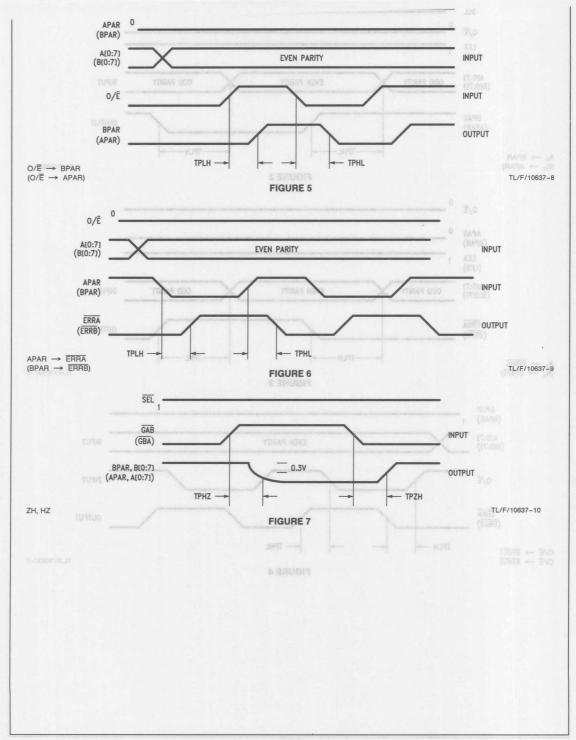
L = LOW Voltage Level

X = Immaterial

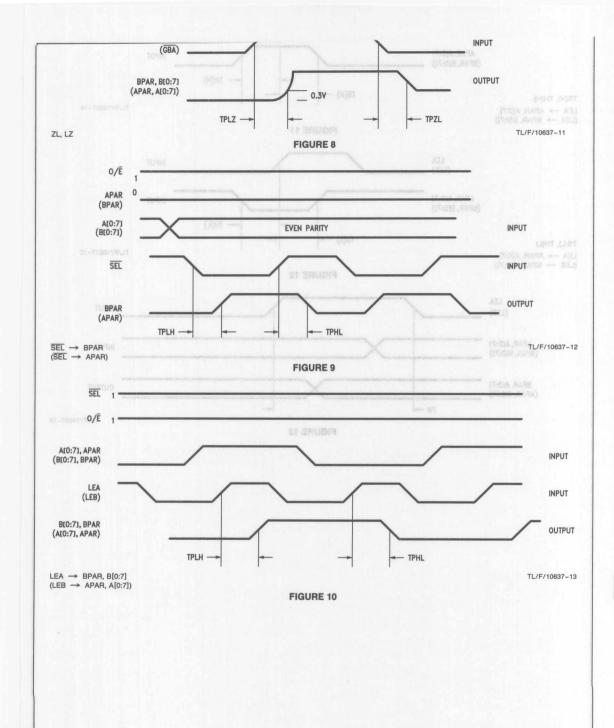
Note 1: O/E = ODD/EVEN



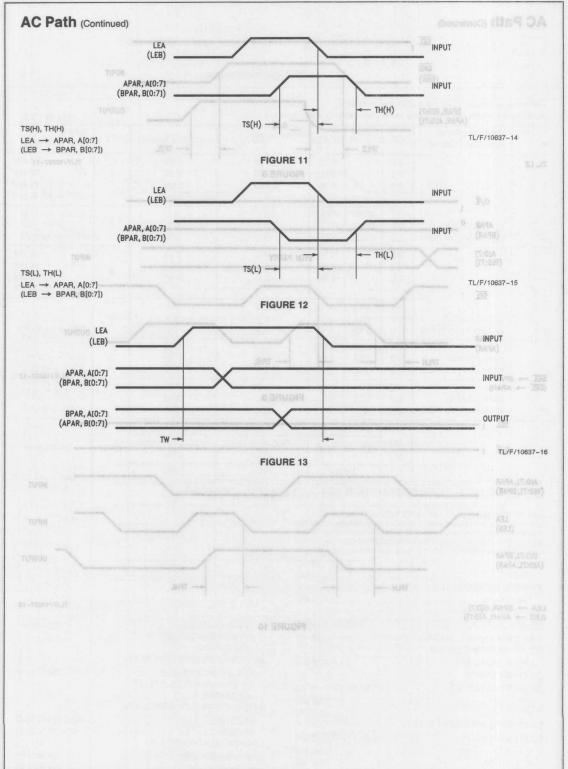












If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )         | 1+ 01 0°01-0. | 5V to +7.0V            |
|---|---------------|------------------------|
| DC Input Diode Current (I <sub>IK</sub> ) | ette          | Li beeinstel           |
| $V_1 = -0.5V$<br>$V_1 = V_{CC} + 0.5V$    |               | -20 mA<br>+20 mA       |
| DC Input Voltage (V <sub>I</sub> )        | ≥√ −0.5V to   | V <sub>CC</sub> + 0.5V |
| DC Output Diode Current (IOK)             |               |                        |

 $V_0 = -0.5V$ -20 mA +20 mA  $V_O = V_{CC} + 0.5V$ DC Output Voltage (Vo) -0.5V to V<sub>CC</sub> + 0.5V

DC Output Source or Sink Current (IO) ±50 mA DC V<sub>CC</sub> or Ground Current

per Output Pin (ICC or IGND) ±50 mA Storage Temperature (TSTG) -65°C to +150°C DC Latch-Up Source or

±300 mA Sink Current Junction Temperature (TJ) CDIP 175°C PDIP 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Absolute Maximum Ratings (Note 1) Recommended Operating **Conditions**

Supply Voltage (V<sub>CC</sub>) 'AC 2.0V to 6.0V 4.5V to 5.5V 'ACT OV to VCC Input Voltage (Vi) Output Voltage (Vo) OV to VCC Operating Temperature (TA) -40°C to +85°C 74AC/ACT 54AC/ACT -55°C to +125°C

Minimum Input Edge Rate ΔV/Δt 'AC Devices

VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.0V, 4.5V, 5.5V

Minimum Input Edge Rate ΔV/Δt 'ACT Devices

VIN from 0.8V to 2.0V Vcc @ 4.5V, 5.5V

125 mV/ns

# DC Electrical Characteristics for 'AC Family Devices

|                      | - 00 V 10  | 8.0                    | 74                                     | AC                   | 8.0                              | 54AC                 | 74AC                            | Rage                                     |  |  |
|----------------------|--|------------------------|--|----------------------|----------------------------------|----------------------|---------------------------------|--|--|--|
| Symbol               | Parameter  | V <sub>CC</sub><br>(V) | V <sub>CC</sub> T <sub>A</sub> = +25°C |                      | T <sub>A</sub> = -55°C to +125°C |                      | T <sub>A</sub> = -40°C to +85°C | Units                                    | Conditions   |  |
|                      | $A = N _{A}$   |                        | Тур                                    | Guaranteed Limits    |                                  |                      |                                 |  |  |  |
| VIH AS —             | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75                    | 2.1<br>3.15<br>3.85  | 4.70                             | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85             | V<br>e.l wo.l a                          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| L of V <sub>IH</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75                    | 0.9<br>1.35<br>1.65  | 08.0                             | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65             | V  | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| VOH                  | Minimum High Level<br>Output Voltage   | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49                   | 2.9<br>4.4<br>5.4    | 08,6°<br>±1.0                    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4               | n InVat                                  | I <sub>OUT</sub> = -50 μA  |  |
|                      | $\mu A \qquad \forall i = V_{IL},$ $\mu A \qquad \forall G = V_{GC}$ $\mu A \qquad \forall i = V_{GC}$ | 3.0<br>4.5<br>5.5      |  | 2.56<br>3.86<br>4.86 | ±10,0                            | 2.4<br>3.7<br>4.7    | 2.46<br>3.76<br>4.76            | a TRI-ST<br>Ce <b>y</b> ent<br>a log/ing | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $I_{OH}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |  |
| Vol. Vaa.            | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001                | 0.1<br>0.1<br>0.1    | 80<br>50                         | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1               | m Dynan<br>kurs <b>y</b> it              | I <sub>OUT</sub> = 50 μA   |  |
|                      | OV = M/V Au  | 3.0<br>4.5<br>5.5      |  | 0.36<br>0.36<br>0.36 | 180.0                            | 0.50<br>0.50<br>0.50 | 0.44<br>0.44<br>0.44            | inemi<br>inevalu<br>i byeal              | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA                                   |  |
| I <sub>IN</sub>      | Maximum Input<br>Leakage Current   | 5.5                    |  | ±0.1                 |                                  | ±1.0                 | ±1.0                            | μА                                       | V <sub>I</sub> = V <sub>CC</sub> , GND (Note)  |  |

<sup>\*</sup>Maximum of 9 outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Electrical Characteristics for 'AC Family Devices (Continued) This end of the Continued 
|                  |                                      |                        | 74AC                  |                    | 54AC                              | 74AC                            | ga wan | t mattery/Antrony  |  |
|------------------|--------------------------------------|------------------------|-----------------------|--------------------|-----------------------------------|---------------------------------|--------|--|--|
| Symbol Parameter |                                      | V <sub>CC</sub><br>(V) | T <sub>A</sub> =      | + 25°C             | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units  | Conditions   |  |
| to Voc           | /0                                   |                        | Typ Guaranteed Limits |                    |                                   |                                 |        | DC Input Diode Cu  |  |
| IOLD             | †Minimum Dynamic                     | 5.5                    | (oV) aga              | NoV Juglu          | 50                                | 75                              | mA     | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD             | Output Current                       | 5.5                    | isregms<br>Ti         | peraphy<br>744C/AI | -50                               | of V3.0 -75                     | mA     | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc              | Maximum Quiescent<br>Supply Current  | 5.5                    | Ti<br>put Edge        | 8.0                | 160.0                             | 80.0                            | μА     | V <sub>IN</sub> = V <sub>CC</sub> or GND (Note)                                |  |
| loz<br>an\vm     | Maximum TRI-STATE<br>Leakage Current | 5.5                    | 30% to<br>30% 4,5V.   | ±0.5               | ¥10.0                             | ±5.0                            | μА     | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |

<sup>\*</sup>Maximum of 9 outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

# **DC Electrical Characteristics for 'ACT Family Devices**

|                 |                                      |                        | 744              | ACT                    |              | 54ACT                             |                     | 74ACT                           | (LT) en                         | Junction Temperati   |  |
|-----------------|--------------------------------------|------------------------|------------------|------------------------|--------------|-----------------------------------|---------------------|---------------------------------|---------------------------------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | T <sub>A</sub> = +25°C |              | T <sub>A</sub> = -55°C to + 125°C |                     | T <sub>A</sub> = -40°C to +85°C | Units                           | Conditions   |  |
|                 |                                      |                        | Тур              |                        |              | Guarar                            | nteed L             | imits                           | The distaloped and a greateners | to the daylos may coaur.   |  |
| VIH             | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0             |              | 2.0                               | en ton av<br>enoths | 2.0<br>2.0                      | o brack                         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5       | 0.8                    | Herrig       | 0.8                               | 101                 | 0.8<br>0.8                      | ٧                               | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                                       |  |
| V <sub>OH</sub> | Minimum High Level Output Voltage    | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4             | = AT         | 4.4<br>5.4                        | 29°C                | 4.4<br>5.4                      | V                               | $I_{OUT} = -50 \mu\text{A}$  |  |
| 0.1V            | = TUOV                               | 4.5<br>5.5             | atimi            | 3.86<br>4.86           | Guard<br>2.1 | 3.70<br>4.70                      | t.s                 | 3.76<br>4.76                    | ere J rigil-                    | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = -24 \text{ mA}$ $V_{IOH} = -24 \text{ mA}$ |  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1             | 88.5         | 0.1<br>0.1                        | 2.85                | 0.1.                            | V                               | $I_{OUT} = 50 \mu A$   |  |
| - 0.13V         | - 00 V 10 V                          | 4.5<br>5.5             |                  | 0.36<br>0.36           | 1.35         | 0.50<br>0.50                      | 1.35                | 0.44                            | egs<br>V                        | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OL</sub> 24 mA<br>24 mA    |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1                   | 4.4          | ±1.0                              | 4,4<br>8.4          | 08.4<br>08.5 ±1.0               | μА                              | $V_I = V_{CC}$ , GND   |  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                  | ±0.5                   | 2.4          | ±10.0                             | 2.56                | ±5.0                            | μА                              | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |
| ICCT            | Maximum I <sub>CC</sub> /Input       | 5.5                    | 0.6              |                        | 4.7          | 1.6                               | 4.08                | 1.5                             | mA                              | $V_I = V_{CC} - 2.1V$  |  |
| lold 0          | †Minimum Dynamic                     | 5.5                    |                  |                        | 1.0          | 50                                | 0.1                 | 900.0 75                        | mA                              | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD            | Output Current                       | 5.5                    |                  |                        | 1.0          | -50                               | 1.0                 | 190.0 -75                       | mA                              | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc             | Maximum Quiescent<br>Supply Current  | 5.5                    |                  | 8.0                    | 00.0         | 160.0                             | 20.0                | 80.0                            | μА                              | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note)   |  |

<sup>\*</sup>Maximum of 9 outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note: I<sub>CC</sub> for 54ACT @ 25°C is identical to 74ACT @ 25°C.

|   | 7 |   |  |
|---|---|---|--|
| r | A |   |  |
| i |   | ì |  |

|                                      | -  |                                     |  | TOARB             |            | 74AC                             | MAY          | 54   | AC                      | 74         | AC                     |       |           |
|--------------------------------------|--|-------------------------------------|--|-------------------|------------|----------------------------------|--------------|------|-------------------------|------------|------------------------|-------|-----------|
| Symbol                               | etinU  | Parar                               | meter  | V <sub>CC</sub> * |            | A = +25<br>C <sub>L</sub> = 50 p |              | to + | −55°C<br>125°C<br>50 pF | to +       | -40°C<br>85°C<br>50 pF | Units | Fig       |
|                                      |  |                                     | 198  | miniki i          | Min        | Тур                              | Max          | Min  | Max                     | Min        | Max                    |       |           |
| t <sub>PLH</sub>                     |  | agation De<br>n to Bn, A            |  | 3.3<br>5.0        | 2.5<br>1.5 | 12.0<br>7.0                      | 15.0<br>10.0 |      | 8.6 PM                  | 2.5<br>1.5 | 15.5<br>10.5           | ns    | 1         |
| t <sub>PLH</sub><br>t <sub>PHL</sub> |  | agation De<br>R, BPAR to            | elay<br>BPAR, APAR   | 3.3<br>5.0        | 2.5<br>1.5 | 9.5<br>5.5                       | 12.0<br>8.0  |      | 3.6   9.6               | 2.5<br>1.5 | 12.5<br>8.5            | ns    | 1         |
| t <sub>PLH</sub><br>t <sub>PHL</sub> |  | agation De<br>n to BPAR             |  | 3.3<br>5.0        | 3.0<br>2.0 | 13.5<br>8.0                      | 16.5<br>11.0 |      | 0.8                     | 3.0<br>2.0 | 17.0<br>11.5           | ns    | 2         |
| t <sub>PLH</sub><br>t <sub>PHL</sub> |  | agation De<br>n to ERRA             |  | 3.3<br>5.0        | 2.5<br>1.5 | 12.5<br>7.5                      | 15.5<br>10.5 |      |                         | 2.5<br>1.5 | 16.5<br>11.0           | ns    | 3         |
| t <sub>PLH</sub>                     | And the State of t | agation De<br>/EVEN to              | elay<br>ERRA, ERRB   | 3.3<br>5.0        | 2.5<br>1.5 | 12.5<br>7.5                      | 15.5<br>10.5 | SOU  | SINSTO                  | 2.5<br>1.5 | 16.5<br>11.0           | ns    | 4         |
| t <sub>PLH</sub>                     |  | agation De<br>/EVEN to              | elay<br>APAR, BPAR   | 3.3               | 3.0<br>2.0 | 12.5<br>7.5                      | 15.5<br>10.5 | *20¥ |                         | 3.0<br>2.0 | 16.5<br>11.0           | ns    | 5<br>odmy |
| t <sub>PLH</sub>                     |  | agation De<br>R, BPAR to            | elay<br>ERRA, ERRB   | 3.3<br>5.0        | 2.0        | 12.5<br>7.5                      | 15.5<br>10.5 |      |                         | 2.0<br>1.5 | 16.5<br>11.0           | ns    | 6         |
| t <sub>PLH</sub>                     | 22.22  | agation De<br>to APAR, E            |  | 3.3<br>5.0        | 2.0        | 10.0                             | 12.5<br>8.5  | 5.0  |                         | 2.0        | 13.5                   | ns    | 9         |
| t <sub>PLH</sub>                     | 153.5  | agation De<br>LEA to A <sub>n</sub> |  | 3.3<br>5.0        | 4.0<br>2.5 | 12.0<br>7.0                      | 15.5<br>10.5 | 5.0  | RAFA                    | 4.0        | 16.5<br>11.0           | ns    | 10,       |
| t <sub>PLH</sub>                     | Sher and   | agation De<br>LEA to AP             | elay<br>PAR, BPAR  | 3.3<br>5.0        | 3.0        | 13.5<br>8.0                      | 17.0<br>11.5 | 5,0  |                         | 3.0<br>2.0 | 18.0<br>12.0           | ns    | 10,       |
| t <sub>PLH</sub><br>t <sub>PHL</sub> |  | agation De<br>LEA to EF             | RRA, ERRB  | 3.3<br>5.0        | 4.0<br>2.5 | 13.5<br>8.0                      | 17.0<br>11.5 | 5.0  |                         | 4.0<br>2.5 | 18.0<br>12.0           | ns    | 12        |
| t <sub>PZH</sub>                     |  | t Enable<br>GAB to A                | A CONTRACTOR OF THE PARTY OF TH | 3.3<br>5.0        | 3.0<br>2.0 | 12.5<br>7.5                      | 15.5<br>10.5 | 5,0  | SEP                     | 3.0        | 16.5<br>11.0           | ns    | 7, 8      |
| t <sub>PZL</sub>                     |  | GAB to A                            | Time<br>PAR, BPAR  | 3.3<br>5.0        | 2.5<br>1.5 | 10.5                             | 13.5<br>9.0  | 5.0  | FIAC                    | 2.5<br>1.5 | 14.0<br>9.5            | ns    | 7, 8      |
| t <sub>PHZ</sub>                     |  | ut Disable<br>GAB to A              |  | 3.3<br>5.0        | 1.5        | 11.0<br>6.5                      | 14.0<br>9.5  | 6.0  | era:                    | 1.5<br>1.0 | 14.0<br>9.5            | ns    | 7, 8      |
| t <sub>PHZ</sub><br>t <sub>PHL</sub> | -  | ut Disable<br>GAB to A              | Time<br>PAR, BPAR  | 3.3<br>5.0        | 1.5        | 11.0<br>6.5                      | 14.0<br>9.5  | 5,0  |                         | 1.5<br>1.0 | 14.0<br>9.5            | ns    | 7, 8      |
|                                      |  | .0 is 5.0V ±                        |  |                   |            |                                  | 2.5          |      |                         |            |                        |       |           |
| 10, 11                               | ange o   | 0.81                                | 0.5  |                   |            |                                  |              |      |                         |            |                        |       |           |
|                                      |  |                                     |  |                   |            |                                  |              |      |                         |            |                        |       |           |
| 7,8                                  |  |                                     |  |                   |            |                                  |              |      |                         |            |                        |       |           |
|                                      |  |                                     |  |                   |            |                                  |              |      |                         |            |                        |       |           |
|                                      |  |                                     |  |                   |            |                                  |              |      |                         |            |                        |       |           |
|                                      |  |                                     | 1.5  |                   |            |                                  |              |      |                         |            |                        |       |           |

| no. | - Allino rarameter  | (V)        | e fo  | C <sub>L</sub> = 50 pF | to + 125°C<br>C <sub>L</sub> = 50 pF | to +85°C<br>C <sub>L</sub> = 50 pF | Units      | Fig.    |
|-----|---|------------|-------|------------------------|--------------------------------------|------------------------------------|------------|---------|
|     | vett ett v  | 4.6        | , IS. | Guara                  | nteed Minimum                        |                                    |            |         |
| ts  | Setup Time, HIGH or LOW<br>An, Bn, PAR to LEA, LEB                          | 3.3<br>5.0 |       | 3.0                    | 3.3 8.8                              | 3.0<br>3.0                         | ns         | 11, 12  |
| th  | Hold Time, HIGH or LOW<br>A <sub>n</sub> , B <sub>n</sub> , PAR to LEA, LEB | 3.3<br>5.0 |       | 2.0<br>1.5             | 3.3 2.1                              | 2.0<br>1.5                         | ns         | 11, 12  |
| tw  | Pulse Width for LEA, LEB  | 3.3<br>5.0 |       | 4.0                    | 8.8 3.1                              | 4.0<br>4.0                         | ns         | 13      |
|     | 1 277 119   | -          | -     | 1 11 11 11 11 11       | 28 1 (12)                            | PRANT PARTE IN                     | WELL THE T | Fi.1031 |

\*Voltage Range 5.0 is 5.0V  $\pm 0.5$ V. Voltage Range 3.3 is 3.3V  $\pm 0.3$ V.

# **AC Electrical Characteristics**

|                                      | 1.5 11.0  |                       | 8.01 74 | ACT               | 8.8  | 54A  | СТ   | 74/  | CT                     | 1300  | JHS          |
|--------------------------------------|---|-----------------------|---------|-------------------|------|--|------|------|------------------------|-------|--------------|
| Symbol                               | Parameter   | V <sub>CC</sub> * (V) |         | + 25°(<br>= 50 pF |      | T <sub>A</sub> = -<br>to + 1<br>C <sub>L</sub> = | 25°C | to + | -40°C<br>85°C<br>50 pF | Units | Fig.         |
| 8                                    | o.17 8.1  |                       | Min o   | Гур               | Max  | Min  | Max  | Min  | Max                    | RARA  | PLH          |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>A <sub>n</sub> , B <sub>n</sub> to B <sub>n</sub> , A <sub>n</sub> | 5.0                   | 2.5     | 7.5               | 11.5 | 3.3  |      | 2.5  | 12.0                   | ns    | 14.15<br>Jan |
| t <sub>PLH</sub>                     | Propagation Delay<br>APAR, BPAR to BPAR , APAR  | 5.0                   | 1.5     | 6.0               | 8.5  | 3.3  |      | 1.5  | 9.0                    | ns    | 11           |
| t <sub>PLH</sub>                     | Propagation Delay<br>A <sub>n</sub> , B <sub>n</sub> to BPAR, APAR                      | 5.0                   | 2.5     | 8.5               | 12.0 | 3.3<br>5.0                                       | 8    | 2.5  | 12.5                   | ns    | 2            |
| t <sub>PLH</sub>                     | Propagation Delay<br>A <sub>n</sub> , B <sub>n</sub> to ERRA, ERRB                      | 5.0                   | 2.0     | 8.0               | 11.5 | 8,8  | 333  | 2.0  | 12.0                   | ns    | 3            |
| t <sub>PLH</sub>                     | Propagation Delay ODD/EVEN to ERRA, ERRB  | 5.0                   | 2.0     | 8.0               | 11.5 | 8.8  |      | 2.0  | 12.0                   | ns    | 4            |
| t <sub>PLH</sub>                     | Propagation Delay ODD/EVEN to APAR, BPAR  | 5.0                   | 2.5     | 8.0               | 11.5 | 3.3  |      | 2.5  | 12.0                   | ns    | 5            |
| t <sub>PLH</sub>                     | Propagation Delay APAR, BPAR to ERRA, ERRB  | 5.0                   | 1.5     | 7.5               | 10.5 | 8.6  | 740  | 1.5  | 11.5                   | ns    | 6            |
| t <sub>PLH</sub>                     | Propagation Delay SEL to APAR, BPAR   | 5.0                   | 1.5     | 6.5               | 9.0  | 8,8  |      | 1.5  | 9.5                    | ns    | 9            |
| t <sub>PLH</sub>                     | Propagation Delay<br>LEB to A <sub>n</sub> , B <sub>n</sub>                             | 5.0                   | 2.5     | 7.0               | 10.5 | 0.6  | HA   | 2.5  | 11.0                   | ns    | 10, 1        |
| t <sub>PLH</sub>                     | Propagation Delay<br>LEA to APAR, BPAR  | 5.0                   | 2.0     | 8.0               | 11.5 |  |      | 2.0  | 12.0                   | ns    | 10, 1        |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>LEA, LEB to ERRA, ERRB   | 5.0                   | 2.5     | 8.0               | 11.5 |  |      | 2.5  | 12.0                   | ns    | 12           |
| t <sub>PZH</sub>                     | Output Enable Time<br>GBA or GAB to A <sub>n</sub> , B <sub>n</sub>                     | 5.0                   | 2.5     | 7.0               | 10.5 |  |      | 2.5  | 11.0                   | ns    | 7, 8         |
| t <sub>PZH</sub>                     | Output Enable Time<br>GBA or GAB to BPAR or APAR  | 5.0                   | 1.5     | 6.0               | 9.0  |  |      | 1.5  | 9.5                    | ns    | 7, 8         |
| t <sub>PHZ</sub>                     | Output Disable Time<br>GBA or GAB to A <sub>n</sub> , B <sub>n</sub>                    | 5.0                   | 1.5     | 6.5               | 9.5  |  |      | 1.5  | 9.5                    | ns    | 7, 8         |
| t <sub>PHZ</sub>                     | Output Disable Time<br>GBA or GAB to BPAR, APAR   | 5.0                   | 1.5     | 6.5               | 9.5  |  |      | 1.5  | 9.5                    | ns    | 7, 8         |

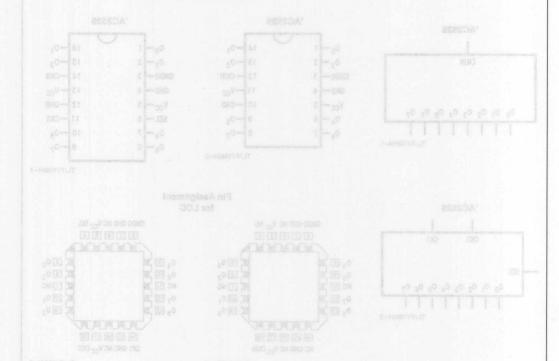
\*Voltage Range 5.0 is 5.0V  $\pm$  0.5V.

|                |  | (V) | C <sub>L</sub> = 50 pF | C <sub>L</sub> = 50 pF                     | C <sub>L</sub> = 50 pF  | Ollita | No.    |
|----------------|--|-----|------------------------|--|-------------------------|--------|--------|
|                |  |     | Guara                  | inteed Minimum                             | Dwall n                 | num    | niM    |
| t <sub>s</sub> | Setup Time, HIGH or LOW<br>A <sub>n</sub> , B <sub>n</sub> , PAR to LEA, LEB | 5.0 | 3.0                    | ok driver villin one                       | 3.0<br>minimum skow cir | ns     | 11, 12 |
| th             | Hold Time, HIGH or LOW<br>An, Bn, PAR to LEA, LEB                            | 5.0 | langle tol 1.5 hl m    | igned for signal gall<br>ions. The 2525 is | 1.5                     | ns     | 11, 12 |
| t <sub>w</sub> | Pulse Width for LEB, LEA   | 5.0 | 4.0                    | Farit attack painub a                      | 4.0                     | ns     | 13     |

<sup>\*</sup>Voltage Range 5.0 = 5.0V ±0.5V.

# Capacitance

| Symbol          | Parameter                        | Тур | Units | Conditions             |
|-----------------|----------------------------------|-----|-------|------------------------|
| CIN             | Input Capacitance                | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 210 | pF    | V <sub>CC</sub> = 5.0V |





### ADVANCE INFORMATION

# 54AC/74AC2525 • 54AC/74AC2526 Minimum Skew Clock Driver

The 'AC2525 is a minimum skew clock driver with one input driving eight outputs specifically designed for signal generation and clock distribution applications. The 2525 is designed to distribute a single clock to eight separate receivers with low skew across all outputs during both the TPLH and TPHL transitions. The AC2526 is similar to the AC2525 but contains a multiplexed clock input to allow for systems with dual clock speeds or systems where a separate test clock has been implemented.

#### **Features**

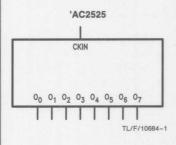
- Ideal for signal generation and clock distribution
- Guaranteed pin to pin and part to part skew
- Multiplexed clock input ('2526)
- Guaranteed 2000V minimum ESD protection
- 24 mA output drive capability

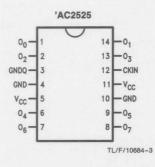
# **Logic Symbols**

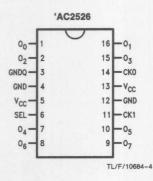
# **Connection Diagrams**

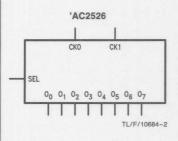
Pin Assignment for DIP, Flatpak and SOIC

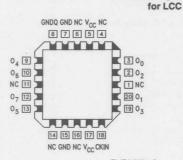
**Pin Assignment** 

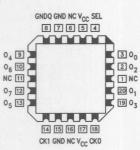












TL/F/10684-5

TL/F/10684-6



# 54AC/74AC2708 • 54ACT/74ACT2708 64 x 9 First-In, First-Out Memory

# **General Description**

The 'AC/'ACT2708 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out typical data rate makes it ideal for highspeed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset (MR) and Output Enable (OE) for initializing the internal registers and allowing the data outputs to be TRI-STATE®. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations. The status flags HF and FULL indicate when the FIFO is full, empty or half full.

The FIFO can be expanded to provide different word lengths by tying off unused data inputs.

#### **Features**

- 64-words by 9-bit dual port RAM organization
- 85 MHz shift-in, 60 MHz shift-out data rate, typical

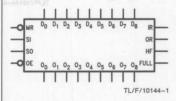
- Expandable in word width only
- 'ACT2708 has TTL-compatible inputs
- Asynchronous or synchronous operation
- Asynchronous master reset
- Outputs source/sink 8 mA
- TRI-STATE outputs
- Full ESD protection
- Input and output pins directly in line for easy board lavout
- TRW 1030 work-alike operation

# **Applications**

- High-speed disk or tape controllers
- A/D output buffers
- High-speed graphics pixel buffer
- Video time base correction
- Digital filtering

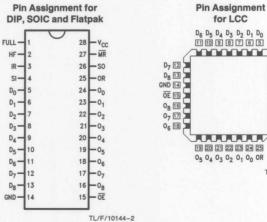
Ordering Code: See Section 8

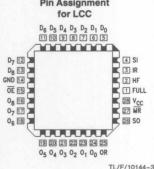
# **Logic Symbol**

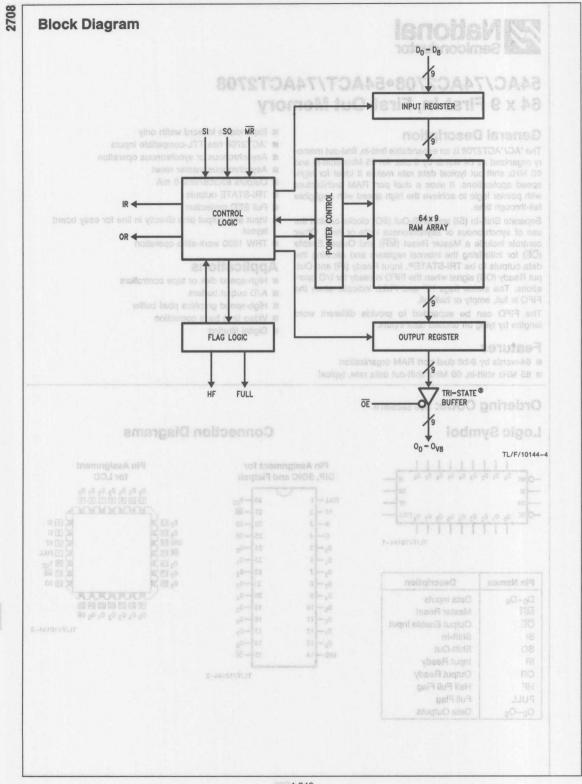


| Pin Names                      | Description         |
|--------------------------------|---------------------|
| D <sub>0</sub> -D <sub>8</sub> | Data Inputs         |
| MR                             | Master Reset        |
| ŌĒ                             | Output Enable Input |
| SI                             | Shift-In            |
| SO                             | Shift-Out           |
| IR                             | Input Ready         |
| OR                             | Output Ready        |
| HF                             | Half Full Flag      |
| FULL                           | Full Flag           |
| 00-08                          | Data Outputs        |

# **Connection Diagrams**







# **Functional Description**

#### INPUTS

#### Data Inputs (D<sub>0</sub>-D<sub>8</sub>)

Data inputs for 9-bit wide data are TTL-compatible. Word width can be reduced by trying unused inputs to ground and leaving the corresponding outputs open.

#### Reset (MR)

Reset is accomplished by pulsing the  $\overline{\text{MR}}$  input LOW. During normal operation  $\overline{\text{MR}}$  is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, OR goes LOW, FH and FULL go LOW. During reset, both internal read and write pointers are set to the first location in the array.

#### Shift-In (SI)

Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into an internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation. After the first word has been written into the FIFO, the falling edge of SI makes HF go HIGH, indicating a non-empty FIFO. The first data word appears at the output after the falling edge of SI. After half the memory is filled, the next rising edge of SI makes FULL go HIGH indicating a half-full FIFO. When the FIFO is full, any further shift-ins are disabled.

When the FIFO is empty and  $\overline{\text{OE}}$  is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

#### Shift-Out (SO)

Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t<sub>D</sub>. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

#### Output Enable (OE)

 $\overline{\text{OE}}$  LOW enables the TRI-STATE output buffers. When  $\overline{\text{OE}}$  is HIGH, the outputs are in a TRI-STATE mode.

#### **OUTPUTS**

#### Data Outputs (O<sub>0</sub>-O<sub>8</sub>)

Data outputs are enabled when  $\overline{\text{OE}}$  is LOW and in the TRI-STATE condition when  $\overline{\text{OE}}$  is HIGH.

#### Input Ready (IR)

IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

#### **Output Ready (OR)**

OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or empty and goes HIGH after the falling edge of the first shift-in.

#### Half-Full (HF)

This status flag along with the FULL status flag indicates the degree of fullness of the FIFO. On reset, HF is LOW; it rises on the falling edge of the first SI. The rising edge of the SI pulse that fills up the FIFO makes HF go LOW. Going from the empty to the full state with SO LOW, the falling edge of the first SI causes HF to go HIGH, the rising edge of the 33rd SI causes FULL to go HIGH, and the rising edge of the 64th SI causes HF to go LOW.

When the FIFO is full, HF is LOW and the falling edge of the first shift-out causes HF to go HIGH indicating a "non-full" FIFO.

#### **Full Flag (FULL)**

This status flag along with the HF status flag indicates the degree of fullness of the FIFO. On reset, FULL is LOW. When half the memory is filled, on the rising edge of the next SI, the FULL flag goes HIGH. It remains set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. The FULL flag then goes LOW on the rising edge of the next SO.

#### Status Flags Truth Table

| HF                | FULL            | Status Flag Condition |
|-------------------|-----------------|-----------------------|
| L                 | L. Sida in case | Empty                 |
| aire and Larrenge | Н               | Full                  |
| Н                 | L               | <32 Locations Filled  |
| Н                 | end H           | ≥32 Locations Filled  |

H = HIGH Voltage Level

L = LOW Voltage Level

#### Reset Truth Table

| 1  | nputs | 3  | HOM & Outputs TO has |    |    |      |       |  |  |  |  |
|----|-------|----|----------------------|----|----|------|-------|--|--|--|--|
| MR | SI    | so | IR                   | OR | HF | FULL | 00-08 |  |  |  |  |
| Н  | X     | X  | X                    | X  | X  | X    | X     |  |  |  |  |
| L  | X     | X  | Н                    | L  | L  | L    | L     |  |  |  |  |

H = HIGH Voltage Level

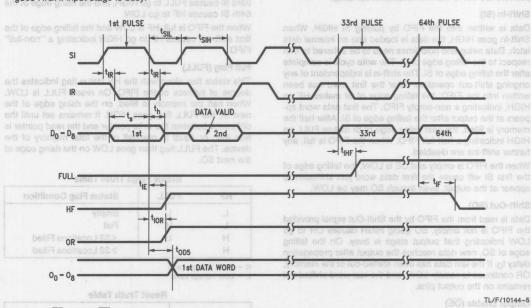
L = LOW Voltage Level

X = Immaterial

#### ...... .. coquence for FIFO Empty to Full

#### Sequence of Operation

- Input Ready is initially HIGH; HF and FULL flags are LOW. The FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data.
- Shift-In is set HIGH, and data is loaded into the FIFO.
   Data has to be settled t<sub>S</sub> before the falling edge of SI and held t<sub>h</sub> after.
- Input Ready (IR) goes LOW propagation delay t<sub>IR</sub> after SI goes HIGH: input stage is busy.
- output propagation delay  $t_{OD5}$  after SI falls. OR goes HIGH propagation delay  $t_{IOR}$  after SI goes LOW, indicating the FIFO has valid data on its outputs. HF goes HIGH propagation delay  $t_{IE}$  after SI falls, indicating the FIFO is no longer empty.
- 5. The process is repeated through the 64th data word. On the rising edge of the 33rd SI, FULL flag goes HIGH propagation delay t<sub>IHF</sub> after SI, indicating a half-full FIFO. HF goes LOW propagation delay t<sub>IF</sub> after the rising edge of the 64th pulse indicating that the FIFO is full. Any further shift-ins are disabled.



Note: SO and OE are LOW; MR is HIGH.

FIGURE 1. Modes of Operation Mode 1

# Mode 2: Master Reset

# Sequence of Operation 3H 38IA OR to entra political and

- Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset (MR) HIGH.
- Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t<sub>MRW</sub> before rising again.
- 3. Master Reset rises.

- 4. IR rises (if not HIGH already) to indicate ready to write state recovery time t<sub>MRIRH</sub> after the falling edge of MR. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t<sub>MRE</sub> and t<sub>MRO</sub> respectively after the falling edge of MR. OR falls recovery time t<sub>MRORL</sub> after MR falls. Data at outputs goes LOW recovery time t<sub>MRONL</sub> after MR goes LOW.
- Shift-In can be taken HIGH after a minimum recovery time t<sub>MRSIH</sub> after MR goes HIGH.

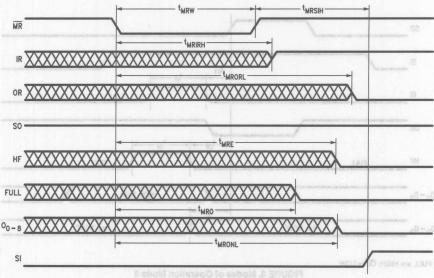


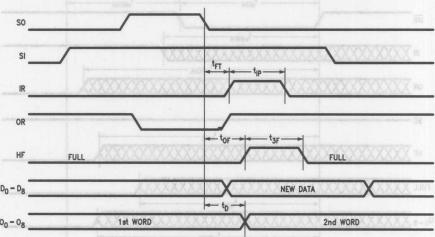
FIGURE 2. Mode of Operation Mode 2

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Mode 3: With FIFO Full, Shift-In is Held HIGH in Season File. In Anticipation of an Empty Location with the season states.

#### Sequence of Operation

- The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
- Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t<sub>D</sub>. New data is written into the FIFO after SO goes LOW.
- Input Ready goes HIGH one fall-through time, t<sub>FT</sub>, after the falling edge of SO. Also, HF goes HIGH one t<sub>OF</sub> after SO falls, indicating that the FIFO is no longer full.
- 4. IR returns LOW pulse width t<sub>IP</sub> after rising and shifting new data in. Also, HF returns LOW pulse width t<sub>3F</sub> after rising, indicating the FIFO is once more full.
- Shift-In is brought LOW to complete the shift-in process and maintain normal operation



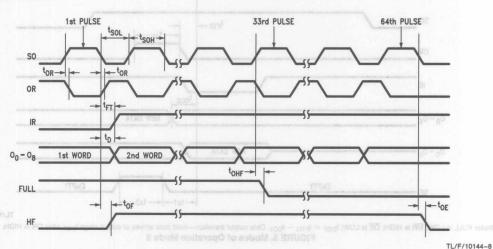
Note: MR and FULL are HIGH; OE is LOW.

FIGURE 3. Modes of Operation Mode 3

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# Mode 4: Shift-Out Sequence, FIFO Full to Empty Sequence of Operation

- 1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
- SO goes HIGH, resulting in OR going LOW one propagation delay, t<sub>OR</sub>, after SO rises. OR LOW indicates output stage is busy.
- SO goes LOW, new data reaches output one propagation delay, t<sub>D</sub>, after SO falls; OR goes HIGH one propagation delay, t<sub>OR</sub>, after SO falls and HF rises one propagation delay, t<sub>OF</sub>, after SO falls. IR rises one fall-through time, t<sub>FT</sub>, after SO falls.
- 4. Repeat process through the 64th SO pulse. FULL flag goes LOW one propagation delay, t<sub>OHF</sub>, after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW one propagation delay, t<sub>OE</sub>, after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.



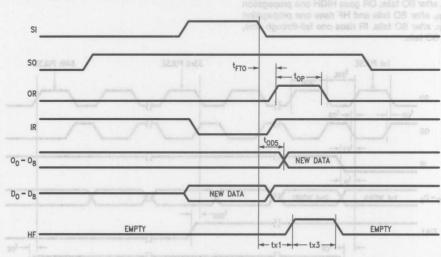
Note: SI and  $\overline{OE}$  are LOW;  $\overline{MR}$  is HIGH; D<sub>0</sub>-D<sub>8</sub> are immaterial.

FIGURE 4. Modes of Operation Mode 4

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

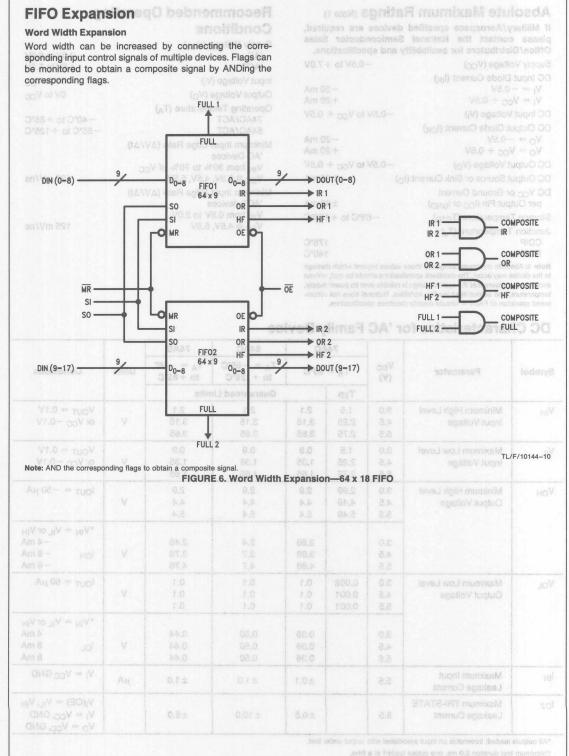
#### Sequence of Operation

- 1. FIFO is initially empty: Shift-Out goes HIGH.
- Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t<sub>x1</sub> after the falling edge of SI.
- OR rises a fall-through time of t<sub>FTO</sub> after the falling edge of Shift-In, indicating that new data is ready to be output.
- Data arrives at output one propagation delay, t<sub>OD5</sub>, after the falling edge of Shift-In.
- OR goes LOW pulse width t<sub>OP</sub> after rising and HF goes LOW pulse width t<sub>X3</sub> after rising, indicating that the FIFO is empty once more.
- 6. Shift-Out goes LOW, necessary to complete the Shift-Out



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Note: FULL is LOW; MR is HIGH;  $\overline{\text{OE}}$  is LOW;  $t_{\text{DOF}} = t_{\text{FTO}} - t_{\text{OD5}}$ . Data output transition—valid data arrives at output stage  $t_{\text{DOF}}$  after OR is HIGH.



### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V<sub>CC</sub>) -0.5V to +7.0V

DC Input Diode Current ( $I_{IK}$ )  $V_{I} = -0.5V$ 

 $V_{\rm I} = V_{\rm CC} + 0.5V$  + 20 mA DC Input Voltage (V<sub>I</sub>) -0.5V to  $V_{\rm CC} + 0.5V$ 

DC Output Diode Current (IOK)

DC Output Source or Sink Current (I<sub>O</sub>)
DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±32 mA torage Temperature (T<sub>STG</sub>) -65°C to +150°C

Storage Temperature (T<sub>STG</sub>)
Junction Temperature (T<sub>J</sub>)

CDIP 175°C 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

Supply Voltage (VCC)

'AC 2.0V to 6.0V
'ACT 4.5V to 5.5V
Input Voltage (V<sub>I</sub>) 0V to V<sub>CC</sub>
Output Voltage (V<sub>O</sub>) 0V to V<sub>CC</sub>

Operating Temperature (T<sub>A</sub>)

74AC/ACT -40°C to +85°C -55°C to +125°C

Minimum Input Edge Rate (ΔV/Δt)

'AC Devices

-20 mA

±32 mA

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub>

V<sub>CC</sub> @ 3.3V, 4.5V, 5.5V 125 mV/ns

Minimum Input Edge Rate (ΔV/Δt)

'ACT devices

V<sub>IN</sub> from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

# DC Characteristics for 'AC Family Device

| Symbol                             |                                      |                     | 74                      | AC                   | 54AC                                | 74AC                              |                  |  |  |
|------------------------------------|--------------------------------------|---------------------|-------------------------|----------------------|-------------------------------------|-----------------------------------|------------------|--|--|
| Symbol                             | Parameter                            | V <sub>CC</sub> (V) | TA                      | 25°C                 | T <sub>A</sub> = -55°C<br>to +125°C | T <sub>A</sub> = -40°<br>to +85°C | Units            | Conditions   |  |
| V <sub>IL</sub><br>V <sub>OH</sub> |                                      |                     | Тур                     |                      | Guaranteed Li                       | imits                             |                  |  |  |
| V <sub>IH</sub>                    | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85                 | 2.1<br>3.15<br>3.85               | V                | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> -0.1V  |  |
| V <sub>IL</sub>                    | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65                 | 0.9<br>1.35<br>1.65               | v<br>agail grabo | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> -0.1V  |  |
| V <sub>OH</sub>                    | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                   | 2.9<br>4.4<br>5.4                 | ٧                | $I_{OUT} = -50 \mu\text{A}$  |  |
|                                    |                                      | 3.0<br>4.5<br>5.5   |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                   | 2.46<br>3.76<br>4.76              | ٧                | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>-4 mA<br>I <sub>OH</sub> -8 mA<br>-8 mA |  |
| V <sub>OL</sub>                    | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                   | 0.1<br>0.1<br>0.1                 | ٧                | I <sub>OUT</sub> = 50 μA   |  |
|                                    |                                      | 3.0<br>4.5<br>5.5   |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50                | 0.44<br>0.44<br>0.44              | ٧                | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>4 mA<br>I <sub>OL</sub> 8 mA<br>8 mA    |  |
| I <sub>IN</sub>                    | Maximum Input<br>Leakage Current     | 5.5                 |                         | ±0.1                 | ±1.0                                | ±1.0                              | μА               | V <sub>I</sub> = V <sub>CC</sub> GND   |  |
| loz                                | Maximum TRI-STATE<br>Leakage Current | 5.5                 |                         | ±0.5                 | ±10.0                               | ±5.0                              |                  | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$                   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# 4

# DC Characteristics for 'AC Family Device (Continued) colored and account of the continued o

|        | 74AC                                | QA.                    | 74                    | AC   | DAI 54AC                             | 74AC                              | 7-17-1   |                              |
|--------|-------------------------------------|------------------------|-----------------------|------|--------------------------------------|-----------------------------------|----------|------------------------------|
| Symbol | Parameter                           | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C |      | T <sub>A</sub> = -55°C<br>to + 125°C | T <sub>A</sub> = -40°<br>to +85°C | Units    | Conditions                   |
| .001   | Ct 60 pF                            | 7q 08                  | Тур                   |      | Guaranteed L                         | .imits                            |          |                              |
| lold   | †Minimum Dynamic                    | 5.5                    | ultil                 | XBM  | 32                                   | 32                                | mA       | V <sub>OLD</sub> = 1.65V Max |
| IOHD   | Output Current                      | 5.5                    | 0.1                   | 16.5 | -32                                  | -32                               | mA       | V <sub>OHD</sub> = 3.85V Min |
| Icc    | Maximum Quiescent<br>Supply Current | 5.5                    | 1:0                   | 8.0  | 160                                  | 6.6 80 <sub>FI</sub>              | μА       | $V_{IN} = V_{CC}$ or GND     |
| ICCD   | Supply Current<br>20 MHz Loaded     | 5.5                    | 125                   | 150  | 4.5 12.0                             | e.e 150 and                       | ,vsmA no | f = 20 MHz<br>(Note 2)       |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54AC @ 25°C is identical to 74AC @ 25°C.

Note 2: Test load 50 pF,  $500\Omega$  to ground.

# **DC Electrical Characteristics for 'ACT Family Devices**

|                 | 3.5 23.6                            | 26.0                   | 54             | ACT          | 54ACT                               | 74ACT                             | tion Detai                       | property Property   |
|-----------------|-------------------------------------|------------------------|----------------|--------------|-------------------------------------|-----------------------------------|----------------------------------|---|
| Symbol          | Parameter                           | V <sub>CC</sub><br>(V) | 1.5            | = 25°C       | T <sub>A</sub> = -55°C<br>to +125°C | T <sub>A</sub> = -40°<br>to +85°C | Units                            | Conditions  |
| 8 8             | 6.0 28.5                            | 31.0                   | Тур            | 23.0         | Guaranteed Li                       | mits                              | A                                | or FIM  |
| V <sub>IH</sub> | Minimum High Level Input Voltage    | 4.5<br>5.5             | 1.5<br>1.5     | 2.0          | 2.0<br>2.0                          | 2.0                               | tion Dela                        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| VIL             | Maximum Low Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5     | 0.8          | 0.8                                 | 0.8                               | idon Dela<br>IF Flag             | $V_{OUT} = 0.1V$<br>or $V_{CC} = 0.1V$  |
| VoH             | Minimum High Level                  | 4.5<br>5.5             | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                          | 4.4<br>5.4                        | WV L                             | $I_{OUT} = -50 \mu\text{A}$   |
|                 | 17.0 79.5 F                         | 4.5<br>5.5             |                | 3.86<br>4.86 | 3.70<br>4.70                        | 3.76<br>4.76                      | widin, b                         | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> -8 mA -8 mA     |
| Vol             | Maximum Low Level Output Voltage    | 4.5<br>5.5             | 0.001<br>0.001 | 0.1          | 0.1                                 | 0.1<br>0.1                        | V<br>sleO noits                  | Ι <sub>ΟΟΤ</sub> = 50 μΑ  |
| s 3,4           | 7.0 50.6<br>6.5 32.6                | 4.5<br>5.5             | 1.0            | 0.32         | 0.40<br>0.40                        | 0.37                              | ata Out<br>atioryDela<br>ata Out | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>II</sub><br>I <sub>OL</sub> 8 mA<br>8 mA |
| IIN             | Maximum Input                       | 5.5                    | 1.0            | ±0.1         | 0.8 +1.0                            | ±1.0                              | μΑ                               | $V_I = V_{CC}$ , GND  |
| loz             | Maximum TRI-STATE Current           | 5.5                    | 1.5            | ±0.5         | ±10.0                               | ±5.0                              | μΑ                               | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |
| Гсст            | Maximum I <sub>CC</sub> /Input      | 5.5                    | 0.6            | 1.0          | 1.6                                 | 1.5                               | mA                               | $V_I = V_{CC} - 2.1V$   |
| lold =          | †Maximum Dynamic                    | 5.5                    | 0.1            | 17.0         | 32                                  | 32 80                             | mA                               | V <sub>OLD</sub> = 1.65V  |
| IOHD            | Output Current                      | 5.5                    | 6.7            | 9.81         | -32                                 | -32                               | mA                               | V <sub>OHD</sub> = 3.85V  |
| Icc             | Maximum Quiescent<br>Supply Current | 5.5                    |                | 8.0          | 160                                 | 80                                | μΑ                               | V <sub>IN</sub> = V <sub>CC</sub> or GND  |
| ICCD            | Supply Current<br>20 MHz Loaded     | 5.5                    | 125            | 150          |                                     | 150                               | mA                               | f = 20 MHz<br>(Note 2)  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

When  $\overline{\rm MR}$  is low with SO High, I<sub>CC</sub> > 1.5 mA.

Note 2: Test load 50 pF,  $500\Omega$  to ground.

<sup>†</sup>Maximum test duration 20 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Notes: I<sub>CC</sub> limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

# AC Characteristics: See Section 2 for waveforms 1/20 yillma 2 OA 107 2018 2018 2018 2019

|                                     | DAI  | 7           | DA.            | 74AC            |              | 54         | AC                      | 74           | IAC                      |       |                |
|-------------------------------------|--|-------------|----------------|-----------------|--------------|------------|-------------------------|--------------|--------------------------|-------|----------------|
| Symbol                              | Parameter 0.88   | *Vcc<br>(V) | A PARTICION OF | = +25<br>L = 50 |              | to +       | −55°C<br>125°C<br>50 pF | to +         | -40°C<br>-85°C<br>-50 pF | Units | Fig            |
| yeld Vää r                          | = auoV Am Se   |             | Min            | Тур             | Max          | Min        | Max                     | Min          | Max                      | 4     | -0.10          |
| tPLH V88.8                          | Propagation Delay, t <sub>IR</sub>                         | 3.3<br>5.0  | 2.5<br>1.5     | 8.5<br>5.5      | 16.5<br>11.5 | 1.0<br>1.5 | 20.0<br>15.0            | 2.0          | 18.5<br>12.5             | ns    | ant            |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>IR</sub>                         | 3.3<br>5.0  | 2.5            | 7.0<br>5.0      | 14.0<br>10.0 | 1.0<br>1.5 | 20.0<br>15.0            | 2.0          | 16.0<br>11.0             | ns    | 1              |
| tpLH                                | Propagation Delay, t <sub>IHF</sub>                        | 3.3<br>5.0  | 4.5<br>3.0     | 12.0<br>8.0     | 23.5<br>15.5 | 1.0<br>1.5 | 30.0<br>20.0            | 4.5<br>3.0   | 27.0<br>18.0             | ns    | 1              |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>IF</sub><br>SI to Full Condition | 3.3<br>5.0  | 5.0            | 11.5            | 22.0<br>15.0 | 1.0        | 28.0                    | 5.0<br>3.5   | 25.0<br>17.0             | ns    | banky<br>tarak |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>IE</sub><br>SI to Not Empty      | 3.3<br>5.0  | 4.5<br>3.0     | 11.5<br>8.0     | 23.5<br>15.5 | 1.0<br>1.5 | 29.0<br>20.0            | 4.5<br>3.0   | 26.5<br>17.5             | ns s  | sto1           |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>IOR</sub>                        | 3.3<br>5.0  | 4.5<br>3.0     | 13.5<br>9.0     | 30.5<br>20.0 | 1.0<br>1.5 | 39.0<br>26.0            | 4.5<br>3.0   | 34.5<br>23.0             | ns    | oa             |
| t <sub>PLH</sub>                    | Propagation Delay t <sub>MRIRH</sub>                       | 3.3         | 3.5<br>2.5     | 10.5<br>7.5     | 21.5         | 1.0<br>1.5 | 26.0<br>18.0            | 3.5<br>2.0   | 23.5<br>16.0             | ns    | 2              |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>MRORL</sub>                      | 3.3<br>5.0  | 7.5<br>6.0     | 18.5<br>12.0    | 35.5<br>23.0 | 1.0        | 45.0<br>31.0            | 7.5<br>6.0   | 41.0<br>26.5             | ns    | 2              |
| tphLV1.0 =                          | Propagation Delay t <sub>MRO</sub>                         | 3.3<br>5.0  | 4.0<br>2.5     | 9.0<br>6.5      | 18.0<br>12.5 | 1.0<br>1.5 | 24.0<br>17.0            | 4.0          | 21.5<br>15.0             | ns    | 2              |
| t <sub>PHL</sub> V <sub>1.0</sub> = | Propagation Delay t <sub>MRE</sub>                         | 3.3<br>5.0  | 8.5<br>7.0     | 20.0<br>13.5    | 39.5<br>26.0 | 1.0<br>4.0 | 49.0<br>33.0            | 8.5<br>6.5   | 44.5<br>29.5             | ns    | 2              |
| tPHL 08-                            | Propagation Delay, t <sub>MRONL</sub>                      | 3.3<br>5.0  | 3.5<br>2.0     | 9.5<br>7.0      | 19.5<br>14.0 | 1.0        | 25.0<br>18.0            | 3.5          | 21.5<br>15.5             | ns    | - 2            |
| V <sub>E, or V</sub> <b>w</b> t     | IR Pulse Width, t <sub>IP</sub>                            | 3.3<br>5.0  | 17.0<br>15.0   | 37.5<br>22.0    | 69.0<br>40.5 | 95-3       | 87.0<br>53.0            | 17.0<br>14.5 | 79.5<br>48.0             | ns    | 3              |
| tw 8-                               | HF Pulse Width t <sub>3F</sub>                             | 3.3<br>5.0  | 18.0<br>16.0   | 40.0<br>23.0    | 71.5<br>42.0 | 1086       | 92.0<br>56.0            | 18.0<br>15.5 | 84.0<br>50.5             | ns    | 3              |
| tPLH<br>MIV TO MV                   | Propagation Delay, t <sub>D</sub>                          | 3.3<br>5.0  | 7.0<br>5.5     | 20.5<br>13.5    | 41.5<br>26.0 | 1.0<br>3.5 | 55.0<br>37.0            | 7.0<br>5.0   | 47.5<br>31.0             | ns    | 3,             |
| t <sub>PHL</sub> 8                  | Propagation Delay, t <sub>D</sub>                          | 3.3<br>5.0  | 7.0<br>5.5     | 22.5<br>14.5    | 43.5<br>28.0 | 1.0<br>3.5 | 55.0<br>37.0            | 7.0<br>5.5   | 50.5<br>32.5             | ns    | 3,             |
| t <sub>PHL</sub> 110 .00            | Propagation Delay, t <sub>OHF</sub>                        | 3.3<br>5.0  | 4.0<br>2.5     | 9.0<br>6.5      | 17.5<br>12.0 | 1.0<br>1.5 | 23.0<br>16.0            | 4.0          | 20.5                     | ns    | 4              |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>OF</sub>                         | 3.3<br>5.0  | 5.5<br>4.0     | 14.5<br>10.0    | 29.0<br>19.0 | 1.0<br>2.5 | 36.0<br>24.0            | 5.5          | 33.0<br>22.0             | ns    | 3,             |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation Delay, t <sub>OR</sub>                         | 3.3<br>5.0  | 3.0            | 8.5<br>5.5      | 17.0<br>12.0 | 1.0<br>1.5 | 22.0<br>18.0            | 3.0          | 19.5<br>13.0             | ns    | _4             |

\*Voltage Range 3.3 is 3.3V  $\pm~0.3$ V

\*Voltage Range 5.0 is 5.0V  $\pm$  0.5V

|                  | ZAACT   | TOAN                 |              | 74AC   |              |              | 54AC                         | 74AC  |       |           |
|------------------|---|----------------------|--------------|--|--------------|--------------|------------------------------|---|-------|-----------|
| Symbol           | Parameter   | *V <sub>CC</sub> (V) |              | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              | to           | = -55°C<br>+125°C<br>= 50 pF | $T_A = -40^{\circ}C$<br>$to +85^{\circ}C$<br>$C_L = 50 pF$  | Units | Fig<br>No |
|                  | self riff   | eski –               | Min          | Тур  | Max          | Min          | Ma                           | x Min Max   |       |           |
| tPHL             | Propagation Delay, t <sub>OE</sub><br>SO to Empty         | 3.3<br>5.0           | 4.0<br>2.5   | 10.5<br>7.0                                      | 20.5<br>14.0 | 1.0<br>1.5   | 26.<br>19.                   | Sells of specimen a sensitivities with  | ns    | 4         |
| tpLH             | Propagation Delay, t <sub>OD5</sub><br>SI to New Data Out | 3.3<br>5.0           | 7.5<br>6.0   | 22.5<br>15.5                                     | 44.5<br>30.0 | 1.0<br>4.5   | 60.<br>39.                   | felly Conserve commentered  | ns    | 5         |
| tPHL             | Propagation Delay, t <sub>OD5</sub><br>SI to New Data Out | 3.3<br>5.0           | 7.5<br>6.0   | 21.5<br>14.5                                     | 42.0<br>28.5 | 1.0<br>4.5   | 60.<br>39.                   | Matter Other sector as a consequential sector   | ns    | 5         |
| t <sub>PLH</sub> | Propagation Delay, t <sub>X1</sub><br>SI to HF            | 3.3<br>5.0           | 4.0<br>2.5   | 11.5<br>8.0                                      | 23.0<br>15.5 | 1.0<br>1.5   | 29.<br>20.                   | -the tributures a presentable and a   | ns    | 5         |
| t <sub>PLH</sub> | Fall-Through Time, t <sub>FTO</sub><br>SI to OR           | 3.3<br>5.0           | 4.0<br>3.0   | 15.5<br>10.5                                     | 30.5<br>20.0 | 1.0<br>2.5   | 39.<br>26.                   | The Library of an artificials   | ns    | 5         |
| tw               | OR Pulse Width, t <sub>OP</sub>                           | 3.3<br>5.0           | 13.0<br>10.0 | 23.5<br>13.5                                     | 42.0<br>25.5 | 0,8          | 54.<br>34.                   | All the Advancer retreated for the  | ns    | 5         |
| tw               | HF Pulse Width, t <sub>x3</sub>                           | 3.3<br>5.0           | 15.0<br>12.0 | 27.0<br>16.0                                     | 49.5<br>30.0 | 0.6          | 63.40.                       | LIES VERME THEORY OF STREET   | ns    | 5         |
| t <sub>PLH</sub> | Fall-Through Time, t <sub>FT</sub><br>SO to IR            | 3.3<br>5.0           | 6.5<br>5.0   | 19.0<br>12.5                                     | 37.0<br>24.0 | 1.0          | 47.<br>31.                   | Walter May A Print and A State of the State | ns    | - 5       |
| t <sub>PZL</sub> | Output Enable  OE to On                                   | 3.3<br>5.0           | 2.5<br>1.5   | 7.0<br>5.0                                       | 14.0<br>10.0 | 1.0<br>1.5   | 21.0                         | The state of the same and a second district of a  | ns ns | 2-6       |
| t <sub>PLZ</sub> | Output Disable OE to On                                   | 3.3<br>5.0           | 2.0          | 4.5<br>3.5                                       | 9.0<br>7.0   | 1.0<br>1.5   | 0.8 17.0                     | The little of the same and a second state of the  | ns ns | 2-6       |
| t <sub>PZH</sub> | Output Enable OE to On                                    | 3.3<br>5.0           | 2.5<br>1.5   | 7.5<br>5.5                                       | 16.5<br>11.5 | 1.0<br>1.5   | 21.0                         | Skill the contract of the same of the   | ns    | 2-7       |
| t <sub>PHZ</sub> | Output Disable  OE to On                                  | 3.3<br>5.0           | 2.0          | 6.5  | 13.0         | 1.0          | 17.0                         |   | ns    | 2-7       |
| fsi<br>4,8 a     | Maximum SI Clock Frequency                                | 3.3<br>5.0           | 35.0<br>60.0 | 0.75   | 18.5         | 20.0<br>45.0 | 0.6                          | 30.0<br>50.0  | MHz   | HTd       |
| fso<br>a.s a     | Maximum SO Clock Frequency                                | 3.3<br>5.0           | 25.0<br>45.0 | 29.5   | 18.5         | 15.0<br>30.0 | 0.8                          | 20.0<br>35.0  | MHz   | JH9       |
| -                | ange 3.3 is 3.3V ± 0.3V<br>ange 5.0 is 5.0V ± 0.5V        |                      |              | 19.5   | 8.6          | 3.6          | 5.0                          | opagation Delay, totals to < HF   |       | .)Hql     |
|                  |   |                      |              |  |              |              |                              |   |       |           |
|                  |   |                      |              |  | 7.0          |              |                              |   |       |           |

# AC Characteristics: See Section 2 for waveforms (Continued)

|                                     |  | SAAC                    | 74ACT |  | 5    | 4ACT   | 74           | ACT  |      |       |          |
|-------------------------------------|--|-------------------------|-------|--|------|--|--------------|--|------|-------|----------|
| Symbol                              | Parameter  | *V <sub>CC</sub><br>(V) |       | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |              | $T_{A} = -40^{\circ}C$ $to +85^{\circ}C$ $C_{L} = 50 \text{ pF}$ |      | Units | Fig      |
|                                     | xaM niM x  | alif n                  | Min   | Тур  | Max  | Min  | Max          | Min  | Max  |       |          |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>IR</sub><br>SI to IR                   | F 0                     | 2.0   | 6.5  | 11.0 | 4.0  | 5.0          | 1.5  | 12.5 | ns ns | JHS<br>1 |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>IR</sub>                               | F 0                     | 2.0   | 6.5  | 11.0 | 7.5  | 5.0          | 1.5  | 12.0 | ns    | HJ       |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>IHF</sub>                              | FO                      | 4.0   | 10.5   | 17.0 | 7.6  | 8.8<br>8.0   | 4.0  | 19.5 | ns ns | JH       |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>IF</sub><br>SI to Full Condition       | FO                      | 4.5   | 10.5   | 16.5 | 4.0  | 8.3<br>5.0   | 4.5  | 19.5 | ns s  | HU       |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>IE</sub>                               | 50                      | 4.0   | 10.0   | 15.5 | 4.0  | 3.3<br>5.0   | 4.0  | 17.5 | ns s  | HU       |
| tpLH ar                             | Propagation Delay, t <sub>IOR</sub>                              | 5.0                     | 4.0   | 13.5   | 16.5 | 13.0   | 3.3<br>5.0   | 4.0  | 19.0 | ns    | V        |
| t <sub>PLH</sub>                    | Propagation Delay t <sub>MRIRH</sub>                             | 5.0                     | 3.0   | 8.5  | 13.5 | 15.0   | 6.8          | 3.0  | 15.5 | ns    | 1        |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>MRORL</sub>                            | 5.0                     | 7.0   | 16.5   | 25.5 | 6.5  | 3.3<br>5.0   | 7.0  | 29.0 | ns ns | HJ       |
| <sup>t</sup> PHL                    | Propagation Delay, t <sub>MRO</sub>                              | 5.0                     | 3.5   | 9.0  | 14.0 | 2.5  | 3.3          | 3.5  | 16.0 | ns    | 15       |
| <sup>t</sup> PHL                    | Propagation Delay, t <sub>MRE</sub>                              | 5.0                     | 8.0   | 17.5   | 27.5 | 0.S<br>0.1   | - 3,3<br>5,0 | 8.0  | 30.5 | ns    | 27       |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>MRONL</sub> MR to O <sub>n</sub> , LOW | 5.0                     | 3.0   | 9.0  | 15.0 | 2.5  | 8.8          | 3.0  | 17.0 | ns    | HCS      |
| tw                                  | IR Pulse Width, t <sub>IP</sub>                                  | 5.0                     | 16.5  | 28.0   | 43.0 | 0.8  | 8.8          | 16.5   | 51.5 | ns    | SH       |
| t <sub>W</sub>                      | HF Pulse Width, t <sub>3F</sub>                                  | 5.0                     | 17.5  | 30.0   | 46.5 | 0,1  | 5.0          | 17.5   | 56.0 | ns    |          |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>D</sub><br>SO to Data Out              | 5.0                     | 6.5   | 18.5   | 27.0 | 0.08   | 3.3          | 6.5  | 31.0 | ns    | 3,       |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>D</sub><br>SO to Data Out              | 5.0                     | 6.5   | 18.5   | 29.5 | 25.0   | 5.8          | 6.5  | 34.5 | ns ns | 3,       |
| t <sub>PHL</sub>                    | Propagation Delay, t <sub>OHF</sub><br>SO to < HF                | 5.0                     | 3.5   | 8.5  | 13.5 |  |              | 3.5  | 15.5 | ns    | Hov      |
| t <sub>PLH</sub>                    | Propagation Delay, t <sub>OF</sub><br>SO to Not Full             | 5.0                     | 5.0   | 12.5   | 19.5 |  |              | 5.0  | 22.0 | ns    | 3,       |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation Delay, t <sub>OR</sub><br>SO to OR                   | 5.0                     | 2.5   | 7.0  | 11.5 |  |              | 2.5  | 13.5 | ns    | 4        |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ± 0.5V

|                  |                      |   | D.A                  |      | 74ACT | THAC              | 54A   | CT  | 744       | 74ACT  |           |             |
|------------------|----------------------|---|----------------------|------|-------|-------------------|---|-----|-----------|--|-----------|-------------|
| Symbol           | Parameter of         |   | *V <sub>CC</sub> (V) |      |       |                   | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ |     | to +      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |           | Fig         |
|                  |                      | mum   | nteed Miln           | Min  | Тур   | Max               | Min   | Max | Min       | Max  |           |             |
| t <sub>PHL</sub> | Propaga<br>SO to E   | ation Delay, t <sub>OE</sub>                | 5.0                  | 3.5  | 9.5   | 15.5              | 9 6<br>9 0  |     | 3.0       | 17.5   | ns        | 4           |
| t <sub>PLH</sub> |                      | ation Delay, t <sub>OD5</sub><br>w Data Out | 5.0                  | 7.0  | 19.0  | 30.5              | 8 E.  |     | 6.0       | 35.5   | ns        | 5           |
| tPHL             |                      | ation Delay, t <sub>OD5</sub><br>w Data Out | 5.0                  | 7.0  | 19.0  | 29.5              | - ε<br>- ο.   | 3 8 | 6.0       | 34.5   | ns        | 5           |
| t <sub>PLH</sub> | Propaga<br>SI to HF  | ation Delay, t <sub>X1</sub>                | 5.0                  | 3.5  | 10.0  | 16.0              | Ε E.  | 8   | 2.5       | 18.0   | ns        | 5           |
| t <sub>PLH</sub> | Fall-Thr<br>SI to OF | ough Time, t <sub>FTO</sub>                 | 5.0                  | 3.5  | 13.5  | 21.0              | 8   |     | 1.5       | 24.0   | ns        | V           |
| tw               | OR Puls              | e Width, t <sub>OP</sub>                    | 5.0 0.               | 12.5 | 17.0  | 26.0              | A 6   |     | 12.5      | 30.5   | ns        | oe <b>5</b> |
| tw               | HF Puls              | e Width, t <sub>X3</sub>                    | 5.0                  | 14.5 | 20.5  | 30.5              | 8 0.  | 8   | 14.5      | 36.5   | ns        |             |
| tPLH             | Fall-Thr<br>SO to IF | ough Times, t <sub>FT</sub>                 | 5.0                  | 6.0  | 15.0  | 23.5              | 8.<br>8. 0.   | 8   | 2.5       | 28.0   | ns        | (H)W        |
| tpzL             | Output I             |   | 5.0                  | 2.0  | 6.5   | 11.0              | 8 0.  |     | 1.5       | 12.0   | ns        | 2-          |
| t <sub>PLZ</sub> | Output I             |   | 5.0                  | 1.5  | 5.0   | 8.5               |   |     | 1.5/2.0   | 9.5  | opneri eg | 2-          |
| t <sub>PZH</sub> | Output I             |   | 5.0                  | 2.0  | 7.0   | 12.0              | 8.  | nen | 1.5       | 13.0   | ns        | 2-          |
| t <sub>PHZ</sub> |                      | Disable n                                   | 5.0                  | 1.5  | 7.0   | 12.0              |   |     | 1.5       | 13.0   | ns        | 2-          |
| fsı              |                      | m SI<br>requency                            | 5.0                  | 55   | 85    | 45 = 75<br>2+ = N | 00  |     | 45        | Pars   | MHz       | ay and      |
| fso              |                      | equency                                     | 5.0                  | 42   | 60    | 9                 | T 0.  | a   | 35        | SI Pulse W   | MHz       | Has         |
| *Voltage R       | ange 5.0 is 5        | .0V ±0.5V                                   |                      |      |       |                   |   |     |           |  |           |             |
| 1                |                      |   |                      |      |       |                   |   |     |           |  |           |             |
|                  |                      |   |                      |      |       |                   |   |     |           |  |           |             |
|                  |                      |   |                      |      |       |                   |   |     |           |  |           |             |
|                  |                      |   |                      |      |       |                   |   |     |           | Recovery<br>VIF to SI  |           |             |
|                  |                      |   |                      |      |       |                   |   |     |           |  |           |             |
|                  |                      |   |                      |      |       |                   |   |     |           |  |           |             |
|                  |                      |   |                      |      |       |                   |   |     |           |  |           |             |
|                  |                      |   |                      |      |       |                   |   |     | Parameter |  |           |             |
|                  |                      |   |                      |      |       |                   |   |     |           |  |           |             |

# AC Operating Requirements (bounding) emolecown of 2 notice and 100 in a second of 2 notice and

|                    |     |   | STANCE      | 74A  | CTOAM        | 54AC  | 74AC  |          |             |
|--------------------|-----|---|-------------|--|--------------|---|---|----------|-------------|
| Symbol             |     | Parameter                                       | *Vcc<br>(V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |              | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40$ °C<br>to +85°C<br>$C_L = 50 \text{ pF}$ | Units    | Fig.<br>No. |
|                    |     | confirmation of                                 | esta Rase   | Тур о  |              | Guaranteed Mi   |   |          |             |
| t <sub>W</sub> (H) | en  | SI Pulse Width, t <sub>SIH</sub>                | 3.3<br>5.0  | 9.0<br>5.5                                       | 16.5<br>10.5 | 11.0<br>9.0   | 20.5<br>12.5  | ns       | .149        |
| t <sub>W</sub> (L) | en  | SI Pulse Width, t <sub>SIL</sub>                | 3.3<br>5.0  | 8.5<br>6.5                                       | 16.0<br>12.0 | 26.0<br>14.0  | 19.5 nose:  | ns       | H           |
| ts                 | 869 | Setup Time, HIGH or LOW, Dn to SI               | 3.3<br>5.0  | -2.0<br>-1.5                                     | 1.0          | 2.0<br>0.0  | agot (1.00 noting<br>ow DataO.htm                   | ns       | -14"        |
| tн                 | en  | Hold Time, HIGH or<br>LOW, D <sub>n</sub> to SI | 3.3         | 1.0<br>1.0                                       | 5.5<br>4.0   | 7.0<br>7.0  | 4.5 A   | ns       | 11          |
| tw                 | an  | MR Pulse Width, t <sub>MRW</sub>                | 3.3<br>5.0  | 13.0<br>8.5                                      | 26.0<br>16.0 | 34.0<br>22.0  | 30.5 Aguari<br>20.0                                 | ns       | 2           |
| t <sub>rec</sub>   | 201 | Recovery Time, t <sub>MRSIH</sub>               | 3.3<br>5.0  | 4.5<br>3.0                                       | 8.0          | 8.0   | 9.5<br>7.0  | ns<br>ns | 2           |
| t <sub>W</sub> (H) | 811 | SO Pulse Width, t <sub>SOH</sub>                | 3.3<br>5.0  | 4.0<br>2.5                                       | 7.5<br>5.5   | 24.0<br>0.0 15.0 0.0  | 8.5<br>6.5  | T-lins   | 4           |
| t <sub>W</sub> (L) | an  | SO Pulse Width, t <sub>SOL</sub>                | 3.3<br>5.0  | 10.0<br>6.0                                      | 18.0<br>12.0 | 23.0<br>16.0  | 21.0<br>14.0  | ns       | 4           |

<sup>\*</sup>Voltage Range 3.3 is 3.3V  $\pm$  0.3V

# **AC Operating Requirements**

| ns 2-5             |  | *Vcc<br>(V) | $^{\circ}V_{CC}$ $T_{A} = +25^{\circ}C$ $T_{A} = -8$ |      | 54ACT   | 74ACT  | Output  | ZHGI        |
|--------------------|--|-------------|--|------|---|--|---------|-------------|
| Symbol             | Parameter  |             |  |      | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | m Units | Fig.<br>No. |
| 4534               |  |             | Typ Guaranteed Mir                                   |      |   | m SQ mumin   | Maxim   | lso.        |
| t <sub>W</sub> (H) | SI Pulse Width, t <sub>SIH</sub>                 | 5.0         | 3.5  | 6.5  |   | 7.5 ***upe1  | ns      | 1           |
| t <sub>W</sub> (L) | SI Pulse Width, t <sub>SIL</sub>                 | 5.0         | 6.0  | 10.0 |   | 12.0   | ns      | 1           |
| ts                 | Setup Time, HIGH or<br>LOW, D <sub>n</sub> to SI | 5.0         | 1.0  | 3.5  |   | 4.5  | ns      | 1           |
| t <sub>H</sub>     | Hold Time, HIGH or<br>LOW, D <sub>n</sub> to SI  | 5.0         | 1.5  | 3.5  |   | 4.5  | ns      | 1           |
| t <sub>W</sub>     | MR Pulse Width, t <sub>MRW</sub>                 | 5.0         | 13.0   | 20.0 |   | 24.5   | ns      | 2           |
| t <sub>rec</sub>   | Recovery Time, t <sub>MRSIH</sub>                | 5.0         | 4.5  | 7.5  |   | 8.5  | ns      | 2           |
| t <sub>W</sub> (H) | SO Pulse Width, t <sub>SOH</sub>                 | 5.0         | 7.5  | 6.5  |   | 8.0  | ns      | 4           |
| t <sub>W</sub> (L) | SO Pulse Width, t <sub>SOL</sub>                 | 5.0         | 9.0  | 14.0 |   | 17.0   | ns      | 4           |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm~0.5V$ 

# Capacitance

| Symbol | Parameter         | Тур | Units | Conditions      |
|--------|-------------------|-----|-------|-----------------|
| CIN    | Input Capacitance | 4.5 | pF    | $V_{CC} = 5.0V$ |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ± 0.5V



# 54ACT/74ACT2725 512 x 9 First In, First Out Memory (FIFO)

# **General Description**

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, ring pointers for fall-through time; it is suited for high-speed applications.

# Master/stave multiprocessing applications

# Bidirectional and rate buffer applications

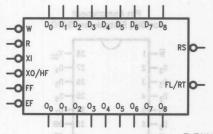
s 'ACT2728 has TTL-competible inputs

# Empty and full warning flags

#### **Features**

- First-in, first-out dual port memory
- 512 x 9 organization
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by word depth and/or bit width
- Half-full flag capability in single device mode
- Empty and full warning flags
- Auto retransmit capability A HENRY RIG ett ned
- Outputs source/sink 8 mA
- 'ACT2725 has TTL-compatible inputs
- Pin and functionality compatible with IDT7201A

# Logic Symbol manpaid noiteenno



TL/F/10138-3

| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>8</sub> | Data Inputs                   |
| 00-08                          | Data Outputs                  |
| W                              | Write Enable                  |
| R                              | Read Enable                   |
| XI                             | Expansion In                  |
| XO/HF                          | Expansion Out, Half-Full Flag |
| EF                             | Empty Flag                    |
| FF                             | Full Flag                     |
| RS                             | Reset                         |
| FL/RT                          | First Load/Retransmit         |

# Connection Diagram Indmy2 olgo.

Pin Assignment for DIP, Flatpak and SOIC

|                  | 0 20 1 | 0 10 10 | e0 | 18 80            |
|------------------|--------|---------|----|------------------|
| <u>w</u> -       | 1      | 0       | 28 | -v <sub>cc</sub> |
| D <sub>8</sub> - | 2      |         | 27 | -D <sub>4</sub>  |
| D <sub>3</sub> - | 3      |         | 26 | -D <sub>5</sub>  |
| D2-              | 4      |         | 25 | -D <sub>6</sub>  |
| D <sub>1</sub> - | 5      |         | 24 | -D <sub>7</sub>  |
| D <sub>0</sub> - | 6      |         | 23 | -FL/RT           |
| XI—              | 7      |         | 22 | - RS             |
| FF —             | 8      |         | 21 | — ĒĒ             |
| 00-              | 9      |         | 20 | - XO/HF          |
| 01-              | 10     |         | 19 | -07              |
| 02-              | 11     |         | 18 | -0 <sub>6</sub>  |
| 03-              | 12     |         | 17 | -05              |
| 08-              | 13     |         | 16 | -04              |
| GND —            | 14     |         | 15 | <b>−</b> R̄      |
|                  |        |         |    |                  |





# 54ACT/74ACT2726 512 x 9 Bidirectional First In, First Out Memory (BIFIFO)

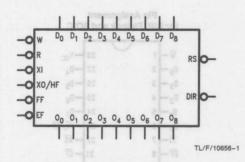
# **General Description**

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, and ring pointers for zero fall-through time. There are two sets of bidirectional ports, each 9 bits wide, through which data flow can be controlled. A direction pin (DIR) controls the direction of the data: when the DIR is HIGH, A is the input port and B is the output port. When the DIR is LOW, the input port is B and output port is A. It is suited for high-speed applications.

#### **Features**

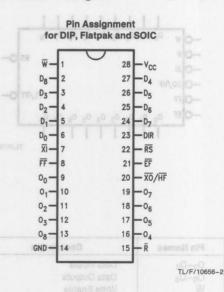
- First-in, first-out bidirectional memory
- 512 x 9 organization
- Low power consumption
- Asynchronous and simultaneous read and write
- Fully expandable by word depth and/or bit width
- Half-full flag capability in single device mode
- Master/slave multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and full warning flags
- Outputs source/sink 8 mA
- 'ACT2726 has TTL-compatible inputs

# Logic Symbol mangald notice and O



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>8</sub> | Data Inputs                   |
| 00-08                          | Data Outputs                  |
| W                              | Write Enable                  |
| R                              | Read Enable                   |
| XI                             | Expansion In                  |
| XO/HF                          | Expansion Out, Half-Full Flag |
| EF                             | Empty Flag                    |
| FF                             | Full Flag                     |
| RS                             | Reset                         |
| DIR                            | Direction                     |

# Connection Diagram Iodmy2 signal





#### Section 5 Contents

| 54ACTQ/74ACTQ153 Dual 4-Input Multiplexer   |
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| Quiet Series Datasheets   |
| 54ACQ/74ACQ373 Quiet Series Octal Transparent Latch with TRI-STATE Outputs 1.1.1.1.02 |
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|   |
| 54ACTQ/74ACTQ374 Quiet Series Octal D Flip-Flop with TRI-STATE Outputs                |
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| 54ACQ/74ACQ821 Quiet Series 19-8it D Flip-Flop with TRI-STATE Outputs                 |
| 54ACTQ/74ACTG827 Quiet Series 10-Bit Buffer/Line Driver with TRI-STATE Outputs        |
|   |
|   |



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# 54ACQ/74ACQ153 • 54ACTQ/74ACTQ153 Quiet Series Dual 4-Input Multiplexer

# **General Description**

The 'ACQ/'ACTQ153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'ACQ/'ACTQ153 can act as a function generator and generate any two functions of three variables.

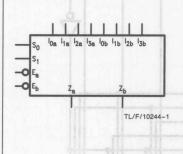
### **Features**

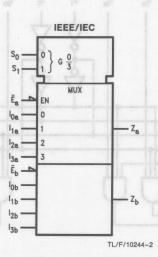
- Outputs source/sink 24 mA tuo sell not anoticupa sigot
- 'ACTQ153 has TTL-compatible inputs
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity

The information for the 'ACQ153 is advanced information only.

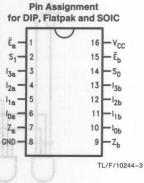
Ordering Code: See Section 8

# **Logic Symbols**

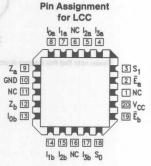




# **Connection Diagrams**



| Pin Names                        | Description          |
|----------------------------------|----------------------|
| I <sub>0a</sub> -I <sub>3a</sub> | Side A Data Inputs   |
| l <sub>0b</sub> -l <sub>3b</sub> | Side B Data Inputs   |
| S <sub>0</sub> , S <sub>1</sub>  | Common Select Inputs |
| Ēa                               | Side A Enable Input  |
| Ēb                               | Side B Enable Input  |
| Za                               | Side A Output        |
| Zb                               | Side B Output        |



TL/F/10244-4

# **Functional Description**

The 'ACQ/'ACTQ153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S<sub>0</sub>, S<sub>1</sub>). The two 4-input multiplexer circuits have individual active-LOW Enables ( $\overline{\mathsf{E}}_a$ ,  $\overline{\mathsf{E}}_b$ ) which can be used to strobe the outputs indepedently. When the Enables ( $\overline{\mathsf{E}}_a$ ,  $\overline{\mathsf{E}}_b$ ) are HIGH, the corresponding outputs  $\mathsf{Z}_a$ ,  $\mathsf{Z}_b$ ) are forced LOW. The 'ACQ/'ACTQ153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$\begin{split} Z_{a} &= \overline{E}_{a} \bullet (I_{0a} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1a} \bullet \overline{S}_{1} \bullet S_{0} + I_{2a} \bullet S_{1} \bullet S_{0}) \\ I_{2a} \bullet S_{1} \bullet \overline{S}_{0} + I_{3a} \bullet S_{1} \bullet S_{0}) \\ Z_{b} &= \overline{E}_{b} \bullet (I_{0b} \bullet \overline{S}_{1} \bullet \overline{S}_{0} + I_{1b} \bullet \overline{S}_{1} \bullet S_{0} + I_{2b} \bullet S_{1} \bullet \overline{S}_{0}) \end{split}$$

# Truth Table

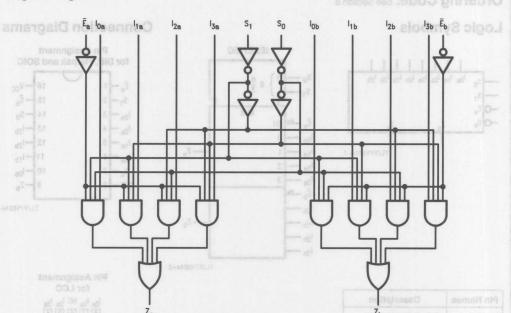
|                | ect            | Inputs (a or b) |                |                |                |                | Output  |
|----------------|----------------|-----------------|----------------|----------------|----------------|----------------|---------|
| S <sub>0</sub> | S <sub>1</sub> | Ē               | I <sub>0</sub> | J <sub>1</sub> | l <sub>2</sub> | l <sub>3</sub> | Z       |
| X              | X              | Н               | X              | X              | X              | X              | SP CL   |
| L              | FEL            | L               | L              | X              | X              | X              | IICL    |
| L              | L              | L               | Н              | X              | X              | X              | Н       |
| Н              | L              | L               | X              | also:          | X              | X              | TG GT   |
| Н              | ol-Liss        | b lgss          | X              | 5 H 8          | X              | X              | N' an H |
| Esta           | H              | pur pu          | X              | X              | se Cou         | X              | Ilw TeL |
| L              | H              | LOW             | X              | X              | Н              | X              | H       |
| Н              | Н              | L               | X              | X              | X              | L              | BOULON  |
| Н              | Н              | L               | X              | X              | X              | Н              | Н       |

H = HIGH Voltage Level

L = LOW Voltage Level

And notice X = Immaterial as a 681000 A sett not notice motel set?

# **Logic Diagram**



TL/F/10244-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

# Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales

| Office/Distributors for availab                       | ility and sp | ecifications.             |
|---|--------------|---------------------------|
| Supply Voltage (V <sub>CC</sub> )                     | 8 + 01 O O E | 0.5V to +7.0V             |
| DC Input Diode Current (IIK)                          |              | Suprembed Limi            |
| $V_{l} = -0.5V$                                       |              | -20 mA                    |
| $V_I = V_{CC} + 0.5V$                                 |              | + 20 mA                   |
| DC Input Voltage (V <sub>I</sub> )                    | -0.5V        | to V <sub>CC</sub> + 0.5V |
| DC Output Diode Current (IOK)                         |              | the second second second  |
| $V_0 = -0.5V$   |              | -20 mA                    |
| $V_O = V_{CC} + 0.5V$                                 |              | + 20 mA                   |
| DC Output Voltage (V <sub>O</sub> )                   | -0.5V to     | to V <sub>CC</sub> + 0.5V |
| DC Output Source<br>or Sink Current (I <sub>O</sub> ) |              | ±50 mA                    |
| DO V O  |              |                           |

DC V<sub>CC</sub> or Ground Current per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±50 mA -65°C to +150°C Storage Temperature (TSTG) DC Latch-Up Source or ±300 mA Sink Current

Junction Temperature (T<sub>J</sub>) CDIP PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recom-

mend operation of FACT™ circuits outside databook specifications.

# Recommended Operating Conditions

Supply Voltage (Vcc) 2.0V to 6.0V 'ACQ 4.5V to 5.5V 'ACTQ Input Voltage (V<sub>I</sub>) OV to VCC Output Voltage (Vo) OV to V<sub>CC</sub>

Operating Temperature (T<sub>A</sub>) 74ACQ/ACTQ -40°C to +85°C 54ACQ/ACTQ -55°C to +125°C

Minimum Input Edge Rate ΔV/Δt Maximum Quiescent 'ACQ Devices

VIN from 30% to 70% of VCC leve I right mumics 125 mV/ns V<sub>CC</sub> @3.0V, 4.5V, 5.5V

Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices

VIN from 0.8V to 2.0V V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

**DC Characteristics for 'ACT Family Devices** 

|                 |                                      |                        | 74A              | СТО          | 54ACTQ   | main. | 74ACTQ       | MED Ton              | AC Electric   |  |
|-----------------|--------------------------------------|------------------------|------------------|--------------|--|-------|--------------|----------------------|---|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = T <sub>A</sub> =<br>-55°C to + 125°C -40°C to +85°C |       | Units        | Conditions           |   |  |
|                 | T <sub>A</sub> = -40°C               |                        | Тур              | AT           | Guaranteed Limits  |       | *neV         |                      |   |  |
| VIH             | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0<br>2.0   | 2.0  |       | 2.0          | V                    | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8<br>0.8   | O E   | 0.8          | atio( <b>Y</b> toita | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4   | 0.6   | 4.4<br>5.4   | ation Dela           | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 | 2.0 12.5 ns                          | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70   | 0.8   | 3.76<br>4.76 | ation Dela           | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| Vols            | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1   | 8.9 0.1 0.8<br>0.1   | 0.8   | 0.1          | stich Deite          | $I_{OUT} = 50 \mu A$  |  |
| 2-3, 4          | en 0.fr 0.S                          | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50   | 3.8   | 0.44<br>0.44 | etion Dela<br>V      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | ±1.0   | 10.35 | ±1.0         | μА                   | $V_I = V_{CC}$ , GND  |  |

175°C

140°C

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

|  | Эq |  |
|--|----|--|

| Symbol           | Parameter Parameter                         | VCC<br>(V) | T <sub>A</sub> = | + 25°C    | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units     | Conditions  |  |
|------------------|---|------------|------------------|-----------|-----------------------------------|---------------------------------|-----------|---|--|
| V3.8 of V3.8     |   | Тур        |                  |           | Guaranteed Limits                 |                                 | ront (lat | DC Input Diode Cu                                 |  |
| ICCT             | Maximum I <sub>CC</sub> /Input              | 5.5        | 0.6              | loV tuqti | Am 08 -<br>1.6 08 +               | 1.5                             | mA        | $V_{\rm I} = V_{\rm CC} - 2.1V$                   |  |
| lold             | †Minimum Dynamic                            | 5.5        | ACTO             | COANT     | 50                                | 75                              | mA        | V <sub>OLD</sub> = 1.65V Max                      |  |
| I <sub>IHD</sub> | Output Current                              | 5.5        | DICA             |           | -50                               | -75                             | mA        | V <sub>OHD</sub> = 3.85V Min                      |  |
| Icc              | Maximum Quiescent<br>Supply Curent          | 5.5        | ivices<br>30% to | 8.0       | 160.0                             | 80.0                            | μА        | V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1) |  |
| VOLP             | Maximum High Level Output Noise             | 5.0        | /8.8.V0          | 1.5       | M Am 08±                          |                                 | V (c      | Figures 1, 2<br>(Note 2, 3)                       |  |
| V <sub>OLV</sub> | Maximum Low Level<br>Output Noise           | 5.0        | -0.6             | -1.2      | £80 mA                            | lo lo                           | V         | Figures 1, 2                                      |  |
| V <sub>IHD</sub> | Maximum High Level Dynamic Input Voltage    | 5.0        | 1.9              | 2.2       | Am 006±                           |                                 | V a       | (Notes 2, 4)                                      |  |
| V <sub>ILD</sub> | †Maximum Low Level<br>Dynamic Input Voltage | 5.0        | 1.2              | 0.8       | 175°C                             |                                 | (LTV en   | (Notes 2, 4)                                      |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# AC Electrical Characteristics: See Section 2 for Waveforms

| enoitib             | G Units Con  | 36 + of           | )°08- | 74ACTQ  | - 88°C   | 54   | ACTQ   | 74A | СТО   |        | Symbo  |
|---------------------|--|-------------------|-------|---------|--|------|--|-----|-------|--------|--------|
| Symbol              | Parameter  | V <sub>CC</sub> * |       |         | $T_{A} = -55^{\circ}C$ to +125°C $C_{L} = 50 \text{ pF}$ |      | $T_{A} = -40^{\circ}C$ $to +85^{\circ}C$ $C_{L} = 50 \text{ pF}$ |     | Units | Fig.   |        |
| V1.0 -              |  | 0.5               | Min   | Тур     | Max  | Min  | Max  | Min | Max   | avel 4 | . 37   |
| tpLH1.0 -           | Propagation Delay S <sub>n</sub> to Z <sub>n</sub> | 5.0               | 3.0   | 7.0 8.0 | 11.5   | 8.0  | 8 1.5  | 2.0 | 13.5  | ns     | 2-3, 4 |
| t <sub>PHL</sub>    | Propagation Delay S <sub>n</sub> to Z <sub>n</sub> | 5.0               | 3.0   | 7.0     | 11.5   | 5.4  | 5 5.49   | 2.5 | 13.5  | ns     | 2-3, 4 |
| t <sub>PLH</sub> -  | Propagation Delay<br>En to Zn                      | 5.0               | 2.0   | 6.5     | 10.5   | 8.86 | 70.70  | 2.0 | 12.5  | ns     | 2-3, 4 |
| t <sub>PHL</sub> 08 | Propagation Delay $\overline{E}_n$ to $Z_n$        | 5.0               | 3.0   | 6.0     | 9.5  | 0.1  | 5 0.001<br>5 0.001   | 2.5 | 11.0  | ns     | 2-3, 4 |
| tpLHo JV            | Propagation Delay                                  | 5.0               | 2.5   | 5.5     | 9.5  | 88.0 | ä  | 2.0 | 11.0  | ns     | 2-3, 4 |
| t <sub>PHL</sub>    | Propagation Delay                                  | 5.0               | 2.0   | 5.5     | 9.5  | 86,0 | 9  | 2.0 | 11.0  | ns     | 2-3, 4 |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 65.0 | pF    | V <sub>CC</sub> = 5.0V |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of Data Inputs defined as (n). n-1 Data Inputs are driven 0V to 5V. One Data Input @  $V_{IN} = GND$ .

Note 4: Max number of Data Inputs (n) switching. (n - 1) Inputs switching 0V to 5V ('ACTQ). Input-under-test switching: 5V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ), f = 1 MHz.

# 54ACQ/74ACQ240 • 54ACTQ/74ACTQ240 Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

# **General Description**

The 'ACQ/'ACTQ240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series<sup>TM</sup> features GTO<sup>TM</sup> output control and undershoot corrector in addition to a split ground bus for superior performance.

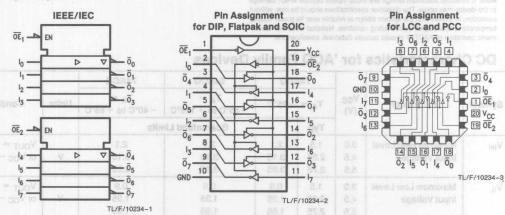
# **Features**

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT240
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

# **Logic Symbol**

# **Connection Diagrams**



| Pin Names                          | Description                    |  |  |
|------------------------------------|--------------------------------|--|--|
| $\overline{OE}_1, \overline{OE}_2$ | TRI-STATE Output Enable Inputs |  |  |
| 10-17                              | Inputs                         |  |  |
| $\overline{O}_0 - \overline{O}_7$  | Outputs                        |  |  |

# **Truth Tables**

| Inpu            | its | Outputs             |  |  |
|-----------------|-----|---------------------|--|--|
| OE <sub>1</sub> | In  | (Pins 12, 14, 16, 1 |  |  |
| easL -          | Le  | Н                   |  |  |
| 88.8L           | H.  | L                   |  |  |
| BB.AH           | X   | Z                   |  |  |

| Inp             | uts 8.5 | Outputs           |
|-----------------|---------|-------------------|
| OE <sub>2</sub> | a In    | (Pins 3, 5, 7, 9) |
| L               | L       | Н                 |
| 96'0 F          | O.H     | L                 |
| H 0.36          | X       | Z                 |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

# Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for availab        | onity and specifications.       |
|---|---------------------------------|
| Supply Voltage (V <sub>CC</sub> )       | -0.5V to $+7.0$ V               |
| DC Input Diode Current (IIK)            |                                 |
| $V_1 = -0.5V$                           | -20 mA                          |
| $V_1 = V_{CC} + 0.5V$                   | + 20 mA                         |
| DC Input Voltage (V <sub>I</sub> )      | $-0.5$ V to $V_{CC} + 0.5$ V    |
| DC Output Diode Current (IOK)           |                                 |
| $V_0 = -0.5V$                           | oonallumie beelins -20 mA       |
| $V_O = V_{CC} + 0.5V$                   | + 20 mA                         |
| DC Output Voltage (V <sub>O</sub> )     | $-0.5$ V to to $V_{CC} + 0.5$ V |
| DC Output Source                        |                                 |
| or Sink Current (I <sub>O</sub> )       | ±50 mA                          |
| DC V <sub>CC</sub> or Ground Current    |                                 |
| per Output Pin (ICC or IGND)            | ±50 mA                          |
| Storage Temperature (T <sub>STG</sub> ) | -65°C to +150°C                 |
|   |                                 |

PDIP

140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

DC Latch-Up Source or

Sink Current Junction Temperature (T<sub>J</sub>)

CDIP

# Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> ) 'ACQ                        | 2.0V to 6.0V                      |
|---|-----------------------------------|
| 'ACTQ   | 4.5V to 5.5V                      |
| Input Voltage (V <sub>I</sub> )                               | OV to V <sub>CC</sub>             |
| Output Voltage (V <sub>O</sub> )                              | OV to V <sub>CC</sub>             |
| Operating Temperature (T <sub>A</sub> ) 74ACQ/ACTQ 54ACQ/ACTQ | -40°C to +85°C<br>-55°C to +125°C |
| Minimum Input Edge Rate ΔV/Δt<br>'ACQ Devices                 | the AUU/AUT(                      |

 $V_{IN}$  from 30% to 70% of VCC  $V_{CC} @ 3.0V, 4.5V, 5.5V$  125 mV/ns Minimum Input Edge Rate  $\Delta V/\Delta t$ 

'ACTQ Devices
V<sub>IN</sub> from 0.8V to 2.0V
V<sub>CC</sub> @ 4.5V, 5.5V
125 mV/ns

# DC Characteristics for 'ACQ Family Devices

|                 |   | 0                      | 74                      | ACQ                  | 54ACQ                             | 74ACQ                           |       |   |  |
|-----------------|---|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|---|--|
| Symbol          | Parameter  Minimum High Level Input Voltage | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions  |  |
|                 |   |                        | Тур                     |                      | Guaranteed Lin                    | mits                            | 10    | Jul   |  |
| V <sub>IH</sub> |   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | V     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage          | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | ٧     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage        | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu\text{A}$   |  |
| (8)             | (Pins 12, 14, 16<br>H<br>L<br>L             | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | V     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$<br>-12  mA<br>$I_{OH}$ $-24 \text{ mA}$<br>-24  mA                  |  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage            | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | ٧     | Ι <sub>ΟΟΤ</sub> = 50 μΑ  |  |
|                 | Z<br>1<br>H                                 | 3.0<br>4.5<br>5.5      | um Consider             | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              | 0.44<br>0.44<br>0.44            | ٧     | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}O_L$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ |  |

±300 mA

175°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# 

|                  |   | BACTE                  | 74                     | ACQ    | 54ACQ                             | 7.0                             | 74ACQ |             |           |  |  |  |
|------------------|---|------------------------|------------------------|--------|-----------------------------------|---------------------------------|-------|-------------|-----------|--|--|--|
| Symbol           | Maximum Input Leakage Current                   | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |        | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C |       |             | Units     | Conditions   |  |  |
|                  |   |                        | Тур                    | beates | Guaranteed Li                     | imits                           |       |             |           |  |  |  |
| IN HI            |   | 5.5                    |                        | ±0.1   | ± 1.0 0±                          | ±1.0                            |       |             | μА        | V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)  |  |  |
| lold             | †Minimum Dynamic                                | 5.5                    |                        |        | 50                                |                                 | 75    |             | mA        | V <sub>OLD</sub> = 1.65V Max   |  |  |
| IOHD             | Output Current                                  | 5.5                    |                        | 0      | -50                               | 8.0                             | -75   |             | mA        | V <sub>OHD</sub> = 3.85V Min   |  |  |
| Icc Vaa          | Maximum Quiescent<br>Supply Current             | 5.5                    |                        | 8.0    | 160.0                             |                                 | 80.0  | 0           | μА        | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)                                       |  |  |
| loz<br>(1 elo    | Maximum TRI-STATE<br>Leakage Current            | 5.5                    |                        | ±0.5   | ±10.0),8                          |                                 | ±5.0  | te          | μА        | $V_{I}$ (OE) = $V_{IL}$ , $V_{IH}$<br>$V_{I}$ = $V_{CC}$ , GND<br>$V_{O}$ = $V_{CC}$ , GND |  |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1.1                    | 1.5    | 1.5                               | 1.1                             | 5,0   | lev         | V         | Figures 1, 2 (Notes 2, 3)  |  |  |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6                   | -1.2   | -1,2                              | 8.0-                            | 5.0   | İst         | Low Lev   | Figures 1, 2<br>(Notes 2, 3)   |  |  |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage     | 5.0                    | 3.1                    | 3.5    | 2.2                               | 1.0                             | 6.0   | la<br>egzi  | fight Lev | (Notes 2, 4) CHIV  |  |  |
| V <sub>ILD</sub> | Maximum Low Level<br>Dynamic Input Voltage      | 5.0                    | 1.9                    | 1.5    | 8.0                               | 2.1                             | 5.0   | ler<br>tage | Lov Lei   | (Notes 2, 4)   |  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# **DC Characteristics for 'ACTQ Family Devices**

|                 | 0°04 - = 40°0   |                        | 744                          | CTQ          | 54ACTQ                           | 74ACTQ                          |                               |   |  |
|-----------------|---|------------------------|------------------------------|--------------|----------------------------------|---------------------------------|-------------------------------|---|--|
| Symbol          | Parameter  Minimum High Level Input Voltage             | V <sub>CC</sub><br>(V) |                              |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                         | Conditions  |  |
|                 |   |                        | Тур                          | rilla        | Guaranteed Li                    | mits                            |                               |   |  |
| V <sub>IH</sub> |   | 4.5<br>5.5             | 1.5<br>1.5                   | 2.0<br>2.0   | 2.0                              | 2.0                             | output                        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| 2-5, 6          | Maximum Low Level Input Voltage                         | 4.5<br>5.5             | 1.5<br>1.5                   | 0.8          | 0.8                              | 0.8                             | Set Vale                      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| Vон             | Minimum High Level Output Voltage                       | 4.5<br>5.5             | 4.49<br>5.49                 | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | Divid                         | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 | 1.6<br>1.0  | 4.5<br>5.5             |                              | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | to Output                     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| VoL             | Maximum Low Level Output Voltage                        | 4.5<br>5.5             | 0.001<br>0.001               | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1<br>0.1                      | 8.0 <b>V</b> 0.8              | ΙΟὖΤ = 50 μA  |  |
| notholito       | to of the same davice. The ap-<br>guaranteed by dealgn. | 4.5<br>5.5             | y hito sepel<br>I (tosua). P | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | inulocda ar<br>goinstiwa<br>V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| IIN             | Maximum Input<br>Leakage Current                        | t 5.5                  |                              | ±0.1         | ±1.0                             | ±1.0                            | μΑ                            | $V_{I} = V_{CC}$ , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n -1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  |   | (4) |      |           | -55°C to + 125°C | -40°C to | +85°C     |                 | - Conditions   |
|------------------|---|-----|------|-----------|------------------|----------|-----------|-----------------|--|
|                  |   |     | Тур  | ranseed I | Guaranteed L     | imits    |           |                 |  |
| loz              | Maximum TRI-STATE<br>Leakage Current        | 5.5 |      | ±0.5      | ±10.00±          | ±5.0     | 0         | μА              | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$        |
| ГССТ             | Maximum I <sub>CC</sub> /Input              | 5.5 | 0.6  | 50        | 1.6              | 1.5      | 0         | mA              | $V_I = V_{CC} - 2.1V$                                |
| lold             | †Minimum Dynamic                            | 5.5 |      | 0.0       | 50               | 75       | to        | mA              | V <sub>OLD</sub> = 1.65V Max                         |
| IOHD             | Output Current                              | 5.5 |      |           | -50              | -78      |           | mA              | V <sub>OHD</sub> = 3.85V Min                         |
| Icc              | Maximum Quiescent<br>Supply Current         | 5.5 |      | 8.0       | ± 160.0 ±        | 80.0     | 311       | μА              | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |
| VOLP             | Maximum High Level Output Noise             | 5.0 | 1.1  | 1.5       | 8,1              | 5.0 1.1  | loV.      | V 213           | Figures 1, 2<br>(Note 2, 3)                          |
| V <sub>OLV</sub> | Maximum Low Level<br>Output Noise           | 5.0 | -0.6 | -1.2      | 9.1-             | 5.0 -0.8 | You       | v Ru<br>Dynamic | Figures 1, 2 (Notes 2, 3)                            |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage | 5.0 | 1.9  | 2.2       | 3.5              | 6.0 8.1  | te<br>age | . V             | (Notes 2, 4)   |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage     | 5.0 | 1.2  | 0.8       | 1.5              | 5.0 1.8  | le<br>egs | V               | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# AC Electrical Characteristics: See Section 2 for Waveforms

| Symbol                              | Parameter                                    | V <sub>CC</sub> * | 74ACQ<br>T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |             | 54ACQ<br>T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |                  | 74ACQ<br>T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |             | Units | Fig.   |
|-------------------------------------|--|-------------------|---|------------|-------------|---|------------------|---|-------------|-------|--------|
| Cymbol                              | 0.88   |                   |   |            |             |   |                  |   |             |       |        |
|                                     |  |                   | Min   | Тур        | Max         | Min   | Max              | Min   | Max         |       |        |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>Data to Output          | 3.3<br>5.0        | 2.0<br>1.5  | 7.0<br>5.0 | 10.0<br>6.5 | 0.S<br>0.S  | 5 1.5<br>6 1.5   | 2.0<br>1.5  | 10.5<br>7.0 | ns    | 2-3, 4 |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                           | 3.3<br>5.0        | 2.5<br>1.5  | 8.0<br>5.5 | 12.0<br>8.0 | 8.0   | 6 1.6<br>6 1.5   | 2.5<br>1.5  | 12.5<br>8.5 | ns    | 2-5, 6 |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                          | 3.3<br>5.0        | 1.0<br>1.0  | 8.5<br>6.0 | 13.5<br>9.0 | 8,8<br>8,4  | 5 4,49<br>5 5,49 | 1.0<br>1.0  | 14.0<br>9.5 | ns    | 2-5, 6 |
| toshl,<br>toslh                     | Output to Output<br>Skew**<br>Data to Output | 3.3<br>5.0        |   | 1.0<br>0.5 | 1.5<br>1.0  | 9.80<br>4.86  | 9 00             | 4.  | 1.5<br>1.0  | ns    |        |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V Voltage Range 3.3 is 3.3  $\pm 0.3$ V.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of Data Inputs defined as (n). n-1 Data Inputs are driven 0V to 3V. One Data Input @  $V_{IN} = GND$ .

Note 4: Max number of Data Inputs (n) switching, (n-1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold  $(V_{ILD})$ , 0V to threshold  $(V_{IHD})$ , f=1 MHz.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshL) or LOW to HIGH (tosth). Parameter guaranteed by design.

| Symbol                              | Parameter                                    | V <sub>CC</sub> * | -   | = +25°C<br>= 50 pF | 7\0 | to +                      | -55°C<br>125°C<br>50 pF | T <sub>A</sub> = -<br>to +8<br>C <sub>L</sub> = 9 | 35°C | Units | Fig.<br>No.                         |
|-------------------------------------|--|-------------------|---|--------------------|-----|---------------------------|-------------------------|---|------|-------|-------------------------------------|
|                                     |  |                   | Min   | Тур                | Max | Min                       | Max                     | Min   | Max  | e2 1: | ino                                 |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>Data to Output          | 5.0               | 1.5   | 5.5                | 7.0 | 1.5                       | 9.0                     | 1.5   | 7.5  | ns    | 2-3, 4                              |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                           | 5.0               | 1.5   | 6.5                | 8.5 | 1.5                       | 11.0                    | 1.5   | 9.0  | ns    | 2-5, 6                              |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                          | 5.0               | 1.0   | 7.0                | 9.5 | 1.5                       | 10.0                    | 1.0   | 10.0 | ns    | 2-5, 6                              |
| toshl,<br>toslh                     | Output to Output<br>Skew**<br>Data to Output | 5.0               | eq bloriseri<br>niq-ot-niq bi<br>mi qu-riptel | 0.5                | 1.0 | driver, clos<br>which pro | address of receiver     | a memon<br>snemitter i<br>density. Th             | 1.0  | ns b  | on only<br>the second<br>the second |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance (CTCAT) visuamini CR3 muminim Vs A as

| Symbol          | Parameter                        | Тур | Units | Conditions             |
|-----------------|----------------------------------|-----|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance                | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 70  | pF    | V <sub>CC</sub> = 5.0V |

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|---|--|---|
|   |  |   |
|   |  |   |
|   |  |   |
|   |  |   |
|   |  |   |
| (Pins 12, 14, 16, 18) L H Z                           |  |   |
| (Pins 12, 14, 16, 18) L H Z Outputs                   |  |   |
| (Pins 12, 14, 16, 18) L H Z                           |  |   |
| (Pine 12, 14, 16, 18) L H Z H (Pine 3, 5, 7, 9)       |  |   |
| (Pins 12, 14, 16, 18) L H Z Outputs (Pins 3, 5, 7, 9) |  |   |

5-11

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshL) or LOW to HIGH (toshL). Parameter guaranteed by design.



# 54ACQ/74ACQ241 • 54ACTQ/74ACTQ241 Quiet Series Octal Buffer/Line Driver with TRI-STATE® Outputs

# **General Description**

The 'ACQ/'ACTQ241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series<sup>TM</sup> features GTO<sup>TM</sup> output control and undershoot corrector in addition to a split ground bus for superior performance.

# **Features**

Guaranteed simultaneous switching noise level and dynamic threshold performance

AC Electrical Characteristics: See Section 2 for Waveforms

- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT241
- 4 kV minimum ESD immunity ('ACTQ)

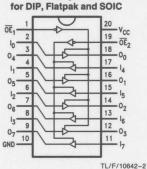
**Connection Diagrams** 

Ordering Code: See Section 8

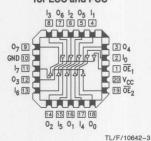
# **Logic Symbol**

# 

# Pin Assignment



# Pin Assignment for LCC and PCC



Symbol

# **Truth Tables**

| Pin Names                             | Description                    |
|---------------------------------------|--------------------------------|
| $\overline{OE}_1$ , $\overline{OE}_2$ | TRI-STATE Output Enable Inputs |
| 10-17                                 | Inputs                         |
| 00-07                                 | Outputs                        |

TL/F/10642-1

| Inpu            | Inputs | Outputs               |
|-----------------|--------|-----------------------|
| OE <sub>1</sub> | In     | (Pins 12, 14, 16, 18) |
| L               | L      | L                     |
| L               | Н      | Н                     |
| Н               | X      | Z                     |

| Inpu            | its | Outputs           |
|-----------------|-----|-------------------|
| OE <sub>2</sub> | In  | (Pins 3, 5, 7, 9) |
| L               | L   | L                 |
| L               | Н   | Н                 |
| Н               | X   | Z                 |

H = HIGH Voltage Level

L = LOW Voltage Level

X = ImmaterialZ = High Impedance

# If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. -0.5V to +7.0V

Supply Voltage (V<sub>CC</sub>) DC Input Diode Current (I<sub>IK</sub>) -20 mA  $V_1 = -0.5V$  $V_1 = V_{CC} + 0.5V$ +20 mA DC Input Voltage (VI) -0.5V to  $V_{CC} + 0.5V$ 

DC Output Diode Current (IOK)  $V_0 = -0.5V$ -20 mA  $V_0 = V_{CC} + 0.5V$ +20 mA DC Output Voltage (Vo) -0.5V to V<sub>CC</sub> + 0.5V

or Sink Current (IO) ±50 mA DC V<sub>CC</sub> or Ground Current per Output Pin (ICC or IGND) ±50 mA Storage Temperature (TSTG) -65°C to +150°C

DC Latch-Up Source or Sink Current

DC Output Source

Junction Temperature (T<sub>J</sub>) CDIP PDIP

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

# Absolute Maximum Rating (Note 1) Recommended Operating 100 13 00 Conditions

Supply Voltage (V<sub>CC</sub>) 'ACQ 2.0V to 6.0V 'ACTQ 4.5V to 5.5V Input Voltage (V<sub>I</sub>) owner ov to V<sub>CC</sub> Output Voltage (Vo)

Operating Temperature (TA) 74ACQ/ACTQ 54ACQ/ACTQ

-40°C to +85°C -55°C to +125°C Minimum Input Edge Rate ΔV/Δt

'ACQ Devices V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> Vcc @ 3.0V, 4.5V, 5.5V

Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices

VIN from 0.8V to 2.0V VCC @ 4.5V, 5.5V

125 mV/ns

OV to Vcc

125 mV/ns

# DC Electrical Characteristics for 'ACQ Family Devices

±300 mA

175°C

140°C

| 1.6GINTER                         | Concess of to Military sources.             |                   | 744                     | CQ                   | an American                      | 54ACC                | )                               | St. Aurent Jr. | 74ACQ                |       | The state of the s |   |  |
|-----------------------------------|---|-------------------|-------------------------|----------------------|----------------------------------|----------------------|---------------------------------|----------------|----------------------|-------|--|---|--|
| Symbol                            | Parameter  Minimum High Level Input Voltage | V <sub>CC</sub>   | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to +125°C |                      | T <sub>A</sub> = -40°C to +85°C |                | 5°C                  | Units | Conditions   |   |  |
|                                   |   | OTOA              | Тур                     | Ø                    | BAROT                            | Guara                | nteed L                         | imits          |                      |       |  |   |  |
| V <sub>IH</sub>                   |   | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | TA -                             | 2.1<br>3.15<br>3.85  | 0.62+                           | = AT           | 2.1<br>3.15<br>3.85  |       | no <b>V</b> mis  | V <sub>OUT</sub> =                          | 0.1V<br>- 0.1V   |
| V <sub>IL</sub><br>V1.0<br>V1.0 - | Maximum Low Level Input Voltage             | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 2.0                              | 0.9<br>1.35<br>1.65  | 2.0                             | 1,5<br>1,5     | 0.9<br>1.35<br>1.65  | lav   | J (V)H r   | V <sub>OUT</sub> = or V <sub>CC</sub>       | 0.1V<br>- 0.1V   |
| V <sub>OHVI</sub> ,o<br>VI.0 -    | Minimum High Level<br>Output Voltage        | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 8.0                              | 2.9<br>4.4<br>5.4    | 6.0<br>8.0                      | 1.5            | 2.9<br>4.4<br>5.4    | lev   | n Low Le   | oV tugat                                    | -50 μΑ   |
| VIL OF VIH                        | = ruol V                                    | 3.0<br>4.5<br>5.5 |                         | 2.56<br>3.86<br>4.86 | 5.4<br>5.4                       | 2.4<br>3.7<br>4.7    | 5.4                             | 6.49<br>6.49   | 2.46<br>3.76<br>4.76 | 19V   | V  | *V <sub>IN</sub> =                          | V <sub>IL</sub> or V <sub>IH</sub><br>-12 mA<br>-24 mA<br>-24 mA |
| V <sub>OL</sub> AS -              | Maximum Low Level<br>Output Voltage         | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 4.70                             | 0.1<br>0.1<br>0.1    | 4,88                            | 100.0          | 0.1<br>0.1<br>0.1    | lav   | n Love Le  | I <sub>OUT</sub> =                          | 50 μΑ  |
| PIL OF VIH<br>24 mA<br>24 mA      | 101 A<br>= WA.                              | 3.0<br>4.5<br>5.5 |                         | 0.36<br>0.36<br>0.36 | 08.0                             | 0.50<br>0.50<br>0.50 | 80.0                            | 100.0          | 0.44<br>0.44<br>0.44 |       | ٧  | *V <sub>IN</sub> =                          | V <sub>IL</sub> or V <sub>IH</sub><br>12 mA<br>24 mA<br>24 mA    |
| INDIAD O                          | Maximum Input<br>Leakage Current            | 5.5               |                         | ±0.1                 | 0.1±                             | ±1.0                 | t.0±                            |                | ±1.0                 |       | μА   | V <sub>1</sub> = V <sub>0</sub><br>(Note 1) | CC, GND  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Electrical Characteristics for 'ACQ Family Devices (Continued)

|                  |   |                        | 74ACQ<br>T <sub>A</sub> = +25°C |           | 54ACQ                             | 74ACQ                   | ga eogi<br>da edi | Conditions   |  |
|------------------|---|------------------------|---------------------------------|-----------|-----------------------------------|-------------------------|-------------------|--|--|
| Symbol           | V0.9 Parameter                                  | V <sub>CC</sub><br>(V) |                                 |           | T <sub>A</sub> = -55°C to + 125°C |                         | Units             |  |  |
| to Voc           |   |                        | Тур                             | stloV haq | Guaranteed Li                     | mits                    | al) Iner          | DC Input Blode Cur   |  |
| IOLD V OF        | †Minimum Dynamic                                | 5.5                    | oV) egg                         | HoV tugha | 50                                | 75                      | mA                | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD             | Output Current                                  | 5.5                    | empera<br>verve                 | pereting  | -50 + 50V                         | of V8.0 -75             | mA (              | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc              | Maximum Quiescent<br>Supply Current             | 5.5                    | KCTQ<br>iput Edg                | 8.0       | 160.0                             | 80.0                    | μА                | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)                           |  |
| loz<br>an\Vm     | Maximum TRI-STATE<br>Leakage Current            | 5.5                    | vices<br>30% to<br>0V, 4.5V     | ±0.5      | ±10.0                             | of V8 0 ± 5.0           | μΑ                | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1,1                             | 1.5       | Am 08 ±                           | (a                      | inevio            | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6                            | -1.2      | 210 + 180°D                       | )°80 — (6°°)            | V a               | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage     | 5.0                    | 3.1                             | 3.5       | 1.500 HeV                         |                         | (LTV or           | (Notes 2, 4)   |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.9                             | 1.5       | 140°C<br>Wilch demage             | anayod acusav exorb era | V                 | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C. Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n – 1 Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

# DC Electrical Characteristics for 'ACTQ Family Devices

|                         |                                      | V <sub>CC</sub> (V) | 744              | СТО          | Guerre               | 54ACT            | Q            | QVT7         | 4ACTQ                       |           |   |  |
|-------------------------|--------------------------------------|---------------------|------------------|--------------|----------------------|------------------|--------------|--------------|-----------------------------|-----------|---|--|
| Symbol                  | Parameter                            |                     | T <sub>A</sub> = | + 25°C       | -58                  | T <sub>A</sub> = | 125°C        | -40°         | T <sub>A</sub> = C to +85°C | Units     | Conditions  |  |
| VEO                     |                                      | 0.0                 | Тур              |              | 60                   | Guara            | nteed L      | imits        | 0.8 164                     | n favo Lo | Maying Maying   |  |
| V <sub>IH</sub> Vt.0 -  | Minimum High Level<br>Input Voltage  | 4.5<br>5.5          | 1.5<br>1.5       | 2.0          | 1.35                 | 2.0              | 1.85         | 2.25<br>2.75 | 2.0                         | V         | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| VIL 08-                 | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5          | 1.5<br>1.5       | 0.8          | 2.8                  | 0.8              | 2.9<br>4.4   | 2.99         | 0.8                         | V No      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>         | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49     | 4.4<br>5.4   | 2.4                  | 4.4<br>5.4       | 88.9         |              | 4.4<br>5.4                  | V         | $I_{OUT} = -50 \mu\text{A}$   |  |
| -24 mA<br>-24 mA        | HO! V                                | 4.5                 |                  | 3.86         | 3.7<br>4.7           | 3.70             | 3,86<br>4,86 |              | 3.76                        | V         | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OH} = -24 \text{ mA}$                          |  |
| Auj Od                  | = TUO!                               | 5.5                 |                  | 4.86         | 1,0                  | 4.70             | 1.0          | 2000         | 4.76                        | n Low Le  | -24 mA  |  |
| V <sub>OL</sub>         | Maximum Low Level Output Voltage     | 4.5<br>5.5          | 0.001<br>0.001   | 0.1<br>0.1   | 0.1                  | 0.1<br>0.1       | 1,0          | 100.0        | 0.1                         | V         | $I_{OUT} = 50 \mu A$  |  |
| 12 mA<br>24 mA<br>24 mA | Jol V                                | 4.5<br>5.5          |                  | 0.36<br>0.36 | 0.50<br>0.50<br>0.50 | 0.50<br>0.50     |              |              | 0.44<br>0.44                | V         | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>I <sub>OL</sub> 24 mA<br>24 mA |  |
| INGNE O                 | Maximum Input<br>Leakage Current     | 5.5                 |                  | ±0.1         | 0.1±                 | ±1.0             | F.0±         |              | ±1.0                        | μА        | $V_I = V_{CC}$ , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| r | Ξ | = |   |  |
|---|---|---|---|--|
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| r | ч | , | 1 |  |

|                  | C1 = 50 pF                                      |     | an c       |      |  | 70 0 10 1 00 0               |       |  |
|------------------|---|-----|------------|------|--|------------------------------|-------|--|
|                  | 100 - 30  | 180 | Тур        | 6    | Guaranteed L   | imits                        |       |  |
| loz              | Maximum TRI-STATE Leakage Current               | 5.5 | 8.         | ±0.5 | ±10.0  | ±5.0 VE                      | μА    | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$        |
| ICCT             | Maximum I <sub>CC</sub> /Input                  | 5.5 | 0.6        |      | 1.6  | 1.5                          | mA    | $V_I = V_{CC} - 2.1V$                                |
| IOLD             | †Minimum Dynamic                                | 5.5 | a          | - 0  | 50   | 75                           | mA    | V <sub>OLD</sub> = 1.65V Max                         |
| I <sub>OHD</sub> | Output Current                                  | 5.5 |            |      | -50  | -75                          | mA    | V <sub>OHD</sub> = 3.85V Min                         |
| Icc              | Maximum Quiescent<br>Supply Current             | 5.5 |            | 8.0  | 160.0  | 80.0 tuque                   | μΑ    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0 | ee owl you | 1.5  | ween the actual propagation<br>HIGH to LDW (foseil) or f | the same direction, either   | V     | Figures 1, 2<br>(Notes 2, 3)                         |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0 | -0.6       | -1.2 |  |                              | ٧     | Figures 1, 2<br>(Notes 2, 3)                         |
| V <sub>IHD</sub> | Minimum High Level Dynamic Input Voltage        | 5.0 | 1.9        | 2.2  | 4.5  | rut Capacitance              | ini V | (Notes 2, 4)   |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0 | 1.2        | 0.8  | 70   | wer Dissipation<br>pacifance |       | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |                                     |                          | 74ACQ  T <sub>A</sub> = +25°C  C <sub>L</sub> = 50 pF |            |             | 54/   | ACQ | 74ACQ  |              |       |             |
|-------------------------------------|-------------------------------------|--------------------------|---|------------|-------------|---|-----|--|--------------|-------|-------------|
| Symbol                              | Parameter                           | V <sub>CC</sub> *<br>(V) |   |            |             | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |     | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 pF$ |              | Units | Fig.<br>No. |
|                                     |                                     |                          | Min   | Тур        | Max         | Min   | Max | Min  | Max          |       |             |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 3.3<br>5.0               | 2.0<br>1.5  | 6.5<br>4.5 | 9.0<br>6.0  |   |     | 2.0<br>1.5   | 9.5<br>6.5   | ns    | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                  | 3.3<br>5.0               | 2.5<br>1.5  | 8.0<br>5.5 | 13.0<br>8.5 |   |     | 2.5<br>1.5   | 13.5<br>9.0  | ns    | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                 | 3.3<br>5.0               | 1.0<br>1.0  | 8.5<br>5.5 | 14.5<br>9.5 |   |     | 1.0<br>1.0   | 15.0<br>10.0 | ns    | 2-5, 6      |
| tosun                               | Skew **Data to Output               | 5.0                      |   | 0.5        | 1.0         |   | 4   |  | 1.5<br>1.0   | ns    |             |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V. Voltage Range 3.3 is 3.3V  $\pm 0.3$ V.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case DIP package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. n - 1 Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHI) or LOW to HIGH (toSLH). Parameter guaranteed by design.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     | Parameter 3788                            | THACT             | 74ACTQ  T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF |     |      | 54ACTQ  T <sub>A</sub> = -55°C  to + 125°C  C <sub>L</sub> = 50 pF |      | 74ACTQ<br>T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.   |
|-------------------------------------|---|-------------------|---|-----|------|--|------|--|------|-------|--------|
| Symbol                              |   | V <sub>CC</sub> * |   |     |      |  |      |  |      |       |        |
|                                     |   | -                 | Min   | Тур | Max  | Min  | Max  | Min  | Max  |       |        |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay Data to Output          | 5.0               | 1.5   | 5.0 | 6.5  | 1.5  | 8.0  | 1.5  | 7.0  | ns    | 2-3, 4 |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                        | 5.0               | 1.5   | 6.5 | 9.0  | 1.5  | 10.5 | 1.5  | 9.5  | ns    | 2-5, 6 |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                       | 5.0               | 1.0   | 7.0 | 10.0 | 1.5  | 9.5  | 1.0  | 10.5 | ns    | 2-5, 6 |
| toshl,                              | Output to Output<br>Skew **Data to Output | 5.0               |   | 0.5 | 1.0  |  | 8.8  | acent  | 1.0  | ns    | GRO    |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$ 0.5V.

# Capacitance

| Symbol                | Parameter                     | Тур | Units | Conditions             |
|-----------------------|-------------------------------|-----|-------|------------------------|
| C <sub>IN</sub> seros | Input Capacitance             | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub>       | Power Dissipation Capacitance | 70  | pF    | V <sub>CC</sub> = 5.0V |

AC Electrical Characteristics, on sure structure

|  |  |  |  | $T_{\Lambda} = -58^{\circ}C$<br>to + 128°C<br>$C_{L} = 50 \text{ pF}$ |  | $T_{A}=+28^{\circ}\text{C}$ $C_{L}=50\text{pF}$ |  |     |  |  |
|--|--|--|--|---|--|---|--|-----|--|--|
|  |  |  |  |   |  |   |  |     |  |  |
|  |  |  |  |   |  |   |  |     |  |  |
|  |  |  |  |   |  |   |  | 2.5 |  |  |
|  |  |  |  |   |  |   |  |     |  |  |
|  |  |  |  |   |  |   |  |     |  |  |

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.



# 54ACQ/74ACQ244 • 54ACTQ/74ACTQ244 **Quiet Series Octal Buffer/Line Driver** with TRI-STATE® Outputs

# **General Description**

The 'ACQ/'ACTQ244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density. The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet SeriesTM features GTOTM output control and undershoot corrector in addition to a split ground bus for superior performance.

# **Features**

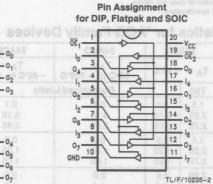
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT244
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

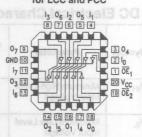
IEE/IEC

# **Logic Symbol**

# **Connection Diagrams**



Pin Assignment for LCC and PCC



TL/F/10235-3

TL/F/10235-1

**Truth Tables** 

| Pin Names                         | Description TRI-STATE Output Enable Inputs |  |  |  |
|-----------------------------------|--|--|--|--|
| OE <sub>1</sub> , OE <sub>2</sub> |  |  |  |  |
| 10-17                             | Inputs 1.0                                 |  |  |  |
| 00-07                             | Outputs                                    |  |  |  |

| Inpu            | ts 0.8  | Outputs               |
|-----------------|---------|-----------------------|
| ŌE <sub>1</sub> | In      | (Pins 12, 14, 16, 18) |
| 1.0L 500        | 0 (68 1 | Vol. Magimum Low Leve |
| 100 F00         | H       | Out ut Voltage        |
| Н               | X       | Z                     |

| Inpu            | its              | Outputs           |  |  |  |
|-----------------|------------------|-------------------|--|--|--|
| OE <sub>2</sub> | In               | (Pins 3, 5, 7, 9) |  |  |  |
| L               | 8.8 <sub>L</sub> | Lidakaga Curren   |  |  |  |
| L               | a.aH oim         | savo muminiHt     |  |  |  |
| Н               | X                | CS tout Current   |  |  |  |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

# Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )                    | -0.5V to +7.0V             |
|--|----------------------------|
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$ | -20 m4                     |
| $V_1 = V_{CC} + 0.5V$                                | -20 mA<br>+20 mA           |
| DC Input Voltage (V <sub>I</sub> )                   | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Diode Current (IOK)                        |                            |
| $V_0 = -0.5V$  | -20 mA                     |
| $V_O = V_{CC} + 0.5V$                                | + 20 mA                    |
| DC Output Voltage (V <sub>O</sub> )                  | $-0.5V$ to $V_{CC} + 0.5V$ |
| DC Output Source                                     | ± 50 mA                    |
| or Sink Current (I <sub>O</sub> )                    | ± 50 mA                    |
| DC V <sub>CC</sub> or Ground Current                 |                            |
| per Output Pin (ICC or IGND)                         | ±50 mA                     |
| Storage Temperature (T <sub>STG</sub> )              | -65°C to +150°C            |
| DC Latch-Up Source or                                |                            |
| Sink Current   | ±300 mA                    |
| Junction Temperature (T <sub>J</sub> )               |                            |
|  |                            |

PDIP Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

# **Recommended Operating** Conditions

| Supply Voltage (V <sub>CC</sub> )  |   |
|--|---|
| 'ACQ 'ACTQ   | 2.0V to 6.0V<br>4.5V to 5.5V              |
| Input Voltage (V <sub>I</sub> )  | 0V to V <sub>CC</sub>                     |
| Output Voltage (V <sub>O</sub> )   | 0V to V <sub>CC</sub>                     |
| Operating Temperature (T <sub>A</sub> )<br>74ACQ/ACTQ<br>54ACQ/ACTQ  | -40°C to +85°C<br>-55°C to +125°C         |
| Minimum Input Edge Rate ΔV/Δ· 'ACQ Devices V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> V <sub>CC</sub> @ 3.0V, 4.5V, 5.5V |   |
| Minimum Input Edge Rate ΔV/Δ   | vides improved PC 1<br>NSC Oulet Series 1 |
| V <sub>CC</sub> @ 4.5V, 5.5V   |   |

# DC Electrical Characteristics for 'ACQ Family Devices

175°C

140°C

|                 |                                      |                        | 744                     | CQ                   | 54ACQ  | 74ACQ                           | ď.         | Tours of   |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|--|---------------------------------|------------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = T <sub>A</sub> =<br>-55°C to + 125°C -40°C to +85°C |                                 | Units      | Conditions   |  |
|                 | 中 清洁流声 电电                            |                        | Тур                     | 21 1                 | Guaranteed L   | imits                           | Manager In | gl   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85             | ٧          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65             | V          | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4  | 2.9<br>4.4<br>5.4               | ٧          | $I_{OUT} = -50 \mu A$  |  |
|                 | Outputs<br>(Pins 12, 14, 16          | 3.0<br>4.5<br>5.5      | etuani                  | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7  | 2.46<br>3.76<br>4.76            | V          | $\begin{tabular}{ll} *V_{IN} &= V_{IL} \mbox{ or } V_{IH} \\ &= 12 \mbox{ mA} \\ I_{OH} &= -24 \mbox{ mA} \\ &= -24 \mbox{ mA} \\ \end{tabular}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1  | 0.1 stugnt<br>0.1 stugnt<br>0.1 | V          | Ι <sub>ΟυΤ</sub> = 50 μΑ   |  |
|                 | Outputs<br>(Pins 3, 5.1              | 3.0<br>4.5<br>5.5      | riugn)                  | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50   | 0.44<br>0.44<br>0.44            | ٧          | $V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $V_{IOL}$ 10 24 mA 24 mA  |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0   | ±1.0                            | μΑ         | V <sub>I</sub> = V <sub>CC</sub> , GND<br>(Note 1)   |  |
| IOLD            | †Minimum Dynamic                     | 5.5                    |                         | _                    | 50   | 75                              | mA         | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD            | Output Current                       | 5.5                    |                         | 11                   | -50  | -75                             | mA         | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc             | Maximum Quiescent<br>Supply Current  | 5.5                    | follage Level           | 8.0                  | 160.0  | 80.0                            | μА         | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)   |  |

\*All outputs loaded thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

# 5

# DC Electrical Characteristics for 'ACQ Family Devices (Continued)

|                    | LACTO   | 7   | 744                    | CQ     | 54ACQ                             | 74ACQ                           |                      |  |  |
|--------------------|---|-----|------------------------|--------|-----------------------------------|---------------------------------|----------------------|--|--|
| Symbol             | /mbol Parameter                                 |     | T <sub>A</sub> = +25°C |        | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                | Conditions   |  |
|                    | 0.484.017                                       | 00  | Тур                    | 1.30 = | Guaranteed L                      | imits                           |                      |  |  |
| loz<br>(4 ,\$ aeto | Maximum TRI-STATE<br>Leakage Current            | 5.5 | (ALL 1990)             | ±0.5   | ±10.0                             | ±5.0                            | μΑ                   | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |
| V <sub>OLP</sub>   | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0 | 1.1                    | 1.5    | 8.0 8                             | evel s.o 1                      | I wVI m              | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>OLV</sub>   | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0 | -0.6                   | -1.2   | Joet retire kiel                  | ingul associated with or        | V<br>selonee         | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>IHD</sub>   | Minimum High Level<br>Dynamic Input Voltage     | 5.0 | 3.1                    | 3.5    | .0%6                              | e identical to PACTO el         | n 2.0 ms,<br>O eVerc | (Notes 2, 4)   |  |
| V <sub>ILD</sub>   | Maximum Low Level<br>Dynamic Input Voltage      | 5.0 | 1.9                    | 1.5    | are driven 6V to 3V. One o        | efined as (n). Diga inputs      | V                    | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded thresholds on input associated with output under test.

# **DC Electrical Characteristics for 'ACTQ Family Devices**

|                  | ERM COM   | Esta                   | 74A                 | CTQ          | 54ACTQ                           | 74ACTQ                            |        |  |  |
|------------------|---|------------------------|---------------------|--------------|----------------------------------|-----------------------------------|--------|--|--|
| Symbol           | Parameter 2                                     | V <sub>CC</sub><br>(V) | T <sub>A</sub> =    | + 25°C       | T <sub>A</sub> = -55°C to +125°C |                                   |        | Conditions   |  |
| 220              | 2.5 12.5  |                        | Тур                 |              | Guaranteed L                     | imits 8.8 em                      | Teldan | tezt, tezh Output E  |  |
| VIH              | Minimum High Level<br>Input Voltage             | 4.5<br>5.5             | 1.5<br>1.5          | 2.0          | 2.0                              | 2.0                               | V      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage                 | 4.5<br>5.5             | 1.5<br>1.5          | 0.8          | 0.8                              | 0.8                               | V      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage            | 4.5<br>5.5             | 4.49<br>5.49        | 4.4<br>5.4   | 4.4<br>5.4                       | 5.4                               | of Vac | $I_{OUT} = -50 \mu\text{A}$  |  |
|                  | specification of the rame device. The specific  | 4.5<br>5.5             | the divid Attri     | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                      | V      | $  ^{*}V_{IN} = V_{IL} \text{ or } V_{IH} $ $  ^{I}_{OH}                                    $  |  |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage             | 4.5<br>5.5             | 0.001               | 0.1          | 0.1<br>0.1                       | 0.1<br>0.1                        | ٧      | I 50 A   |  |
|                  | 74ACTQ  | 4.5<br>5.5             | STACT               | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                      | ٧      | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub>  | Maximum Input<br>Leakage Current                | 5.5                    | 121 + 02<br>24 = 50 | ±0.1         | ±1.0                             | ±1.0                              | μА     | $V_I = V_{CC}$ , GND   |  |
| loz              | Maximum TRI-STATE<br>Leakage Current            | 5.5                    | ni                  | ±0.5         | ± 10.0                           | ±5.0                              | μΑ     | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |  |
| Ісст             | Maximum I <sub>CC</sub> /Input                  | 5.5                    | 0.6                 |              | 1.6                              | 1.5                               | mA     | $V_I = V_{CC} - 2.1V$  |  |
| IOLD             | †Minimum Dynamic                                | 5.5                    |                     |              | 50                               | 75                                | mA     | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD             | Output Current                                  | 5.5                    | U.                  |              | -50                              | -75                               | mA     | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc              | Maximum Quiescent<br>Supply Current             | 5.5                    | G.                  | 8.0          | 160.0                            | 80.0                              | μА     | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)   |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1.1                 | 1.5          | 0.6 1.0                          | 5.0                               | V      | Figures 1, 2 (Notes 2, 3)  |  |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6                | -1.2         | ween the estual propassion       | V.<br>stue of the difference both | V      | Figures 1, 2<br>(Notes 2, 3)   |  |

<sup>\*</sup>All outputs loaded thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.
I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching, (n - 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

| Зуппын           | rai ailletei                             | (V) | IA- | T 20 C                | -55°C to + 125°C   -40°C to +85°C |            | Units    | Conditions   |
|------------------|--|-----|-----|-----------------------|-----------------------------------|------------|----------|--------------|
|                  | (30)V                                    |     | Тур | Typ Guaranteed Limits |                                   |            | T mundiy | 11           |
| V <sub>IHD</sub> | Minimum High Level Dynamic Input Voltage | 5.0 | 1.9 | 2.2                   | ±0.5                              | a.a ther   | O epski  | (Notes 2, 4) |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage  | 5.0 | 1.2 | 0.8                   | 1.1 1.5                           | mamic Vol. | V        | (Notes 2, 4) |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |   |                   | .ovio e  | 74ACQ      |   | 54A     | CQ   | 74         | ACQ         | dmun xaM r  | 6 e1024 |
|-------------------------------------|---|-------------------|--|------------|---|---------|--|------------|-------------|-------------|---------|
| Symbol Parameter                    |   | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |         | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |            | Units       | Fig.<br>No. |         |
|                                     |   | Chart             | Min  | Тур        | Max   | Min     | Max  | Min        | Max         | 1           |         |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay Data to Output          | 3.3<br>5.0        | 2.0  | 7.0<br>5.0 | 9.0<br>6.0  | 82+ - A | V <sub>CC</sub> (V)  | 2.0        | 9.5<br>6.5  | ns          | 2-3, 4  |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                        | 3.3               | 2.5<br>1.5                                       | 8.0<br>6.5 | 12.0<br>8.0   | Typ   2 | 8.5  | 2.5<br>1.5 | 12.5        | ns          | 2-5, 6  |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                       | 3.3<br>5.0        | 1.0<br>1.0                                       | 9.0<br>7.5 | 13.5<br>9.0   | 1.6 2.  | 4,5  | 1.0        | 14.0<br>9.5 | ns          | 2-5, 6  |
| toshl,                              | Output to Output<br>Skew** Data to Output | 3.3<br>5.0        |  | 1.0<br>0.5 | 1.5<br>1.0  | D 0.F   | 6.8  | tave.      | 1.5<br>1.0  | ns          | но      |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     | TOI A                               | 0.44              |     | 74ACTQ                | 0   | 54A  | CTQ  | 74A      | CTQ                    |       |             |
|-------------------------------------|-------------------------------------|-------------------|-----|-----------------------|-----|--|------|----------|------------------------|-------|-------------|
| Symbol                              | V = Parameter                       | V <sub>CC</sub> * |     | C <sub>L</sub> = +25° |     | T <sub>A</sub> = -<br>to + 1<br>C <sub>L</sub> = | 25°C | to +     | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                                     | V = V An                            | 0.81              | Min | Тур                   | Max | Min  | Max  | Min      | Max                    | GSMI  | loz         |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>Data to Output | 5.0               | 1.5 | 5.5                   | 6.5 | 1.5 0.0  | 9.0  | 1.5      | 7.0                    | ns    | 2-7         |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                  | 5.0               | 1.5 | 7.0                   | 8.5 | 1.5  | 10.5 | 1.5      | 9.0                    | ns    | 2-7         |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                 | 5.0               | 1.0 | 8.0                   | 9.5 | 1.5  | 10.5 | 1.0      | 10.0                   | ns    | 2-3         |
| toshl,                              | Output to Output                    | 0,00              |     | U.130 F               |     | 3 1  | 61.0 |          | oly Gurrent            | dn5   |             |
| toslh (8.)                          | Skew **<br>Data to Output           | 5.0               |     | 0.5                   | 1.0 | a ta   |      | amic VoL | 1.0                    | ns    | PLOV        |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Voltage Range 3.3 is 3.3V ±0.3V.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

# Capacitance

| Symbol          | Parameter         | Тур | Units | Conditions      |
|-----------------|-------------------|-----|-------|-----------------|
| C <sub>IN</sub> | Input Capacitance | 4.5 | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation | 70  | pF    | $V_{CC} = 5.0V$ |

# Semicon

- - - Minummi au-riotel beverent &
- # TRI-STATE outputs drive bus lines or butter memory

  - B Faster prop delays than the standard 'ACT245











# 54ACQ/74ACQ245 • 54ACTQ/74ACTQ245 Quiet Series Octal Bidirectional Transceiver with TRI-STATE® Inputs/Outputs

# **General Description**

The 'ACQ/'ACTQ245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condition.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

# **Features**

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT245
- 4 kV minimum ESD immunity ('ACQ)

# Ordering Code: See Section 8

# **Logic Symbols**

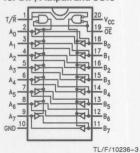


| Pin<br>Names                   | Description  |
|--------------------------------|--|
| ŌĒ                             | Output Enable Input                                |
| T/R                            | Transmit/Receive Input                             |
| A <sub>0</sub> -A <sub>7</sub> | Side A TRI-STATE Inputs or TRI-STATE Outputs       |
| B <sub>0</sub> -B <sub>7</sub> | Side B TRI-STATE<br>Inputs or TRI-STATE<br>Outputs |

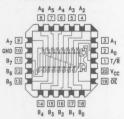
# | IEEE/IEC | G3 | T/R | 3 EN1 (BA) | 3 EN2 (AB) | B0 | D 2 \(\nabla \) | B1 | B2 | B3 | B4 | B4 | B5 | B6 | B7 | TL/F/10236-2

# **Connection Diagrams**

Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC



TL/F/10236-4

# **Truth Table**

| Inp | outs | Outputs             |  |  |  |  |  |
|-----|------|---------------------|--|--|--|--|--|
| OE  | T/R  | Outputs             |  |  |  |  |  |
| L   | L    | Bus B Data to Bus A |  |  |  |  |  |
| L   | Н    | Bus A Data to Bus B |  |  |  |  |  |
| Н   | X    | HIGH-Z State        |  |  |  |  |  |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

# Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales

| Office/Distributors for availab   | ility and specification         | S. T |
|---|---------------------------------|------|
| Supply Voltage (V <sub>CC</sub> )   | -0.5V to +7                     | .0V  |
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$<br>$V_I = V_{CC} + 0.5V$                 | -20<br>+20                      | mA   |
| DC Input Voltage (V <sub>I</sub> )  | $-0.5$ V to $V_{CC} + 0$        | .5V  |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$                | 0.09 -20<br>+20                 |      |
| DC Output Voltage (V <sub>O</sub> ) DC Output Source or Sink Current (I <sub>O</sub> )        | -0.5V to to V <sub>CC</sub> + 0 |      |
| DC V <sub>CC</sub> or Ground Current<br>per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50                             |      |
| Storage Temperature (T <sub>STG</sub> )   | -65°C to +15                    | 0°C  |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

DC Latch-Up Source or Sink Current

CDIP

PDIP

Junction Temperature (T,I)

# Conditions

| Supply Voltage (V <sub>CC</sub> ) 'ACQ 'ACTQ                        | 2.0V to 6.0V<br>4.5V to 5.5V |
|---|------------------------------|
| Input Voltage (V <sub>I</sub> )                                     | 0V to V <sub>CC</sub>        |
| Output Voltage (V <sub>O</sub> )                                    | OV to V <sub>CC</sub>        |
| Operating Temperature (T <sub>A</sub> )<br>74ACQ/ACTQ<br>54ACQ/ACTQ | -40°C to +85°C               |

Minimum Input Edge Rate ΔV/Δt 'ACQ Devices

V<sub>IN</sub> from 30% to 70% of V<sub>CC</sub> 125 mV/ ns

Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V<sub>IN</sub> from 0.8V to 2.0V

125 mV/ns V<sub>CC</sub> @ 4.5V, 5.5V

DC Characteristics for 'ACQ Family Devices

| Jane (Vieta).  | dends of VO <sub>AOA</sub> V) blodesh | lof Vë spriris         | 74A                     | CQ                   | 54ACQ                             | grd (t -   | 74ACQ                           | Data Ingela       | Note 4: Max number of  |
|--|---------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|------------|---------------------------------|-------------------|--|
| Symbol   | Parameter                             | V <sub>CC</sub><br>(V) | <b>T</b> A = -          | + 25°C               | T <sub>A</sub> = -55°C to + 125°C | -40        | T <sub>A</sub> =<br>°C to +85°C | Units             | Conditions   |
|  |                                       | 000000                 | Тур                     | 25/19/25 1           | Guaranteed L                      | imits.     |                                 |                   |  |
| V <sub>IH</sub><br>anoth                               | Minimum High Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | AT         | 2.1<br>3.15<br>3.85             | V                 | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                                   |
| VIL<br>V1.0  | Maximum Low Level<br>Input Voltage    | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | yT<br>Lt   | 0.9<br>1.35<br>1.65             | V <sub>1</sub>    | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                                   |
| 0.1\/hOV   | Minimum High Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 1.†<br>1.† | 2.9<br>4.4<br>5.4               | ed wo i m         | $I_{OUT} = -50 \mu\text{A}$  |
| Ац Оё-   | = Tuol   . V                          | 3.0                    |                         | 2.56                 | 2.4                               | 5.4        | 2.46                            | egatio\<br>ottage | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>-12 mA                        |
| VIL or VIH<br>- 24 mA                                  | =  4 V*                               | 4.5<br>5.5             |                         | 3.86<br>4.86         | 3.7<br>4.7                        |            | 3.76<br>4.76                    | ٧                 | I <sub>OH</sub> -24 mA<br>-24 mA   |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage   | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 00.0       | 0.1<br>0.1<br>0.1               | s LwV.I a         | I <sub>OUT</sub> = 50 μA   |
| V <sub>II,</sub> or V <sub>IIH</sub><br>24 mA<br>24 mA | of V                                  | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              |            | 0.44<br>0.44<br>0.44            | v                 | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}O_L$ $^{24} \text{ mA}$ |
| IN OND O   | Maximum Input<br>Leakage Current      | 5.5                    |                         | ±0.1                 | ±1.0 ±                            |            | ±1.0                            | μΑ                | V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)  |

±300 mA

175°C

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'ACQ Family Devices (Continued) In A mumber of State of Acquired and Acquired and Acquired acquir

|                  |   |     | 74                               | ACQ               | 54ACQ                            | 74ACQ                           | pace spaint        | if Military/Aeros  |  |
|------------------|---|-----|----------------------------------|-------------------|----------------------------------|---------------------------------|--------------------|--|--|
| Symbol           | Symbol Parameter                                |     | T <sub>A</sub> =                 | + 25°C            | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units              | Conditions   |  |
|                  | 70  |     | Тур                              | atloV Jugi        | Guaranteed Li                    | mits                            | nent (lg           | DC Input Diode Or  |  |
| IOLD             | †Minimum Dynamic                                | 5.5 | oV) egst                         | lutput Vol        | 50                               | 75                              | mA                 | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub> | Output Current                                  | 5.5 | neome t<br>ACTO                  | paraung<br>zuscen | -50 + 00V                        | of √8.0 −75                     | mA                 | V <sub>OHD</sub> = 3.85V Min   |  |
| lcc              | Maximum Quiescent<br>Supply Current             | 5.5 | ACTO<br>iput Edg                 | 8.0               | 160.0                            | 80.0                            | μА                 | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)                           |  |
| lozt<br>an \Vm   | Maximum I/O<br>Leakage Current                  | 5.5 | 3090 to<br>3090 to<br>4.57, 4.57 | ±0.6              | V8.0 + 55V<br>±11.0              | ±6.0                            | μA                 | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0 | 800 VB(                          | 1.5               | Am 08±                           | (a)                             | Company<br>Company | Figures 1, 2 (Notes 2, 3)  |  |
| Volv             | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0 | -0.6                             | -1.2              | O*087 + of 0                     | 198-                            | TST) ST            | Figures 1, 2<br>(Notes 2,3)  |  |
| V <sub>IHD</sub> | Maximum High Level<br>Dynamic Input Voltage     | 5.0 | 3.1                              | 3.5               | 175'C                            |                                 | (Tyen)             | (Notes 2, 4)   |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0 | 1.9                              | 1.5               | O°047<br>Which deniego           | i me thicse values beyon        | ٧                  | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C. DC Characteristics for 'ACQ Family Devices Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>),

# **DC Characteristics for 'ACTQ Family Devices**

| 2/2.0  |                                      |            | 74A            | CTQ          | 54ACTQ                           | 74ACTQ                          | i andre |   |  |
|--|--------------------------------------|------------|----------------|--------------|----------------------------------|---------------------------------|---------|---|--|
| Symbol   | Parameter                            | Vcc<br>(V) | VCC TA = +25°C |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units   | Conditions  |  |
| VI.0   | = TUOV.                              | 6.0        | Тур            | 8,0          | Guaranteed L                     | imits a.e lev                   | JwoJn   | V <sub>II</sub> Maximus   |  |
| V <sub>IH</sub> 1.0                                    | Minimum High Level<br>Input Voltage  | 4.5<br>5.5 | 1.5<br>1.5     | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧       | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| VIL  | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5 | 1.5<br>1.5     | 0.8          | 0.8                              | 0.8<br>0.8                      | V       | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| Vон  | Minimum High Level<br>Output Voltage | 4.5<br>5.5 | 4.49<br>5.49   | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V       | $I_{OUT} = -50 \mu\text{A}$   |  |
|  | HO! V                                | 4.5        |                | 3.86         | 3.70                             | 3.76                            | V       | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>-24 mA   |  |
| Au 08  | # mol                                | 5.5        |                | 4.86         | 4.70                             | 4.76                            | 1 wo to | -24 mA  |  |
| V <sub>OL</sub>  | Maximum Low Level Output Voltage     | 4.5<br>5.5 | 0.001<br>0.001 | 0.1<br>0.1   | 0.1                              | 0.0 0.1<br>0.0 0.1              | V       | I <sub>OUT</sub> = 50 μA  |  |
| V <sub>III</sub> or V <sub>III</sub><br>Am 21<br>Am 4S | aol V                                | 4.5<br>5.5 |                | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44<br>0.44                    | v       | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| IN ON O  | Maximum Input<br>Leakage Current     | 5.5        |                | ±0.1         | ± 1.0                            | ±1.0                            | μА      | V <sub>I</sub> = V <sub>CC</sub> , GND  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'ACTQ Family Devices (Continued)

|                  | TEACTQ  | 1 8                    | 74A0               | CTQ    | 54ACTQ                            | 74ACTQ                          |       |  |
|------------------|---|------------------------|--------------------|--------|-----------------------------------|---------------------------------|-------|--|
| Symbol           | Parameter                                       | V <sub>CC</sub><br>(V) | T <sub>A</sub> = - | + 25°C | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |
|                  | CL = 50 pF                                      | 30                     | Тур                |        | Guaranteed L                      | imits                           |       |  |
| loz              | Maximum TRI-STATE<br>Leakage Current            | 5.5                    | 8,                 | ±0.5   | ±10.0                             | ±5.0                            | μА    | $V_1 = V_{1L}, V_{1H}$<br>$V_0 = V_{CC}, GND$        |
| ICCT             | Maximum<br>I <sub>CC</sub> /Input               | 5.5                    | 0.6                |        | 1.6                               | 2 1.5 emi                       | mA    | $V_I = V_{CC} - 2.1V$                                |
| IOLD             | †Minimum Dynamic                                | 5.5                    | 0.                 |        | 50                                | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max                         |
| IOHD             | Output Current                                  | 5.5                    |                    |        | -50                               | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min                         |
| Icc              | Maximum Quiescent<br>Supply Current             | 5.5                    |                    | 8.0    | 160.0                             | 80.0                            | μА    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | e = 1.1 = 1        | 1.5    | Ween the actual propagate         | velue of the difference be      | ٧     | Figures 1, 2<br>(Notes 2, 3)                         |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6               | -1.2   |                                   |                                 | V     | Figures 1, 2<br>(Notes 2, 3)                         |
| V <sub>IHD</sub> | Maximum High Level<br>Dynamic Input Voltage     | 5.0                    | 1.9                | 2.2    | atinU q                           | (T refer                        | V     | (Notes 2, 4)   |
| V <sub>ILD</sub> | Maximum Low Level<br>Dynamic Input Voltage      | 5.0                    | 1.2                | 0.8    | 30                                | t tight                         | o Van | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |  |                   |            | 74ACQ                 |             | 54/  | ACQ                     | 744        | CQ                     |       |             |
|-------------------------------------|--|-------------------|------------|-----------------------|-------------|------|-------------------------|------------|------------------------|-------|-------------|
| Symbol                              | Parameter                                    | V <sub>CC</sub> * |            | A = +25°<br>CL = 50 p |             | to + | -55°C<br>125°C<br>50 pF | to +       | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                                     |  | (V)               | Min        | Тур                   | Max         | Min  | Max                     | Min        | Max                    |       |             |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>Data to Output          | 3.3<br>5.0        | 2.0<br>1.5 | 7.5<br>5.0            | 10.0<br>6.5 |      |                         | 2.0<br>1.5 | 10.5<br>7.0            | ns    | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                           | 3.3<br>5.0        | 3.0<br>2.0 | 8.5<br>6.0            | 13.0<br>8.5 |      |                         | 3.0<br>2.0 | 13.5<br>9.0            | ns    | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                          | 3.3<br>5.0        | 1.0        | 8.5<br>7.5            | 14.5<br>9.5 |      |                         | 1.0<br>1.0 | 15.0<br>10.0           | ns    | 2-5, 6      |
| toshl,<br>toshh                     | Output to Output<br>Skew**<br>Data to Output | 3.3<br>5.0        |            | 1.0<br>0.5            | 1.5<br>1.0  |      |                         |            | 1.5<br>1.0             | ns    |             |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V Voltage Range 3.3 is 3.3V ±0.3V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: ICC for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). n-1 Data Inputs are driven 0V to 3V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold  $(V_{ILD})$ , 0V to threshold  $(V_{IHD})$  f=1 MHz.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |  | PARCTO            |  | 74ACTQ |  | 54A | СТО  | 74A  | CTQ   |             |           |
|-------------------------------------|--|-------------------|--|--------|--|-----|--|------|-------|-------------|-----------|
| Symbol                              | Parameter                                    | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |        | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units | Fig.<br>No. |           |
|                                     | N = N  |                   | Min  | Тур    | Max  | Min | Max  | Min  | Max   | Nive Ad     |           |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>Data to Output          | 5.0               | 1.5  | 5.5    | 7.0  | 1.5 | 9.0  | 1.5  | 7.5   | ns          | 2-3, 4    |
| tpzL, tpzH                          | Output Enable Time                           | 5.0               | 2.0  | 7.0    | 9.0  | 1.5 | 12.0   | 2.0  | 9.5   | ns          | 2-5, 6    |
| tpHZ, tpLZ                          | Output Disable Time                          | 5.0               | 1.0  | 8.0    | 10.0   | 1.0 | 11.5   | 1.0  | 10.5  | ns          | 2-5, 6    |
| toshl,<br>toshh                     | Output to Output<br>Skew**<br>Data to Output | 5.0               |  | 0.5    | 1.0  | 8   | 5.5<br>5.6   | fneo | 1.0   | ns          | OHO<br>OO |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol           | Parameter                        | Тур  | Units | Conditions             |
|------------------|----------------------------------|------|-------|------------------------|
| CIN              | Input Capacitance                | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>I/O</sub> | Input/Output<br>Capacitance      | 15   | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub>  | Power Dissipation<br>Capacitance | 80.0 | pF    | V <sub>CC</sub> = 5.0V |

AC Flectrical Characteristics: see sections to Wavetone

Note to May number of outputs defined as (n), n-1 Data Inputs are driven OV to SV; one output @ GMD.

Mohe 1: log for SAACTO & 28°C is identical to 74AC

|        | 90  |  |  |  |  |     |     |             |                    |  |
|--------|---|--|--|--|--|-----|-----|-------------|--------------------|--|
|        | $T_A = -80^{\circ}C$<br>to +86°C<br>$C_L = 50 \text{ pF}$ |  |  |  | T <sub>A</sub> = +26'0<br>C <sub>L</sub> = 50 pF |     |     | "50¥<br>(¥) | Parameter          |  |
|        |   |  |  |  |  | qyT |     |             |                    |  |
| 2-5, 4 |   |  |  |  |  |     | 2.0 |             |                    |  |
|        | 13.5  |  |  |  |  |     |     |             | Output Enable Time |  |
|        |   |  |  |  |  |     |     | 3,8         |                    |  |
|        |   |  |  |  |  |     |     |             |                    |  |

Stary is defined as the obsolute value of the difference between the actual propagation datay for any two separate outputs of the same device. The specification of any other two experiences for the specification of the same devices, when the same devices after the same and the same devices.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHI) or LOW to HIGH (toSLH). Parameter guaranteed by design.

# **General Description**

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The 'AC/'ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ( $\overline{\rm MR}$ ) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{\text{MR}}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic

threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

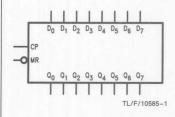
# **Features**

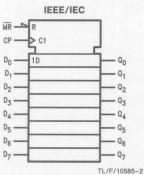
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered common clock and asynchronous master reset
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT273
- 4 kV minimum ESD immunity

The information for the ACQ273 is Advanced Information only.

Ordering Code: See Section 8

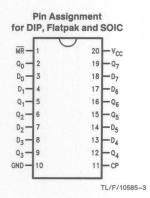
# **Logic Symbols**

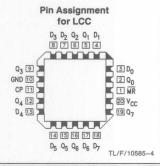




| Pin Names                      | Description      |
|--------------------------------|------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs      |
| MR                             | Master Reset     |
| CP                             | Clock Pulse Inpu |
| $Q_0 - Q_7$                    | Data Outputs     |

# **Connection Diagrams**





5

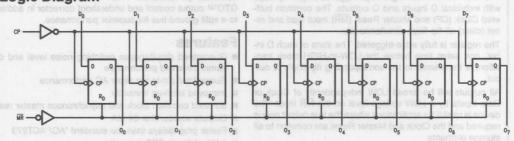
|               | IVIH | CP | Dn     | Qn    |
|---------------|------|----|--------|-------|
| Reset (Clear) | 272  | X  | X      | DAIL2 |
| Load '1'      | Н    | _  | H      | Н     |
| Load '0'      | Н    | _  | Felori | L     |

H = HIGH Voltage Level
L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Transition

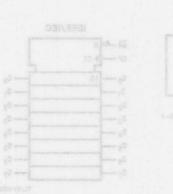




TL/F/10585-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.







| 00-07 |
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|       |
|       |
|       |

# Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales

| Office/Distributors for availab  |            |                           |
|--|------------|---------------------------|
| Supply Voltage (V <sub>CC</sub> )  | 40'0 10 +8 | 0.5V to +7.0V             |
| DC Input Diode Current (I <sub>IK</sub> )                                      | at l       |                           |
| $V_{I} = -0.5V$<br>$V_{I} = V_{CC} + 0.5V$                                     |            | -20 mA<br>+20 mA          |
| DC Input Voltage (V <sub>I</sub> )   | -0.5V t    | to V <sub>CC</sub> + 0.5V |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$ |            | -20 mA<br>+20 mA          |
| DC Output Voltage (V <sub>O</sub> )  | -0.5V      | to V <sub>CC</sub> + 0.5V |
| DC Output Source<br>or Sink Current (I <sub>O</sub> )                          |            | ±50 mA                    |
| DC V <sub>CC</sub> or Ground Current   |            |                           |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )                          |            | ±50 mA                    |
| Storage Temperature (T <sub>STG</sub> )  | -65        | 5°C to +150°C             |
| DC Latch-up Source or<br>Sink Current  |            | ±300 mA                   |
| Junction Temperature (T <sub>1</sub> )   |            |                           |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT circuits outside databook specifications.

CDIP PDIP

# Conditions

| Supply Voltage (V <sub>CC</sub> ) 'ACQ 'ACTQ  | 2.0V to 6.0V<br>4.5V to 5.5V                   |
|---|--|
| Input Voltage (V <sub>I</sub> )   | 0V to V <sub>CC</sub>                          |
| Output Voltage (V <sub>O</sub> )  | oimenyO muminiM 0V to V <sub>CC</sub>          |
| Operating Temperature (T<br>74ACQ/ACTQ<br>54ACQ/ACTQ                                    | -40°C to +85°C<br>-55°C to +125°C              |
| Minimum Input Edge Rate   | ΔV/Δt memuO (regula)                           |
| 'ACQ Devices<br>V <sub>IN</sub> from 30% to 70% o<br>V <sub>CC</sub> @ 3.0V, 4.5V, 5.5V | of Vcc hand munic 125 mV/ns                    |
| Minimum Input Edge Rate 'ACTQ Devices   | Vol.ν Guiet Output τΔ\VΔ  Minimum Dynamic Vol. |
| V <sub>IN</sub> from 0.8V to 2.0V<br>V <sub>CC</sub> @ 4.5V, 5.5V                       | leve I dpiH mumb(s) 125 mV/ns                  |
|   |  |

# **DC Characteristics for 'ACTQ Family Devices**

|                 | OTOAN                                |                        | 74A              | СТО                   | 54ACTQ                           | 74ACTQ                          |                  |  |  |
|-----------------|--------------------------------------|------------------------|------------------|-----------------------|----------------------------------|---------------------------------|------------------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C                | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units            | Conditions   |  |
|                 | Rq 08 = 10                           | 760                    | Тур              | Typ Guaranteed Limits |                                  |                                 |                  | Symbol   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0                   | 2.0                              | 2.0<br>2.0                      | V                | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$                                       |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8                   | 0.8<br>0.8                       | 0.8                             | BCVV             | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V                         |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4            | 4.4<br>5.4                       | 4.4<br>5.4                      | Output<br>V      | $I_{OUT} = -50 \mu\text{A}$  |  |
|                 | n 0.1 na                             | 4.5<br>5.5             |                  | 3.86<br>4.86          | 3.7<br>4.7                       | 3.76<br>4.76                    | Output<br>Output | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> I <sub>OH</sub> -24 mA |  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001   | 0.1<br>0.1            | 0.1<br>0.1                       | 0.1<br>0.1                      | od Vola s        | $I_{OUT} = 50 \mu A$   |  |
|                 |                                      | 4.5<br>5.5             |                  | 0.36<br>0.36          | 0.50<br>0.50                     | 0.44<br>0.44                    | V                | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = -24 \text{ mA}$              |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1                  | ±1.0                             | ±1.0                            | μΑ               | $V_I = V_{CC}$ , GND   |  |
| ICCT            | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              |                       | 1.6                              | 1.5                             | mA               | $V_I = V_{CC} - 2.1V$  |  |

175°C

140°C

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'ACTQ Family Devices (Continued)

|                  |   |                        | 74A                      | 74ACTQ 54ACTQ 74ACTQ |                                   | 74ACTQ                          | ge eoe           | If Military/Aerospa<br>plense contact ti             |  |
|------------------|---|------------------------|--------------------------|----------------------|-----------------------------------|---------------------------------|------------------|--|--|
| Symbol Parameter |   | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C   |                      | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units            | Conditions   |  |
|                  |   |                        | Тур                      | atioV tuc            | Guaranteed L                      | imits                           | rent (lpc        | DC Input Diode Qu                                    |  |
| IOLD OF          | †Minimum Dynamic                                | 5.5                    | DV) egat                 | loV tugti            | 50                                | 75                              | mA               | V <sub>OLD</sub> = 1.65V Max                         |  |
| IOHD             | Output Current                                  | 5.5                    | Tengana                  | peraling             | -500 + <sub>00</sub> \            | of Va.0-75                      | mA (             | V <sub>OHD</sub> = 3.85V Min                         |  |
| Icc 331          | Maximum Quiescent Supply Current                | 5.5                    | ACTO<br>nput Edg         | 8.0                  | 160,005                           | 80.0                            | μА               | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | seolvi<br>d 4:16<br>g vn | 1.5                  | /oc + 0.5V                        | of V8.0—                        | VoV              | Figures 1, 2<br>(Notes 2, 3)                         |  |
| V <sub>OLV</sub> | Quiet Output Minimum Dynamic VOL                | 5.0                    | -0.6                     | -1.2                 | ±50 mA M                          |                                 | v (c             | Figures 1, 2 (Notes 2, 3)                            |  |
| V <sub>IHD</sub> | Maximum High Level Dynamic Input Voltage        | 5.0                    | 1.9                      | 2.2                  | 250 mA<br>150°C                   | o)<br>—66°C                     | 118 <b>V)</b> e1 | (Notes 2, 4)   |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.2                      | 0.8                  | Am 008±                           |                                 | ٧                | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     | 271                                   | -                 | 74ACTQ 54ACTQ |                      | CTQ | 74ACTQ   |                         |      |                        |       |             |
|-------------------------------------|---------------------------------------|-------------------|---------------|----------------------|-----|----------|-------------------------|------|------------------------|-------|-------------|
| Symbol                              | Parameter                             | V <sub>CC</sub> * |               | A = +25<br>CL = 50 p |     | to +     | -55°C<br>125°C<br>50 pF | to + | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
| V1.0 =                              | TUOV V 0                              | 2                 | Min           | Тур                  | Max | Min      | Max                     | Min  | Max                    | initA | HIV         |
| f <sub>max</sub>                    | Maximum Clock<br>Frequency            | 5.0               | 125           | 189                  | 8   | 85       | 6.5                     | 110  | vol mum                | MHz   | JiV         |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>Clock to Output  | 5.0               | 1.5           | 6.5                  | 8.5 | 1.5      | 10.0                    | 1.5  | 9.0                    | ns    | 2-3, 4      |
| t <sub>PHL</sub>                    | Propagation Delay MR to Output        | 5.0               | 1.5           | 7.0                  | 9.0 | 1.5      | 11.0                    | 1.5  | 9.5                    | ns    | 2-3, 4      |
| toshl,<br>toslh                     | Output to Output Skew** Data to Ouput | 5.0               |               | 0.5                  | 1.0 | 8<br>.A. | 4.5                     |      | 1.0                    | ns    |             |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). n - 1 Data inputs are driven 0V to 3V; one output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ) f = 1 MHz.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

| <b>AC Operating Requi</b> | rements: See Section 2 for Waveforms |  | -LARWY |
|---------------------------|--------------------------------------|--|--------|
|---------------------------|--------------------------------------|--|--------|

|                  |                                       |   | 744  | CTQ   | 54ACTQ   | 74ACTQ                                 | nicraco     |        |
|------------------|---------------------------------------|---|------|---|--|--|-------------|--------|
| Symbol Parameter |                                       | $V_{CC}^*$ $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |      | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units                                  | Fig.<br>No. |        |
|                  |                                       |   | Тур  | tasu  | Guaranteed Min   | imum () pol                            | ta2 t       | ainC   |
| ts               | Setup Time, HIGH or LOW<br>Data to CP | 5.0   | 1.0  | 3.5   | 5.0  | ® = 3.5                                | ns          | 2-7    |
| th               | Hold Time, HIGH or LOW<br>Data to CP  | 5.0   | -0.5 | 1.5   | 2.0  | nd.5qho                                | ns          | 2-7    |
| t <sub>w</sub>   | Clock Pulse Width<br>HIGH or LOW      | 5.0   | 2.0  | 4.0   | nikw seriolsi ing<br>en ap0.5 ations.                        | er to eleignoc SN                      | ns          | 2-3    |
| t <sub>w</sub>   | MR Pulse Width<br>HIGH or LOW         | 5.0   | 1.5  | 4.0   | ent or selected at   | 4.0                                    | ns          | 2-3    |
| t <sub>rec</sub> | Recovery Time                         | 5.0   | 0.5  | 3.0   | V. Wnen OE is Hit<br>ce state.                               | Table (OE) Is LOY<br>the higo.8 needan | ns          | 2-3, 7 |

\*Voltage Range 5.0 is 5.0V ±0.5V

# Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| C <sub>IN</sub> | Input Capacitance                | 4.5  | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40.0 | pF    | V <sub>CC</sub> = 5.0V |

| Pin Assignment | Pin Assignment | Pin Assignment | Pin Assignment | Pin Assignment | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and SOIC | Pin Petpak and Petpak a



# 54ACQ/74ACQ373 • 54ACTQ/74ACTQ373 Quiet Series Octal Transparent Latch with TRI-STATE® Outputs

# **General Description**

The 'ACQ/'ACTQ373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

The 'ACQ/'ACTQ373 utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

# **Features**

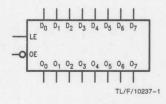
 Guaranteed simultaneous switching noise level and dynamic threshold performance

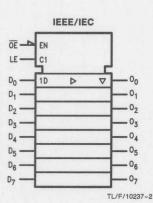
AC Operating Requirements: see Section 2 for Waveforms

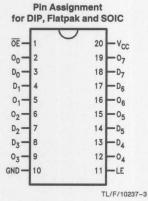
- Guaranteed pin-to-pin skew AC performance
- Improved latch up immunity
- Eight latches in a single package
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT373
- 4 kV minimum ESD immunity ('ACQ)

Ordering Code: See Section 8
Logic Symbols

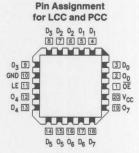
**Connection Diagrams** 







| Pin Names                      | Description             |
|--------------------------------|-------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs             |
| LE                             | Latch Enable Input      |
| ŌĒ                             | Output Enable Input     |
| 00-07                          | TRI-STATE Latch Outputs |



TL/F/10237-4

# Functional Description

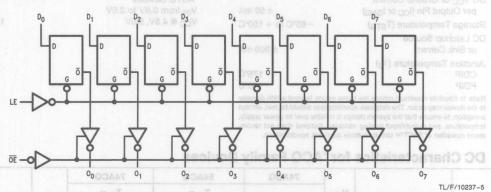
The 'ACQ/'ACTQ373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

# Truth Table 157 mumixsM stuloadA

|              | Inputs | lace specific<br>the Metions | Outputs                   |
|--------------|--------|------------------------------|---------------------------|
| .scLE sobi   | OE OE  | della D <sub>n</sub> not an  | oludinO <sub>n</sub> \sol |
| VO.T X OF V8 | 0- H   | X                            | ov) egatigy viqu          |
| Н            | L      | (¿Li) tnerti                 | input Diode Ou            |
| H            | L      | Н                            | H                         |
| Un US        | L      | X                            | 00                        |

- H = HIGH Voltage Level
- L = LOW Voltage Level Z = High Impedance
- X = Immaterial
- O<sub>0</sub> = Previous O<sub>0</sub> before HIGH to Low transition of Latch Enable

# **Logic Diagram**



| Please note that this diagram is provided or   | ly for the understanding | of logic operations and should not be used to estimate propagation delays. |
|--|--------------------------|--|
| riedse note triat triis diagram is provided of | ly for the understanding | of logic operations and should not be used to estimate propagation delays. |

|  |   |                      | 2.1<br>3.15<br>3.85 |      |  | Minimum High Level<br>Input Voltage |  |
|--|---|----------------------|---------------------|------|--|-------------------------------------|--|
| $V_{CUT} = 0.1V$ or $V_{CC} - 0.1V$  |   |                      |                     |      |  |                                     |  |
|  | V | 2.9<br>4,4<br>5.4    |                     |      |  |                                     |  |
| $\begin{array}{ll} ^{\rm e}V_{\rm IL}\ {\rm or}\ V_{\rm IL} \\ -12\ {\rm mA} \\ -12\ {\rm mA} \\ -24\ {\rm mA} \\ -24\ {\rm mA} \end{array}$ |   | 2.46<br>3,76<br>4,76 | 2.4<br>8.7<br>4.7   |      |  |                                     |  |
| 100т = 50 µА   |   |                      |                     |      |  |                                     |  |
| $^{eV}_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA 10L 24 mA 24 mA   | ٧ |                      |                     |      |  |                                     |  |
|  |   |                      |                     | f.0± |  | Maximum Input<br>Leakage Current    |  |

# Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )  | -0.5V to $+7.0$ V               |
|--|---------------------------------|
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$<br>$V_I = V_{CC} + 0.5V$  | -20 mA<br>+20 mA                |
| DC Input Voltage (V <sub>I</sub> )   | -0.5V to V <sub>CC</sub> + 0.5V |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$ | −20 mA<br>+20 mA                |
| DC Output Voltage (V <sub>O</sub> )  | $-0.5$ V to to $V_{CC} + 0.5$ V |
|  |                                 |

DC Output Source or Sink Current (Io)  $\pm 50$  mA DC V<sub>CC</sub> or Ground Current per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>)  $\pm 50$  mA Storage Temperature (T<sub>STG</sub>)  $-65^{\circ}$ C to  $+150^{\circ}$ C

DC Latchup Source or Sink Current Junction Temperature (T<sub>J</sub>) CDIP PDIP

175°C 140°C ich damage

±300 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating and formal Conditions of the sense of the Conditions of the sense of the Conditions of the Conditi

| Supply Voltage (V <sub>CC</sub> )                  |                       |
|--|-----------------------|
| 'ACQ   | 2.00 10 0.00          |
| 'ACTQ als .e., inelegated els se                   |                       |
| Input Voltage (V <sub>I</sub> )                    | 0V to V <sub>CC</sub> |
| Output Voltage (Vo)                                |                       |
| Operating Temperature (TA)                         |                       |
| 74ACQ/ACTQ   |                       |
| 54ACQ/ACTQ   |                       |
| Minimum Input Edge Rate ΔV/Δt                      |                       |
| 'ACQ Devices                                       |                       |
| V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> | aerone.               |
| V <sub>CC</sub> @ 3.0V, 4.5V, 5.5V                 | 125 mV/ns             |
| Minimum Input Edge Rate ΔV/Δt                      | Logic Diagran         |
| 'ACTQ Devices                                      |                       |
| V <sub>IN</sub> from 0.8V to 2.0V                  | .6                    |
| V <sub>CC</sub> @ 4.5V, 5.5V                       | 125 mV/ns             |

# DC Characteristics for 'ACQ Family Devices

|                 | to 90                                | Se                     | 74                      | ACQ                  | 54ACQ                             | 74ACQ                           |       |  |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |  |
|                 |                                      |                        | Тур                     |                      | Guaranteed Li                     | mits                            |       |  |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | ٧     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | V     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | V     | $I_{OUT} = -50 \mu\text{A}$  |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | V     | $\label{eq:VIN} \begin{split} *V_{IN} &= V_{IL}  or  V_{IH} \\ &- 12  mA \\ I_{OH} &- 24  mA \\ &- 24  mA \end{split}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | V     | I <sub>OUT</sub> = 50 μA   |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              | 0.44<br>0.44<br>0.44            | ٧     | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ 12 mA $I_{OL}$ 24 mA 24 mA   |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                              | ±1.0                            | μА    | V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'ACQ Family Devices (Continued) 101 applications of the continued of

|                  |   | SACTO                  | 74.                    | ACQ TO   | 54ACQ OTO                         | 74ACQ                           |                 |  |  |
|------------------|---|------------------------|------------------------|----------|-----------------------------------|---------------------------------|-----------------|--|--|
| Symbol           | Parameter O'88                                  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |          | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units           | Conditions   |  |
|                  |   |                        | Тур                    | l beeing | Guaranteed Li                     | imits                           |                 |  |  |
| IOLD             | †Minimum Dynamic                                | 5.5                    |                        | -        | 50                                | 75                              | mA              | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD             | Output Current                                  | 5.5                    |                        |          | -50                               | -75                             | mA              | V <sub>OHD</sub> = 3.85V Min   |  |
| Icc              | Maximum Quiescent<br>Supply Current             | 5.5                    |                        | 8.0      | 160.0                             | 0.0 80.0                        |                 | V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)                        |  |
| loz<br>(1 eso    | Maximum TRI-STATE<br>Leakage Current            | 5.5                    |                        | ±0.5     | ± 10.0 <sup>0.8</sup>             | ±5.0                            | μА              | $V_{I}(OE) = V_{IL}, V_{IH}$ $V_{I} = V_{CC}, GND$ $V_{O} = V_{CC}, GND$ |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1.1                    | 1.5      | d,f                               | f.f U.8                         | V               | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>OLV</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | -0.6                   | -1.2     | 2.7-                              | 8.0 - 0.8                       | V <sup>SS</sup> | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage     | 5.0                    | 3.1                    | 3.5      | 8.3                               | 2.0 0.0 age                     | lo\v_viqr       | (Notes 2, 4)   |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.9                    | 1.5      | 8.0                               | S.F U.C age                     | NoV Vigi        | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# DC Characteristics for 'ACTQ Family Devices

|                 | 10 + 85°C Unit   | 0.68                   | 74A                        | CTQ          | 54ACTQ                            | 74ACTQ                          | Parame                      | Symbol  |  |
|-----------------|--|------------------------|----------------------------|--------------|-----------------------------------|---------------------------------|-----------------------------|---|--|
| Symbol          | Parameter  | V <sub>CC</sub><br>(V) | T <sub>A</sub> =           | + 25°C       | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units                       | Conditions  |  |
|                 | 7.64 3.0   | A.WHIL                 | Тур                        | 2.01         | Guaranteed Li                     | mits                            | Clesion                     |   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage                              | 4.5<br>5.5             | 1.5<br>1.5                 | 2.0          | 2.0<br>2.0                        | 0.8 2.0<br>2.0                  | V                           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage                               | 4.5<br>5.5             | 1.5<br>1.5                 | 0.8          | 0.8                               | 0.8                             | V                           | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level Output Voltage                                | 4.5<br>5.5             | 4.49<br>5.49               | 4.4<br>5.4   | 5.4                               | 4.4<br>5.4                      | ٧                           | $I_{OUT} = -50 \mu\text{A}$   |  |
| 2-5, 6          | 1.0 10.0 ns  | 4.5<br>5.5             |                            | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | aju <b>V</b> or             | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage                              | 4.5<br>5.5             | 0.001<br>0.001             | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | 0± <b>V</b> 0.8             | I <sub>OUT</sub> = 50 μA  |  |
| noltsolito      | ujpute of the same device. The apu<br>oter guaranteed by dueign. | 4.5<br>5.5             | e pay (wa si<br>JGH (last) | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | uloade ed<br>goldotiwe<br>V | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub> | Maximum Input Leakage<br>Current                                 | 5.5                    |                            | ±0.1         | ±1.0                              | ±1.0                            | μΑ                          | $V_{I} = V_{CC}$ , GND  |  |
| loz             | Maximum TRI-STATE<br>Leakage Current                             | 5.5                    |                            | ±0.5         | ±10.0                             | ±5.0                            | μΑ                          | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1:  $I_{\text{IN}}$  and  $I_{\text{CC}}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{\text{CC}}$ . Icc for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>ILD</sub>), AC Electrical Characteristics: See Section 2 for Waveforms

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'ACTQ Family Devices (Continued)

|                  |  | OOAt            | 74ACTQ           |        | 54ACTQ                            | 7    | 4ACTQ                          |       |  |  |
|------------------|--|-----------------|------------------|--------|-----------------------------------|------|--------------------------------|-------|--|--|
| Symbol           | Parameter Oral                           | V <sub>CC</sub> | T <sub>A</sub> = | + 25°C | T <sub>A</sub> = -55°C to + 125°C | -40° | T <sub>A</sub> =<br>C to +85°C | Units | Conditions   |  |
|                  |  |                 | Тур              | beeins | Guaranteed Li                     | mits |                                |       |  |  |
| ICCT Vaa.        | Maximum Am                               | 5.5             | 0.6              | 0 50   | 1.6                               |      | 1.5                            | mA    | $V_I = V_{CC} - 2.1V$                                |  |
| IOLD             | †Minimum Dynamic                         | 5.5             |                  |        | 50                                |      | 75                             | mA    | V <sub>OLD</sub> = 1.65V Max                         |  |
| IOHD 00          | Output Current                           | 5.5             |                  | 0,0    | -50                               |      | -75                            | mA    | V <sub>OHD</sub> = 3.85V Min                         |  |
| Icc V alV        | Maximum Quiescent<br>Supply Current      | 5.5             |                  | 8.0    | 160.0                             |      | 80.0                           | μА    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |  |
| V <sub>OLP</sub> | Maximum High Level<br>Output Noise       | 5.0             | 1.1              | 1.5    | 2.                                |      | 0.3                            | V     | Figures 1, 2<br>(Notes 2, 3)                         |  |
| Volv             | Maximum Low Level Output Noise           | 5.0             | -0.6             | -1.2   | 0.4                               | 5 Pa | JOV JOV                        | V tu  | Figures 1, 2<br>(Notes 2, 3)                         |  |
| V <sub>IHD</sub> | Maximum High Level Dynamic Input Voltage | 5.0             | 1.9              | 2.2    | 20                                | 2.0  | VOL.                           | V     | (Notes 2, 4)   |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage  | 5.0             | 1.2              | 0.8    |                                   |      | 993<br>16                      | V     | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |  |                   | 81         | 74ACQ                   | i viima     | 54A   | CQ  | 74/  | ACQ          | Chan  | 00          |
|-------------------------------------|--|-------------------|------------|-------------------------|-------------|---|-----|--|--------------|-------|-------------|
| Symbol                              | Parameter  | V <sub>CC</sub> * |            | C <sub>L</sub> = +250 p |             | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |              | Units | Fig.        |
|                                     | 98.0   | + 03 0,09 -       | Min        | Тур                     | Max         | Min   | Max | Min  | Max          |       | Contract of |
| tphL, tpLH                          | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | 3.3<br>5.0        | 2.5<br>1.5 | 8.0<br>5.5              | 10.5<br>7.0 | 1.5   | 4,5 | 2.5<br>1.5   | 11.0<br>7.5  | ns    | 2-3, 4      |
| tpLH, tpLH                          | Propagation Delay<br>LE to On                      | 3.3<br>5.0        | 2.5<br>2.0 | 8.0<br>6.0              | 12.0<br>8.0 | 1.6   | 8,8 | 2.5  | 12.5<br>8.5  | ns    | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                                 | 3.3 5.0           | 2.5<br>1.5 | 8.5<br>4.4 6.5          | 13.0<br>8.5 | 1.5   | 4.5 | 2.5<br>1.5   | 13.5<br>9.0  | ns    | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                                | 3.3<br>5.0        | 1.0        | 9.0<br>6.5              | 14.5<br>9.5 | 99.6  | n n | 1.0<br>1.0   | 15.0<br>10.0 | ns    | 2-5, 6      |
| toshl,                              | Output to Output Sker                              | w** 3.3<br>5.0    |            | 1.0<br>0.5              | 1.5<br>1.0  |   | 8.8 |  | 1.5          | ns    |             |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$  0.5V.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Voltage Range 3.3 is 3.3V ±0.3V.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl) or LOW to HIGH (toslh). Parameter guaranteed by design.

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The 'ACQ/'ACTQ374 utilizes Culet Series tech

|                  |   |                   | 74.        | ACQ             | 54ACQ  | 74ACQ  | ma2   |             |
|------------------|---|-------------------|------------|-----------------|--|--|-------|-------------|
| Symbol Parameter | Parameter                                       | V <sub>CC</sub> * |            | + 25°C<br>50 pF | $T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$ | $T_A = -40^{\circ}C$ to $+85^{\circ}C$ $C_L = 50 \text{ pF}$ | Units | Fig.<br>No. |
|                  |   |                   | Тур        | (2/3/2          | <b>Guaranteed Min</b>  | 0210   | hiΩ   |             |
| ts               | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 3.3<br>5.0        | 0          | 3.0<br>3.0      | Outputs  | 3.0<br>3.0   | ns    | 2-7         |
| th               | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 3.3<br>5.0        | 0          | 1.5<br>1.5      |  | 1.5<br>1.5   | ns    | 2-7         |
| t <sub>w</sub>   | LE Pulse Width, HIGH                            | 3.3<br>5.0        | 2.0<br>2.0 | 4.0<br>4.0      | ed, low-power oots<br>pe inputs for each                           | 4.0<br>4.0   | ns ns | 2-3         |

buffered Clock (CP) and Output Enable (OE) are common to simproved tatch-up immunity

\*Voltage Range 5.0 is 5.0V  $\pm$ 0.5V. Voltage Range 3.3 is 3.3V  $\pm$ 0.3V.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     | At                               | V <sub>CC</sub> *<br>(V) | s/aonnos   | 74ACTQ | enut | 54A  | CTQ I | 74A  | СТО  | nghaq bl | thresho     |
|-------------------------------------|----------------------------------|--------------------------|--|--------|------|--|-------|--|------|----------|-------------|
| Symbol                              | Parameter Vin                    |                          | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |        |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |       | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units    | Fig.<br>No. |
|                                     |                                  |                          | Min  | Тур    | Max  | Min  | Max   | Min  | Max  | pring    | Orde        |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay                | 5.0                      | 2.0  | 6.5    | 7.5  | 1.5  | 10.5  | 2.0  | 8.0  | ns       | 2-3, 4      |
| t <sub>PLH</sub> , t <sub>PLH</sub> | Propagation Delay<br>LE to On    | 5.0                      | 2.5  | 7.0    | 8.5  | 1.5  | 11.5  | 2.5  | 9.0  | ns       | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time               | 5.0                      | 2.0  | 7.0    | 9.0  | 1.5  | 11.0  | 2.0  | 9.5  | ns       | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time              | 5.0                      | 1.0  | 8.0    | 10.0 | 1.5  | 10.5  | 1.0  | 10.5 | ns       | 2-5, 6      |
| toshl,                              | Output to Output Skew** Dn to On | 5.0                      |  | 0.5    | 1.0  | James 93   |       |  | 1.0  | ns       | 10          |

\*Voltage Range 5.0 is 5.0V  $\pm$ 0.5V. Voltage Range 3.3 is 3.3V  $\pm$ 0.3V.

\*\*Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHI) or LOW to HIGH (toSLH). Parameter guaranteed by design.

# AC Operating Requirements: See Section 2 for Waveforms

| Symbol S-88    | 90-11 01-089<br>Parameter                       | V <sub>CC</sub> * | 74ACTQ  T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF |     | 54ACTQ   | 74ACTQ   | Units | Fig.<br>No. |
|----------------|---|-------------------|---|-----|--|--|-------|-------------|
|                |   |                   |   |     | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |       |             |
|                |   |                   | Тур   |     | Guaranteed Min   |  |       |             |
| t <sub>s</sub> | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0               | 0   | 3.0 | 3.5  | 3.0  | ns    | 2-7         |
| th             | Hold Time, HIGH or LOW                          | 5.0               | 0   | 1.5 | 1.5 <sub>fugo</sub>  | Student stadd  | ns    | 2-7         |
| t <sub>w</sub> | LE Pulse Width, HIGH                            | 5.0               | 2.0   | 4.0 | 5.0  | 4.0  | ns    | 2-3         |

\*Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

\*Voltage Range 3.3 is 3.3V ±0.3V

# Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions             |
|-----------------|-------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation Capacitance | 44.0 | pF    | V <sub>CC</sub> = 5.0V |



# 54ACQ/74ACQ374 • 54ACTQ/74ACTQ374 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

# **General Description**

The 'ACQ/'ACTQ374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops.

The 'ACQ/'ACTQ374 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

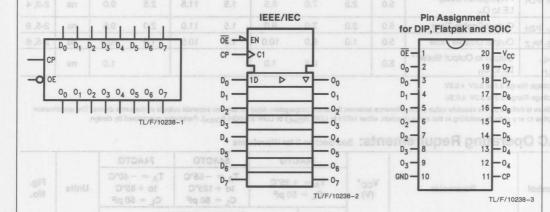
# **Features**

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT374
- 4 kV minimum ESD immunity

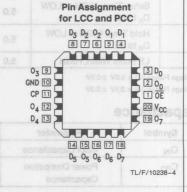
Ordering Code: See Section 8

**Logic Symbols** 

# **Connection Diagrams**



| Pin Names                            | Description                   |  |  |  |  |
|--------------------------------------|-------------------------------|--|--|--|--|
| D <sub>0</sub> -D <sub>7</sub>       | Data Inputs                   |  |  |  |  |
| D <sub>0</sub> -D <sub>7</sub><br>CP | Clock Pulse Input             |  |  |  |  |
| ŌĒ                                   | TRI-STATE Output Enable Input |  |  |  |  |
| 00-07                                | TRI-STATE Outputs             |  |  |  |  |



# **Functional Description**

The 'ACQ/'ACTQ374 consists of eight edge-triggered flipflops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{\text{OE}}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{\text{OE}}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{\text{OE}}$  input does not affect the state of the flip-flops.

# Truth Table its R mumixs M etuloed A

| pequired, | Inputs            | ece specifie   | Outputs          |
|-----------|-------------------|----------------|------------------|
| Dn        | off page CPs vill | della OE sot a | rohudhiOn\selfi( |
| V0.7 H of | V80-              | L 60           | upply VHtage (Vo |
| L         | _                 | (al) men       | C Input Diode Cu |
| X         | X                 | Н              | V3.02 = V        |

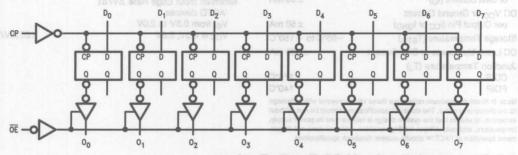
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance \_ = LOW-to-HIGH Transition

# **Logic Diagram**



TL/F/10238-5
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

|   | adinü |  |                     |                      |  |  |                                     |     |
|---|-------|--|---------------------|----------------------|--|--|-------------------------------------|-----|
| Conditions  |       |  |                     |                      |  |  |                                     |     |
|   |       |  |                     |                      |  |  |                                     |     |
| $V_{COT} = 0.1V$ $V_{CO} - 0.1V$  |       |  | 7.S<br>37.D<br>38.E | 2.15<br>3.15<br>3.85 |  |  | Minimum High Level<br>Input Voltage |     |
| $V_{OUT} = 0.1V$ $V_{OC} - 0.1V$  |       |  |                     | 6.0<br>86.1<br>86.1  |  |  |                                     |     |
|   |       |  |                     |                      |  |  |                                     |     |
|   | ٧     |  |                     | 2.56<br>3.66<br>4.66 |  |  |                                     |     |
|   |       |  |                     | 1.0<br>1.0<br>1.0    |  |  | Maximum Low Level<br>Output Voltage | Vot |
| $V_{\rm IM} = V_{\rm IL} \ {\rm or} \ V_{\rm IM}$ for $V_{\rm IM} = V_{\rm IL} \ {\rm or} \ V_{\rm IM}$ |       |  |                     |                      |  |  |                                     |     |
|   | Au    |  |                     |                      |  |  | Naximum Input<br>Laakage Curent     |     |

| Supply Voltage (V <sub>CC</sub> )                     | -0.5V to +7.0V                  |
|---|---------------------------------|
| DC Input Diode Current (I <sub>IK</sub> )             |                                 |
| $V_1 = -0.5V$   | -20 mA                          |
| $V_I = V_{CC} + 0.5V$                                 | + 20 mA                         |
| DC Input Voltage (V <sub>I</sub> )                    | $-0.5V$ to $V_{CC} + 0.5V$      |
| DC Output Diode Current (IOK)                         |                                 |
| $V_0 = -0.5V$   | -20 mA                          |
| $V_O = V_{CC} + 0.5V$                                 | + 20 mA                         |
| DC Output Voltage (V <sub>O</sub> )                   | $-0.5$ V to to $V_{CC} + 0.5$ V |
| DC Output Source                                      |                                 |
| or Sink Current (I <sub>O</sub> )                     | ±50 mA                          |
| DC V <sub>CC</sub> or Ground Current                  |                                 |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                          |
| Storage Temperature (T <sub>STG</sub> )               | -65°C to +150°C                 |
| DC Latch-Up Source or Sink Curren                     | t ±300 mA                       |
| Junction Temperature (T <sub>.I</sub> )               |                                 |
| CDIP  | 175°C                           |
|   |                                 |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

| 'ACQ  |                 | E.O 4 10 0.0 4 |    |
|---|-----------------|----------------|----|
| Input Voltage (V <sub>I</sub> )   |                 | OV to VCC      |    |
| Output Voltage (V <sub>O</sub> )  |                 | OV to Vcc      |    |
| Operating Temperature (T <sub>A</sub> ) 74ACQ/ACTQ 54ACQ/ACTQ   | -40 application | °C to +85°C    |    |
| Minimum Input Edge Rate $\Delta V/\Delta t$ 'ACQ Devices $V_{IN}$ from 30% to 70% of $V_{CC}$ $V_{CC}$ @ 3.0V, 4.5V, 5.5V |                 | 125 mV/ns      | -  |
| Minimum Input Edge Rate ΔV/Δt 'ACTQ devices V <sub>IN</sub> from 0.8V to 2.0V   |                 | 105 mV/ac      |    |
| V <sub>CC</sub> @ 4.5V, 5.5V  |                 | 125 mV/r       | 18 |

# **DC Characteristics for 'ACQ Family Devices**

|                 |                                      |                        | 74                      | ACQ                  | 54ACQ                             | 74ACQ                           |       |  |  |
|-----------------|--------------------------------------|------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|-------|--|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |  |
|                 |                                      |                        | Тур                     | Guaranteed Limits    |                                   | mits                            |       |  |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | ٧     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | ٧     | $I_{OUT} = -50 \mu\text{A}$  |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | ٧     | $\label{eq:VIN} \begin{split} *V_{\text{IN}} &= V_{\text{IL}}  \text{or}  V_{\text{IH}} \\ &- 12  \text{mA} \\ I_{\text{OH}} &- 24  \text{mA} \\ &- 24  \text{mA} \end{split}$ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | ٧     | Ι <sub>ΟUT</sub> = 50 μΑ   |  |
|                 |                                      | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              | 0.44<br>0.44<br>0.44            | ٧     | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{12} \text{ mA}$ $^{1}_{OL}$ $^{24} \text{ mA}$ $^{24} \text{ mA}$  |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                              | ±1.0                            | μА    | V <sub>I</sub> = V <sub>CC</sub> , GND<br>(Note 1)   |  |

 $<sup>^{*}</sup>$ All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  | 1000  | (A) | wer's w | SER TO SER ! | -55°C to + 125°C   - | -40°C to + | 85°C           | - Conditions   |
|------------------|---|-----|---------|--------------|----------------------|------------|----------------|--|
|                  |   |     | Тур     | Guarantead   | Guaranteed Limi      | ts         |                |  |
| IOLD             | †Minimum Dynamic                                | 5.5 |         | 9.1          | 50                   | 75         | m/             | V <sub>OLD</sub> = 1.65V Max                         |
| IOHD             | Output Current                                  | 5.5 |         |              | -50                  | -75        | m/             | V <sub>OHD</sub> = 3.85V Min                         |
| Icc              | Maximum Quiescent<br>Supply Current             | 5.5 |         | 8.0          | 160.0                | 80.0       | μΑ             | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |
| loz († etc       | Maximum TRI-STATE<br>Leakage Current            | 5.5 |         | ±0.5         | ±10.0                | ±50        | intoasii<br>μΑ | - K/ ILD ILD   |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0 | 1.1     | 1.5          | 6.1                  | 10.6       | No almen       | Figures 1 and 2<br>(Notes 2 and 3)                   |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0 | -0.6    | -1.2         | 5.7- 0.0             | 0.6        | V              | Figures 1 and 2<br>(Notes 2 and 3)                   |
| V <sub>IHD</sub> | Maximum High Level<br>Dynamic Input Voltage     | 5.0 | 3.1     | 3.5          | 5.5                  | 0.0        | egs oV         | (Notes 2 and 4)                                      |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0 | 1.9     | 1.5          | topingson son to     | W.C.       | egal eV V      | (Notes 2 and 4)                                      |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## **DC Characteristics for 'ACTQ Family Devices**

|                 | TA = -APC   |                        | 74A                          | СТО          | 54ACTQ                            | 74ACTQ                          |                |  |
|-----------------|---|------------------------|------------------------------|--------------|-----------------------------------|---------------------------------|----------------|--|
| Symbol          | Parameter 12  | V <sub>CC</sub><br>(V) |                              |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units          | Conditions   |
|                 | xeM alk   |                        | Тур                          | EXECUTE N    | Guaranteed Li                     | mits                            |                |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage                       | 4.5<br>5.5             | 1.5<br>1.5                   | 2.0<br>2.0   | 2.0<br>2.0                        | 2.0<br>2.0                      | ٧              | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| VIL             | Maximum Low Level Input Voltage                           | 4.5<br>5.5             | 1.5<br>1.5                   | 0.8          | 0.8<br>0.8                        | 0.8<br>0.8                      | V              | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V   |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage                      | 4.5<br>5.5             | 4.49<br>5.49                 | 4.4<br>5.4   | 4.4<br>5.4                        | 4.4<br>5.4                      | ٧              | $I_{OUT} = -50 \mu\text{A}$  |
| 2-5, 6          | 1.0 16.0 ns   | 4.5<br>5.5             |                              | 3.86<br>4.86 | 3.70<br>4.70                      | 3.76<br>4.76                    | V              | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| VOL             | Maximum Low Level Output Voltage                          | 4.5<br>5.5             | 0.001<br>0.001               | 0.1<br>0.1   | 0.1<br>0.1                        | 0.1<br>0.1                      | V <sub>a</sub> | I <sub>OUT</sub> = 50 μA   |
| noitection      | us of the earns device. The ap<br>r guaranteed by dealon. | 4.5<br>5.5             | toss owi vivi<br>Lituago His | 0.36<br>0.36 | 0.50<br>0.50                      | 0.44<br>0.44                    | ٧              | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |
| IIN             | Maximum Input<br>Leakage Current                          | 5.5                    |                              | ±0.1         | ±1.0                              | ±1.0                            | μΑ             | $V_I = V_{CC}$ , GND   |
| loz             | Maximum TRI-STATE<br>Current                              | 5.5                    | ndist                        | ±0.5         | ±10.0                             | ±5.0                            | μА             | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'ACTQ Family Devices (Continued) and additional additional and additional additional additional additional and additional additio

|                  |   | PAACO                  | 74A                    | СТО         | 54ACTQ                           | 74ACTQ                          |       |  |  |
|------------------|---|------------------------|------------------------|-------------|----------------------------------|---------------------------------|-------|--|--|
| Symbol           | Parameter 3788                                  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |             | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units | Conditions   |  |
|                  |   |                        | Тур                    | es editeres | Guaranteed Li                    | mits                            |       |  |  |
| ICCT / 83        | Maximum I <sub>CC</sub> /Input                  | 5.5                    | 0.6                    | 50          | 1.6                              | 1.5                             | mA    | $V_I = V_{CC} - 2.1V_I$                              |  |
| lold             | †Minimum Dynamic                                | 5.5                    | -                      |             | 50                               | 75                              | mA    | V <sub>OLD</sub> = 1.65V Max                         |  |
| IOHD             | Output Current                                  | 5.5                    |                        | 0.081       | -50                              | -75                             | mA    | V <sub>OHD</sub> = 3.85V Min                         |  |
| ICC V AIV        | Maximum Quiescent<br>Supply Current             | 5.5                    |                        | 8.0         | 160.0                            | 80.0                            | μА    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1.1                    | 1.5         |                                  | 12 02                           | V     | Figures 1 and 2<br>(Notes 2 and 3)                   |  |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6                   | -1.2        | 5 - 6                            | 2 Vot.                          | ٧     | Figures 1 and 2<br>(Notes 2 and 3)                   |  |
| V <sub>IHD</sub> | Maximum High Level Dynamic Input Voltage        | 5.0                    | 1.9                    | 2.2         | 5.0                              | JOV Jay                         | ٧     | (Notes 2 and 4)                                      |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.2                    | 0.8         | 2.4                              | egai                            | V     | (Notes 2 and 4)                                      |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>ILD</sub>), f = 1 MHz.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |                                  | TE                | 81         | 74ACC          |             | 54   | ACQ                          | 74/        | ACQ                    | Chart | 00          |
|-------------------------------------|----------------------------------|-------------------|------------|----------------|-------------|------|------------------------------|------------|------------------------|-------|-------------|
| Symbol                              | Parameter and organization       | V <sub>CC</sub> * |            | = +2<br>L = 50 |             | to - | - 55°C<br>+ 125°C<br>= 50 pF | to +       | -40°C<br>85°C<br>50 pF | Units | Fig.<br>No. |
|                                     | MODELLE                          | Man .             | Min        | Тур            | Max         | Min  | Max                          | Min        | Max                    |       |             |
| f <sub>max</sub>                    | Maximum Clock<br>Frequency       | 3.3<br>5.0        | 75<br>90   | 2.0            |             | 0.8  | 8.1 8                        | 70<br>85   | s.i rigiH mu           | MHz   | H/V         |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation Delay<br>CP to On    | 3.3<br>5.0        | 3.0<br>2.0 | 9.5<br>6.5     | 13.0<br>8.5 | 8.0  | 5 1.6                        | 3.0<br>2.0 | 13.5<br>9.0            | ns    | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time               | 3.3<br>5.0        | 3.0<br>2.0 | 9.5<br>6.5     | 13.0<br>8.5 | A,b  | 8 4.49                       | 3.0<br>2.0 | 13.5<br>9.0            | ns    | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time              | 3.3<br>5.0        | 1.0<br>1.0 | 9.5<br>8.0     | 14.5<br>9.5 |      |                              | 1.0<br>1.0 | 15.0<br>10.0           | ns    | 2-5, 6      |
| toshl,                              | Output to Output Skew** CP to On | 3.3<br>5.0        |            | 1.0<br>0.5     | 1.5<br>1.0  | 98.8 | 5                            | 8          | 1.5<br>1.0             | ns    |             |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND OF STATE OF STA

Voltage Range 3.3 is 3.3V ±0.3V

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshL) or LOW to HIGH (tosLH). Parameter guaranteed by design.

# AC Operating Requirements: See Section 2 for Waveforms

|                    |   |                   | 74         | ACQ               | 54ACQ  | 74ACQ  | I Semi               |             |
|--------------------|---|-------------------|------------|-------------------|--|--|----------------------|-------------|
| Symbol             | Parameter                                       | V <sub>CC</sub> * |            | + 25°C<br>= 50 pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units                | Fig.<br>No. |
|                    | eldenE  | ock               | Тур        | w act             | Guaranteed Min   | imum 🗎 💍   | et Se                | ŧυŌ         |
| t <sub>s</sub>     | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 3.3<br>5.0        | 0          | 3.0<br>3.0        |  | 3.0<br>3.0   | ns                   | 2-7         |
| t <sub>h</sub> -yb | Hold Time, HIGH or LOW                          | 3.3<br>5.0        | 0 2.0      | 1.5<br>1.5        | ggered D-typs flip f<br>uts. The common I                      | 1.5  | ns<br>ns             | 2-7         |
| t <sub>w</sub>     | CP Pulse Width,<br>HIGH or LOW                  | 3.3<br>5.0        | 2.0<br>2.0 | 4.0               | p-flogs sinuitenam<br>w. The register is                       | 4.0  | (90) Abo<br>(90) Abo | 2-3         |

# AC Electrical Characteristics: See Section 2 for Waveforms 10 and Auditor O a golf-oil publication and an action of the control of the contro

|                                     |                                  | on clock          | mmoo. | 74ACT          | Q    | 54A0   | TQ   | 74A    | CTQ                    | n for pred | ransitio    |
|-------------------------------------|----------------------------------|-------------------|-------|----------------|------|--|------|--------|------------------------|------------|-------------|
| Symbol                              | Parameter                        | V <sub>CC</sub> * |       | = +2<br>L = 50 |      | T <sub>A</sub> = -<br>to + 1<br>C <sub>L</sub> = ! | 25°C | * to + | -40°C<br>85°C<br>50 pF | Units      | Fig.<br>No. |
|                                     |                                  |                   | Min   | Тур            | Max  | Min  | Max  | Min    | Max                    | albaugas   | Bas a c     |
| f <sub>max</sub>                    | Maximum Clock<br>Frequency       | 5.0               | 85    |                |      | 95   |      | 80     | nine                   | MHz        | dan         |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation Delay<br>CP to On    | 5.0               | 2.0   | 7.0            | 9.0  | 2.0  | 11.5 | 2.0    | 9.5                    | ns         | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time               | 5.0               | 2.0   | 7.5            | 9.0  | 2.0  | 11.5 | 2.0    | 9.5                    | ns         | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time              | 5.0               | 1.0   | 8.0            | 10.0 | 1.5  | 10.5 | 1.0    | 10.5                   | ns         | 2-5, 6      |
| toshl,                              | Output to Output Skew** CP to On | 5.0               | 00    | 0.5            | 1.0  | 02 - 120   |      |        | 1.0                    | ns         | 90          |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

# AC Operating Requirements: See Section 2 for Waveforms

|                | 0-101   |                       | 74A  | СТО | 54ACTQ   | 74ACTQ   |       |             |
|----------------|---|-----------------------|--|-----|--|--|-------|-------------|
| Symbol         | Parameter                                       | V <sub>CC</sub> * (V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units | Fig.<br>No. |
|                |   |                       | Тур  |     | Guaranteed Min   | imum   |       |             |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0                   | 0  | 3.0 | 3.5  | 3.0  | ns    | 2-7         |
| th             | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 5.0                   | 0  | 1.5 | 2.0  | ock Enable (Active<br>13.0 Outputs                         | ns    | 2-7         |
| t <sub>w</sub> | CP Pulse Width,<br>HIGH or LOW                  | 5.0                   | 2.0  | 4.0 | 5.0  | high Pulse Input<br>4.0                                    | ns    | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

# Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions             |
|-----------------|-------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation Capacitance | 42.0 | pF    | V <sub>CC</sub> = 5.0V |

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshi) or LOW to HIGH (toshi). Parameter guaranteed by design.

Symbol



# 54ACQ/74ACQ377 • 54ACTQ/74ACTQ377 Quiet Series Octal D Flip-Flop with Clock Enable

#### **General Description**

The 'ACQ/'ACTQ377 has 8 edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is low. The register is fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The CE input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT377

14 15 16 17 18 D<sub>5</sub> Q<sub>5</sub> Q<sub>6</sub> D<sub>6</sub> D<sub>7</sub>

TL/F/10151-4

■ 4 kV minimum ESD immunity

#### **Logic Symbols Connection Diagrams Pin Assignment** IEEE/IEC for DIP, Flatpak and SOIC 20 Do D1 D2 D3 D4 D5 D6 D7 00. 19 - Q7 Qo 2D Do Q1 17 Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 02 16 -Q8 03 D3 -Q2 15 -Q<sub>5</sub> TL/F/10151-1 Q4 DA . D2 14 -D5 Q<sub>5</sub> D3 13 -D4 D6 . Q6 12 -Q4 Q3 D7 -GND -TL/F/10151-2 TL/F/10151-3 **Pin Names** Description **Data Inputs** D0-D7 Pin Assignment CE Clock Enable (Active LOW) for LCC Q0-Q7 **Data Outputs** D<sub>3</sub> D<sub>2</sub> Q<sub>2</sub> Q<sub>1</sub> D<sub>1</sub> 8 7 6 5 4 CP Clock Pulse Input Q3 9 3 D<sub>0</sub> 2 Q<sub>0</sub> GND 10 CP 11 1 CE Q4 12 20 V<sub>CC</sub> D4 13 19 Q<sub>7</sub>



# 54ACQ/74ACQ533 • 54ACTQ/74ACTQ533 Quiet Series Octal Transparent Latch with TRI-STATE® Outputs

#### **General Description**

The 'ACQ/'ACTQ533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

The 'ACQ/'ACTQ533 utilizes NSC Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### Features

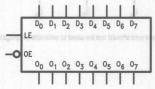
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch up immunity
- Eight latches in a single package
- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Inverted version of the 'ACQ/'ACTQ373
- 4 kV minimum ESD immunity

Ordering Code: See Section 8

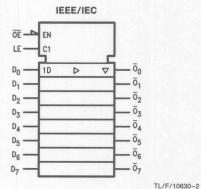
**Logic Symbols** 

# **Connection Diagrams**

GND -



TL/F/10630-1

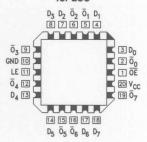


| Pin Names                         | Description             |
|-----------------------------------|-------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs             |
| LE                                | Latch Enable Input      |
| ŌĒ                                | Output Enable Input     |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Latch Outputs |

TL/F/10630-3

# Pin Assignment for LCC

11 -LE



TL/F/10630-4

input is HIGH, data on the  $D_\Pi$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

| LE    | OE      | Dn    | On               |
|-------|---------|-------|------------------|
| X     | COHO    | X     | Z                |
| Н     | L       | L     | Н                |
| H     | ISLOO   | 20H 9 | Outet 6          |
| A. L. | A Chier | X     | $\overline{O}_0$ |

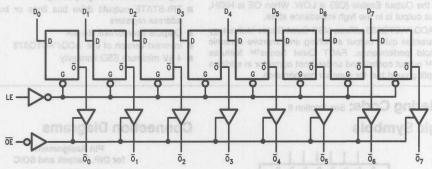
H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance X = Immaterial

 $\overline{O}_0$  = Previous  $\overline{O}_0$  before HIGH to Low transition of Latch Enable

#### **Logic Diagram**



TL/F/10630-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| r |   |   | 3 |  |
|---|---|---|---|--|
| ı | , | 4 |   |  |
| L | d | ĸ | ٦ |  |
| r | ٩ | , | 1 |  |
|   |   |   |   |  |

| Supply Voltage (V <sub>CC</sub> )  | 8+ 010 01-0. | 5V to +7.0V            | 'ACTQ                         |                       |          | 4.5V                                    | to 5.5V              |
|--|--------------|------------------------|-------------------------------|-----------------------|----------|---|----------------------|
| DC Input Diode Current (I <sub>IK</sub> )  |              | Ggaranteed Li          | Input Volt                    | age (V <sub>I</sub> ) |          | 0\                                      | to V <sub>CC</sub>   |
| $V_{I} = -0.5V$<br>$V_{I} = V_{CC} + 0.5V$   |              | -20 mA<br>+20 mA       | Output Vo                     |                       | 2000     |   | / to V <sub>CC</sub> |
| DC Input Voltage (V <sub>I</sub> )   | ∂√0.5V to    | V <sub>CC</sub> + 0.5V | Operating<br>74ACQ            |                       | ature (1 | √A) —40°C to                            | +85°C                |
| DC Output Diode Current (IOK)  |              |                        | 54ACQ                         | /ACTQ                 |          | medean -55°C to                         | + 125°C              |
| $V_{O} = -0.5V$<br>$V_{O} = V_{CC} + 0.5V$   |              | -20 mA<br>+20 mA       | Minimum<br>'ACQ D             |                       | ge Rate  | Supply Current τΔ\VΔ e                  |                      |
| DC Output Voltage (V <sub>O</sub> ) DC Output Source or Sink Current (I <sub>O</sub> )     | -0.5V to     | ±50 mA                 | V <sub>IN</sub> from          | m 30% to<br>3.0V, 4.5 | V, 5.5V  | manuO apada 125                         | s mV/ns              |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) |              | ±50 mA                 | 'ACTQ<br>V <sub>IN</sub> from | Devices<br>m 0.8V to  | 2.0V     |   |                      |
| Storage Temperature (T <sub>STG</sub> )  | -65°         | C to + 150°C           | V <sub>CC</sub> @             | 4.5V, 5.5             | /        | tuotuO teluO                            | mV/ns                |
| DC Latchup Source<br>or Sink Current   |              | ±300 mA                |                               |                       |          |   |                      |
| Junction Temperature (T <sub>J</sub> ) CDIP  |              | 175°C                  |                               |                       |          |   |                      |
| PDIP  Note 1: Absolute maximum ratings are to the device may occur. The databook           |              |                        |                               |                       |          | Maximum Low Level Dynamic Ingut Voltage |                      |

temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# **DC Characteristics for 'ACQ Family Devices**

|  |                                      |                        | 74                      | ACQ                  | 54ACQ                        | unit one     | stugei é          | 74ACQ                | aribit | etegiua ta           | sodmun xat/l £ etcl)   |
|--|--------------------------------------|------------------------|-------------------------|----------------------|------------------------------|--------------|-------------------|----------------------|--------|----------------------|--|
| Symbol   | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to +1 | 25°C         | -40               | T <sub>A</sub> =     | 5°C    | Units                | Conditions   |
|  |                                      |                        | Тур                     | 890                  | Guarante                     | ed Li        | mits              | A' not a             | oll    | ches                 | DC Charac  |
| VIH  | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85          | NT<br>- AT   | Vco               | 2.1<br>3.15<br>3.85  | tel    | V                    | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>                                      | Maximum Low Level Input Voltage      | 3.0<br>4.5<br>5.5      | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65          | Typ          | 8.4               | 0.9<br>1.35<br>1.65  | le     | V<br>veul rigit-l    | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$  |
| VOH.0 =  | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5      | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4            | 1.5          | 5.5<br>4.5<br>5.6 | 2.9<br>4.4<br>5.4    | ie     | ege<br>LoV Lev       | $I_{OUT} = -50 \mu\text{A}$  |
| -50 µA<br>Vil. or Vil.                               | = TUOI V                             | 3.0<br>4.5<br>5.5      |                         | 2.56<br>3.86<br>4.86 |                              | 4,49<br>5.49 | 4.5<br>5.5        | 2.46<br>3.76<br>4.76 | lo     | High Lev             | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>- 12 mA<br>I <sub>OH</sub> - 24 mA<br>- 24 mA |
| V <sub>OL</sub> 9 -                                  | Maximum Low Level Output Voltage     | 3.0<br>4.5<br>5.5      | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1            | 00.00        | 5.5<br>4.5        | 0.1<br>0.1<br>0.1    | le     | /ed V <sub>rod</sub> | I <sub>OUT</sub> = 50 μA   |
| V <sub>IL</sub> or V <sub>IH</sub><br>24 mA<br>24 mA | NA. 101                              | 3.0<br>4.5<br>5.5      |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50         |              | 4.6               | 0.44<br>0.44<br>0.44 |        | ٧                    | $^*$ V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> 12 mA $^I$ OL 24 mA 24 mA                    |
| IIN HIV  | Maximum Input<br>Leakage Current     | 5.5                    |                         | ±0.1                 | ±1.0                         |              | 8.8               | ±1.0                 | EKS.   | μΑ                   | V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'ACQ Family Devices (Continued) The mumber of Acquired and Acquired to the Acquired to

|                  |   |                        | 74/                             | ACQ               | 54ACQ                            | 74ACQ                           | 48 9060<br>84 Arts | tocken seeds   |  |
|------------------|---|------------------------|---------------------------------|-------------------|----------------------------------|---------------------------------|--------------------|--|--|
| Symbol           | Parameter                                       | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C          |                   | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units              | Conditions   |  |
|                  |   |                        | Тур                             | ulloV tuqn        | Guaranteed Li                    | mits                            | al) inem           | DC Input Diade Cu  |  |
| IOLD             | †Minimum Dynamic                                | 5.5                    | oV) egat                        | Sutput Vol        | 50                               | 75                              | mA                 | V <sub>OLD</sub> = 1.65V Max   |  |
| IOHD             | Output Current                                  | 5.5                    | Lemper<br>ACTO                  | Sperating 712 ACC | -50 - 00V                        | ₩ V8.0 —75                      | mA                 | V <sub>OHD</sub> = 3.85V Min   |  |
| lcc st           | Maximum Quiescent<br>Supply Current             | 5.5                    | AGTO<br>nput Edg                | 8.0               | 160.0                            | 80.0                            | μΑ                 | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)                           |  |
| loz<br>sn\Vm.i   | Maximum TRI-STATE<br>Leakage Current            | 5.5                    | 190% to<br>190% to<br>190, 4:50 | ±0.5              | V8.0 + 00V<br>±10.0              | or V8.0−<br>±5.0                | μΑ                 | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 2 1.1.0                         | 1.5               | Am 08±                           | (a)                             | nenwo              | Figures 1, 2 (Notes 2, 3)  |  |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6                            | -1.2              | C to + 150°C                     | 10-                             | V e                | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage     | 5.0                    | 3.1                             | 3.5               | 175*0                            |                                 | (TV)               | (Notes 2, 4)   |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.9                             | 1.5               | 140°C<br>1 which damage          | noved seuley eacht are:         | V                  | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

## **DC Characteristics for 'ACTQ Family Devices**

| VI.0                              | = ruoV                       |                      |                   |                        | 744              | CTQ          | 54ACTQ                       | 6.1        | 74ACTQ                          | digirl mu           | Minim Minim  |
|-----------------------------------|------------------------------|----------------------|-------------------|------------------------|------------------|--------------|------------------------------|------------|---------------------------------|---------------------|--|
| Symbol                            | 30V 10                       | Parameter            |                   | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to +1 | 25°C       | T <sub>A</sub> = -40°C to +85°C | Units               | Conditions   |
| VIO                               | = TUOV =                     |                      | 1.35              |                        | Тур              | 1.35         | Guarante                     | ed Li      | mits                            | voll mu<br>relieses | Lustani TiA  |
| V <sub>IH</sub>                   | Minimum<br>Input Volt        | High Level<br>tage   | 1.65              | 4.5<br>5.5             | 1.5<br>1.5       | 2.0          | 2.0<br>2.0                   | 37.        | 2.0                             | V                   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>IL</sub>                   | Maximum<br>Input Volt        | Low Level            | 4,4               | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8<br>0.8                   | .49<br>.49 | 0.8                             | V                   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| Vон                               | Minimum<br>Output Vo         | High Level<br>oltage | 2.46              | 4.5<br>5.5             | 4.49<br>5.49     | 4.4          | 4.4<br>5.4                   |            | 4.4<br>5.4                      | V                   | $I_{OUT} = -50 \mu A$  |
|                                   | HO                           |                      |                   | 4.5                    |                  | 3.86         | 3.70                         |            | 3.76                            | V                   | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>-24 mA                |
| Vol                               |                              | Low Level            | 0.1<br>0.1<br>0.1 | 5.5<br>4.5<br>5.5      | 0.001            | 0.1<br>0.1   | 0.1<br>0.1                   | 001        | 0.1<br>0.1                      | V                   | $\frac{10H}{10UT} = 50 \mu\text{A}$  |
| IL of V <sub>IH</sub> 12 mA 24 mA | 70j<br>/ = NI <sub>A</sub> , | V                    | 0.44              | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                 |            | 0.44                            | v                   | $^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{24} \text{ mA}$ $^{24} \text{ mA}$ |
| I <sub>IN</sub>                   | Maximum                      | Input Leakage        | e Current         | 5.5                    |                  | ±0.1         | ±1.0                         |            | ±1.0                            | μΑ                  | $V_I = V_{CC}$ , GND   |
| loz                               | Maximum<br>Leakage           | TRI-STATE<br>Current | 0.7生              | 5.5                    |                  | ±0.5         | ±10.0                        |            | ±5.0                            | μА                  | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$                                  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. 1: I<sub>IN</sub> and I<sub>CC</sub> © 3.0V are guaranteed to be less than or equal to the response limit of the second of the secon

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>),

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

## DC Characteristics for 'ACTQ Family Devices (Continued)

|                  | 74ACQ                                    |                        | 74/              | ACTQ   | 54ACTQ                           | 74ACT                           | Q         |       |  |
|------------------|--|------------------------|------------------|--|----------------------------------|---------------------------------|-----------|-------|--|
| Symbol           | Parameter of                             | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C   | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C |           | Units | Conditions   |
|                  | Ct = 80 pF                               | NI 125                 | Тур              |  | Guaranteed L                     | mits                            |           |       |  |
| I <sub>CCT</sub> | Maximum 0.8                              | 5.5                    | 0.6              | Service of the servic | 1.6                              | 1.5                             | U 10 HE   | mA    | $V_{\rm I} = V_{\rm CC} - 2.1V$                      |
| IOLD             | †Minimum Dynamic                         | 5.5                    |                  |  | 50                               | . 75                            | Dut south | mA    | V <sub>OLD</sub> = 1.65V Max                         |
| IOHD             | Output Current                           | 5.5                    |                  |  | -50                              | 0.8 -75                         |           | mA    | V <sub>OHD</sub> = 3.85V Min                         |
| Icc              | Maximum Quiescent<br>Supply Current      | 5.5                    |                  | 8.0  | 160.0                            | 0.08                            | HDIH.     | μΑ    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |
| V <sub>OLP</sub> | Maximum High Level Output Noise          | 5.0                    | 1.1              | 1.5  |                                  |                                 |           | VE VE | Figures 1, 2 (Notes 2, 3)                            |
| V <sub>OLV</sub> | Maximum Low Level Output Noise           | 5.0                    | -0.6             | -1.2   | See Section 2 for \              | teristics                       | arac      | V     | Figures 1, 2<br>(Notes 2, 3)                         |
| V <sub>IHD</sub> | Maximum High Level Dynamic Input Voltage | 5.0                    | 1.9              | 2.2  | 070457                           | *coV                            |           | ٧     | (Notes 2, 4)   |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage  | 5.0                    | 1.2              | 0.8  | GL = 50 pF                       | (4)                             | 10        | ٧     | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     | 9-1  |                   |            | 74ACQ                |               | 54A   | CQ   | 74/  | ACQ O       |       | HTSO   |
|-------------------------------------|--|-------------------|------------|----------------------|---------------|---|------|--|-------------|-------|--------|
| Symbol                              | Parameter  | V <sub>CC</sub> * |            | A = +25<br>CL = 50 p | °C lauros art | T <sub>A</sub> = -<br>to + 1:<br>C <sub>L</sub> = 5 | 25°C | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ |             | Units | Fig.   |
|                                     |  |                   | Min        | Тур                  | Max           | Min   | Max  | Min  | Max         | (per  | OA.    |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | 3.3<br>5.0        | 2.5<br>1.5 | 8.5<br>5.5           | 11.5<br>7.5   |   |      | 2.5<br>1.5   | 12.0<br>8.0 | ns    | 2-3, 4 |
| t <sub>PLH</sub> , t <sub>PLH</sub> | Propagation Delay<br>LE to On                      | 3.3<br>5.0        | 2.5        | 2.5<br>6.0           | 13.0<br>8.5   | Voc'<br>(V)   |      | 2.5  | 13.5<br>9.0 | ns    | 2-3, 4 |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                                 | 3.3<br>5.0        | 2.5<br>1.5 | 8.5<br>6.0           | 13.0<br>8.5   |   | WO.  | 2.5  | 13.5<br>9.0 | ns    | 2-5, 6 |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                                | 3.3<br>5.0        | 1.0        | 9.0<br>6.5           | 14.5<br>9.5   | 0.6   | WC   | 1.0  | 15.0        | ns    | 2-5, 6 |
| toshl,<br>toshh                     | Output to Output Skew** Dn to On                   | 3.3<br>5.0        |            | 1.0                  | 1.5<br>1.0    | 8.0   |      | din, HiGH  | 1.5         | ns    | W/2    |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

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<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: ICC for 54ACTQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

Voltage Range 3.3 is 3.3V ±0.3V

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshi) or LOW to HIGH (toshi). Parameter guaranteed by design.

# AC Operating Requirements: See Section 2 for Waveforms 2004 and and analysis and 200

|                   | ACTO  |                   | 74   | ACQ        | 54ACC  | 2      | 74ACQ  |       |      |
|-------------------|---|-------------------|--|------------|--|--------|--|-------|------|
| Symbol            | Parameter A + of 5                              | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |        | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|                   |   | I Limite          | Тур  |            | Guarantee  | d Mini | mum  |       |      |
| ts                | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 3.3<br>5.0        | 0.1  | 3.0<br>3.0 | 6.0  | 8,6    | 3.0<br>3.0   | an ns | 2-7  |
| t <sub>H</sub>    | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 3.3<br>5.0        | 0  | 1.5<br>1.5 |  | 5.5    | 1.5<br>1.5   | ns ns | 2-7  |
| t <sub>W</sub> co | LE Pulse Width, HIGH                            | 3.3<br>5.0        | 2.0  | 4.0<br>4.0 | 8  | 8,8    | 4.0  | ns    | 2-3  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$ 0.5V. Voltage Range 3.3 is 3.3V  $\pm$ 0.3V.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                     | N. MRIOWELL   |                       |             |                      |      |   |                |  | PRODUCT. | 1177731  |        |
|-------------------------------------|---|-----------------------|-------------|----------------------|------|---|----------------|--|----------|----------|--------|
| 4)                                  | Caetol/II   |                       |             | 74ACTQ               |      | 54A   | СТО            | 74ACTQ   |          | monstal  | αнιV   |
| Symbol                              | Parameter   | V <sub>CC</sub> * (V) |             | A = +25<br>CL = 50 p |      | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |                | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |          | Units    | Fig.   |
|                                     |   |                       | Min         | Тур                  | Max  | Min   | Max            | Min  | Max      | asrayu j |        |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 5.0                   | 2.0         | 6.0                  | 8.0  | a time.   | ta bebaol n    | 2.0  | 8.5      | ns       | 2-3, 4 |
| t <sub>PLH</sub> , t <sub>PLH</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0                   | 2.5         | 7.0                  | 9.0  | inb ens atuq  | ni ataŭ "(n) ŝ | 2.5  | 9.5      | ns       | 2-3, 4 |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                                    | 5.0                   | 2.0         | 7.0                  | 9.0  | is stugni (1  | n) -pordoth    | 2.0  | 9.5      | ns       | 2-5, 6 |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time                                   | 5.0                   | 1.0         | 8.0                  | 10.0 |   |                | 1.0  | 10.5     | ns       | 2-5, 6 |
| toshl,                              | Output to Output Skew** Dn to On                      | 5.0                   | annors<br>a | 0.5                  | 1.0  | 1001  | POR TORK       | is isil.   | 1.0      | ns       | V354   |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V.

#### AC Operating Requirements: See Section 2 for Waveforms

| 4 .E-S e       | 2.5 12.0  |                   | 74ACTQ 54ACTQ                     |                 |  | 74ACTQ | H Propi  | gi JH9  |         |
|----------------|---|-------------------|-----------------------------------|-----------------|--|--------|--|---------|---------|
| Symbol         | 0.8   | V <sub>CC</sub> * | T <sub>A</sub> = C <sub>L</sub> = | + 25°C<br>50 pF | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |        | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units   | Fig.    |
|                |   |                   | Тур                               | 8.8             | Guaranteed Minimum   |        |  | q/uO Ho | ezu, ie |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0               | 0                                 | 3.0             | 1.6  | 5.0    | 3.0  | ns      | 2-7     |
| t <sub>H</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 5.0               | 0                                 | 1.5             | 1,0  | 5.0    | 1.5  | ns      | 2-7     |
| t <sub>W</sub> | LE Pulse Width, HIGH                            | 5.0               | 2.0                               | 4.0             |  | 5.0    | 4.0  | ns      | 2-3     |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V.

#### Capacitance

| Symbol          | Parameter                        | Тур | Units | Conditions             |
|-----------------|----------------------------------|-----|-------|------------------------|
| CIN             | Input Capacitance                | 4.5 | pF    | $V_{CC} = 5.0V$        |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40  | pF    | V <sub>CC</sub> = 5.0V |

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

# 54ACQ/74ACQ534•54ACTQ/74ACTQ534 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'ACQ/'ACTQ534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The 'ACQ/'ACTQ534 is the same as the 'ACQ/'ACTQ374 except that the outputs are inverted.

The 'ACQ/'ACTQ534 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

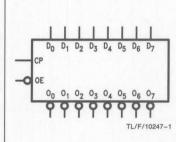
#### **Features**

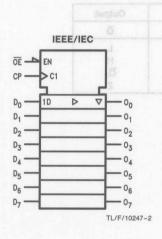
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Inverted output version of the 'ACQ/'ACTQ374
- Faster prop delays than the standard 'ACT534
- 4 kV minimum ESD immunity

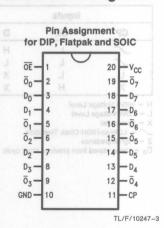
Ordering Code: See Section 8

**Logic Symbols** 

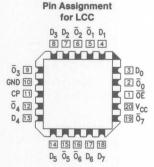
#### **Connection Diagrams**







| Pin Names  | Description   |
|--|---|
| $\begin{array}{c} D_0 - D_7 \\ \hline CP \\ \hline OE \\ \hline O_0 - \overline O_7 \end{array}$ | Data Inputs Clock Pulse Input TRI-STATE Output Enable Input Complementary TRI-STATE Outputs |



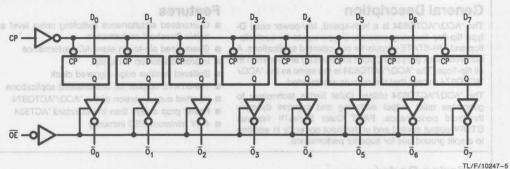
TL/F/10247-4

#### **Functional Description**

The 'ACQ/'ACTQ534 consists of eight D-type flip-flops with individual inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times

requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Function Table

|    | Inputs           |     | Output           |
|----|------------------|-----|------------------|
| CP | OE               | D   | ō                |
| _  | PROPERTY , THU T | Н   | L                |
| 1  | LIL              | ₩ L | н                |
| L  | L                | X   | $\overline{O}_0$ |
| X  | Н                | X   | Z                |

H = HIGH Voltage Level

L = LOW Voltage Level

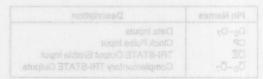
X = Immaterial

= LOW-to-HIGH Clock Transition

Z = High Impedance

 $\overline{O}_0$  = Value stored from previous clock cycle

NEW MENT



| Supply Voltage (V <sub>CC</sub> )                                      | -0.         | 5V to +7.0V      | 'ACTQ               |                       |          | 4.5V                            | to 5.5V            |
|--|-------------|------------------|---------------------|-----------------------|----------|---------------------------------|--------------------|
| DC Input Diode Current (I <sub>IK</sub> )                              |             | LI pastristatio  | Input Volta         | ige (V <sub>I</sub> ) |          | 0V                              | to V <sub>CC</sub> |
| $V_1 = -0.5V$  |             | -20 mA<br>+20 mA | Output Vo           | tage (V <sub>C</sub>  | ) 3.3    | Vo Minimum Dynamic              | to VCC             |
| $V_{I} = V_{CC} + 0.5V$  | -75         |                  | Operating           | Tempera               | ature (T | Output Carrent (A               |                    |
| DC Input Voltage (V <sub>I</sub> )                                     | -0.5V to    | $V_{CC} + 0.5V$  | 74ACQ/              | ACTQ                  |          | -40°C to                        | +85°C              |
| DC Output Diode Current (IOK)  |             | 160.0            | 54ACQ/              | ACTQ                  |          | -55°C to ∃                      | -125°C             |
| $V_{O} = -0.5V$<br>$V_{O} = V_{CC} + 0.5V$                             |             | -20 mA<br>+20 mA | Minimum I           |                       | ge Rate  | ΔV/Δt                           |                    |
| DC Output Voltage (V <sub>O</sub> )                                    | -0.5V to to | $V_{CC} + 0.5V$  |                     | 30% to                | 70% 0    | f V <sub>CC</sub> InsmuO egalas |                    |
| DC Output Source   |             |                  | V <sub>CC</sub> @3  | .0V, 4.5\             | /, 5.5V  | 125                             | mV/ns              |
| or Sink Current (I <sub>O</sub> ) DC V <sub>CC</sub> or Ground Current |             | ±50 mA           | Minimum I           |                       | ge Rate  | ΔV/Δt M Notio Otlog             |                    |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )                  |             | ±50 mA           |                     | 0.8V to               | 2.0V     |                                 |                    |
| Storage Temperature (T <sub>STG</sub> )                                | -65°        | C to +150°C      | V <sub>CC</sub> @ 4 | .5V, 5.5\             | / 0.0    | JoV olman 125                   | mV/ns              |
| DC Latch-Up Source or<br>Sink Current                                  |             | ±300 mA          |                     |                       |          |                                 |                    |
| Junction Temperature (T <sub>J</sub> ) CDIP                            |             | 175°C            |                     |                       |          |                                 |                    |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

#### DC Characteristics for 'ACQ Family Devices

|                        |  |                          | 74/                     | ACQ                  | 54ACQ                             | ma                              | 74ACQ                     | tainat                        | DC Charac   |  |
|------------------------|--|--------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|---------------------------|-------------------------------|---|--|
| Symbol                 | Parameter                                      | V <sub>CC</sub><br>(V)   | T <sub>A</sub> =        | + 25°C               | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C |                           | Units                         | Conditions  |  |
|                        | one Units Cons                                 | = 47                     | Тур                     | nasar                | Guaranteed Li                     | mits                            | 20V                       | release                       | Symbol Pa   |  |
| V <sub>IH</sub>        | Minimum High Level<br>Input Voltage            |                          |                         | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 9y7<br>2.7                      | 2.1<br>3.15<br>3.85       | V<br>pul rigil h              | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| VIH VILO               | Maximum Low Level Input Voltage                | 3.0<br>4.5<br>5.5        | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 1.5                             | 0.9<br>1.35<br>1.65       | ed v d n                      | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| HI OF VIH              | Minimum High Level<br>Output Voltage           | 3.0<br>4.5<br>5.5        | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 5.48                            | 2.9<br>4.4<br>5.4         | e V llo                       | $I_{OUT} = -50 \mu\text{A}$   |  |
|                        | HOI V  | 3.0<br>4.5               |                         | 2.56<br>3.86         | 2.4<br>3.7                        | 100.0                           | 2.46<br>3.76              | ed vyd n                      | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $I_{OH}$ $-24 \text{ mA}$                |  |
| V <sub>OL</sub> NO INV | Maximum Low Level<br>Output Voltage            | 5.5<br>3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 4.7<br>0.1<br>0.1<br>0.1          | 100.0                           | 4.76<br>0.1<br>0.1<br>0.1 | V                             | $-24 \text{ mA}$ $I_{OUT} = 50  \mu\text{A}$  |  |
| ыV.                    | $pA$ $V_1 = V_0$ $pA$ $V_1 = V_0$ $pA$ $Q = V$ | 3.0<br>4.5<br>5.5        |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              |                                 | 0.44<br>0.44<br>0.44      | Ourrent<br>Ourrent<br>Ourrent | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>I</sub><br>12 mA<br>I <sub>OL</sub> 24 mA<br>24 mA |  |
| IIN                    | Maximum Input<br>Leakage Current               | 5.5                      |                         | ±0.1                 | ±1.0                              | 8.0                             | ±1.0                      | μА                            | V <sub>I</sub> = V <sub>CC</sub> , GND<br>(Note 1)  |  |

\*All outputs loaded; thresholds on input associated with output under test. †Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'ACQ Family Devices (Continued)

|                  |   |                        | 74                                    | ACQ        | 54ACQ                             | 74ACQ               | de ace<br>the his | it murery a erosp  |
|------------------|---|------------------------|---------------------------------------|------------|-----------------------------------|---------------------|-------------------|--|
| Symbol           |   | V <sub>CC</sub><br>(V) | T <sub>A</sub> =                      | + 25°C     | T <sub>A</sub> = -55°C to + 125°C |                     | Units             | Conditions   |
|                  |   |                        | Тур                                   | stioV tua  | Guaranteed Li                     | mits                | nent (lg          | DC Input Diode Cu  |
| I <sub>OLD</sub> | †Minimum Dynamic                                | 5.5                    | loV) aga                              | toV rugtor | 50                                | 75                  | mA                | V <sub>OLD</sub> = 1.65V Max   |
| IOHD             | Output Current                                  | 5.5                    | steqme?                               | perating   | -50                               | -75                 | mA                | V <sub>OHD</sub> = 3.85V Min   |
| Icc              | Maximum Quiescent<br>Supply Current             | 5.5                    | 010/                                  | 8.0        | 160.0                             | 80.0 610            | μА                | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)                           |
| loz              | Maximum TRI-STATE<br>Leakage Current            | 5.5                    | pur cog<br>vices<br>30% to<br>ov 4.6V | ±0.5       | ±10.0                             | ±5.0<br>of at V8.0— | μA<br>(oV)        | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |
| V <sub>OLP</sub> | Quiet Output Maximum<br>Dynamic V <sub>OL</sub> | 5.0                    | 90 <b>1,1</b> 09                      | 1.5        | ±50 mA                            |                     | o) v<br>Curtent   | Figures 1, 2<br>(Note 2, 3)  |
| V <sub>OLV</sub> | Quiet Output Minimum<br>Dynamic V <sub>OL</sub> | 5.0                    | -0.6                                  | -1.2       | ± 50 mA<br>210 + 150°C            |                     | nol V or          | Figures 1, 2<br>(Notes 2, 3)   |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage     | 5.0                    | 3.1                                   | 3.5        | £300 mA                           |                     | V                 | (Notes 2, 4)   |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.9                                   | 1.5        | 178°C                             |                     | (,T) en           | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>. I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## **DC Characteristics for 'ACTQ Family Devices**

| anobi           | 15°C Units Cond                      | A 1                    | 74A              | CTQ          | 54ACTQ                           | 74ACTQ                        |       | netema    | 169                              | Symbol   |
|-----------------|--------------------------------------|------------------------|------------------|--------------|----------------------------------|-------------------------------|-------|-----------|----------------------------------|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C       | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +89 | 5°C   | Units     | Cond                             | ditions  |
| V1.0            | = ruoV                               | 2.1<br>ar.p            | Тур              | 3.5          | Guaranteed Li                    | mits                          | 18VI  | I rigit i | numinilyi<br>Ny fivont           |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 4.5<br>5.5             | 1.5<br>1.5       | 2.0          | 2.0<br>2.0                       | 2.0                           | -     | V         | V <sub>OUT</sub> =               |  |
| VILVE.0         | Maximum Low Level<br>Input Voltage   | 4.5<br>5.5             | 1.5<br>1.5       | 0.8          | 0.8                              | 0.8                           |       | Vell      | V <sub>OUT</sub> =               |  |
| VOH             | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49     | 4.4<br>5.4   | 4.4<br>5.4                       | ee s 4.4<br>5.4               | lave  | V         | I <sub>OUT</sub> =               | -50 μΑ   |
| HIV TO JIH      | $= NI \wedge_x$                      | 4.5<br>5.5             |                  | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                  |       | ٧         | *V <sub>IN</sub> =               | V <sub>IL</sub> or V <sub>IH</sub><br>-24 mA<br>-24 mA |
| Vol. 3 -        | Maximum Low Level<br>Output Voltage  | 4.5<br>5.5             | 0.001<br>0.001   | 0.1          | 0.1<br>0.1                       | 0.1<br>0.1                    |       | ٧         | I <sub>OUT</sub> =               | 50 μΑ  |
| Aay 08          |                                      | 4.5<br>5.5             |                  | 0.36<br>0.36 | 0.50<br>0.50                     | 0.44                          | fevs. | m Low L   | *V <sub>IN</sub> =               | V <sub>IL</sub> or V <sub>IH</sub><br>24 mA<br>24 mA   |
| INV 10 JIV      | Maximum Input<br>Leakage Current     | 5.5                    |                  | ±0.1         | ±1.0                             | ± 1.0                         |       | μΑ        | $V_I = V_C$                      | C, GND   |
| loz sa          | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                  | ±0.5         | ± 10.0                           | ±5.0                          |       | μΑ        | $V_{I} = V_{IL}$ $V_{O} = V_{I}$ | , V <sub>IH</sub>                                      |
| ICCT 10 .       | Maximum<br>I <sub>CC</sub> /Input    | 5.5                    | 0.6              | 0.1          | ± 1.6 <sub>1.0 ±</sub>           | 1,5                           |       | mA        | $V_I = V_C$                      | C - 2.1V   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  | PAACQ                                    |                        | 74                      | ACTQ | 54ACTQ                             |            | 74ACTQ                           |       |  |  |
|------------------|--|------------------------|-------------------------|------|------------------------------------|------------|----------------------------------|-------|--|--|
| Symbol           | Parameter of                             | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C  |      | T <sub>A</sub> = -55°C to +125°C   | -40        | T <sub>A</sub> = 0°C to +85°C    | Units | Conditions   |  |
|                  | C <sub>L</sub> = 50 pF                   | mically (              | Тур                     | 1000 | Guaranteed Li                      | imits      |                                  |       |  |  |
| IOLD             | †Minimum Dynamic                         | 5.5                    | 100 100 100 100 100 100 |      | 50                                 | 8.8        | 75                               | mA    | V <sub>OLD</sub> = 1.65V Max                         |  |
| IOHD             | Output Current                           | 5.5                    |                         | -    | -50                                | 6.0        | -75                              | mA    | V <sub>OHD</sub> = 3.85V Min                         |  |
| Iccs             | Maximum Quiescent<br>Supply Current      | 5.5                    |                         | 8.0  | 160.0                              | 3.8<br>5.0 | 80.0                             | μА    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |  |
| VOLP             | Maximum High Level Output Noise          | 5.0                    | 1.1                     | 1.5  | 4 S<br>4 S                         | 9.9        |                                  | V     | Figures 1, 2<br>(Note 2, 3)                          |  |
| V <sub>OLV</sub> | Maximum Low Level<br>Output Noise        | 5.0                    | -0.6                    | -1.2 | V ± 0.3V<br>Ž. Sae Section 2 tor V |            | , volege mage 5<br>arre crearies | ٧     | Figures 1, 2<br>(Notes 2, 3)                         |  |
| V <sub>IHD</sub> | Minimum High Level Dynamic Input Voltage | 5.0                    | 01.9                    | 2.2  | TAACTO                             |            |                                  | ٧     | (Notes 2, 4)   |  |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage  | 5.0                    | 1.2                     | 0.8  | TA = +28°C<br>CL = 50 pF           |            | Vec" (V)                         | ٧     | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                     | a 0.r  |                   |            | 74ACQ               | 0.5         | 54A   | CQ     | 744  | CQ           | Ske   | HTISO       |
|-------------------------------------|--|-------------------|------------|---------------------|-------------|---|--------|--|--------------|-------|-------------|
| SELVE GENTON: 1 US PERCEICERELL.    | Parameter  | V <sub>CC</sub> * |            | = + 25°<br>L = 50 p | 1320        | $T_A = -55^{\circ}C$<br>to $+125^{\circ}C$<br>$C_L = 50 pF$ |        | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ |              | Units | Fig.<br>No. |
|                                     |  |                   | Min        | Тур                 | Max         | Min   | Max    | Min  | Max          |       | 275.25      |
| f <sub>max</sub>                    | Maximum Clock<br>Frequency                                 | 3.3<br>5.0        | 75<br>90   | DIEVENT I           | TOART       | 5 905 183   | PERMIT | 70<br>85   | 1 (Cases)    | MHz   | 107.0%      |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay CP to $\overline{Q}_n$                   | 3.3<br>5.0        | 3.0        | 9.5<br>6.5          | 13.0<br>8.5 | *ee   | A      | 3.0<br>2.0   | 13.5<br>9.0  | ns    | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time   | 3.3<br>5.0        | 3.0<br>2.0 | 9.5<br>6.5          | 13.0<br>8.5 |   |        | 3.0<br>2.0   | 13.5<br>9.0  | ns    | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time  | 3.3<br>5.0        | 1.0<br>1.0 | 9.5<br>8.0          | 14.5<br>9.5 | 5.0   | VVC    | 1.0  | 15.0<br>10.0 | ns    | 2-5, 6      |
| toshl,<br>toslh                     | Output to Output<br>Skew** CP to $\overline{\mathbb{Q}}_n$ | 3.3<br>5.0        |            | 1.0<br>0.5          | 1.5         | 0.8   | W      | OJ to HOII   | 1.5          | ns    | nî          |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$  0.5V, Voltage Range 3.3 is 3.3V  $\pm$  0.3V.

 Capacitance
 Typ
 Units
 Conditions

 Symbol
 Parameter
 Typ
 Units
 Conditions

 Cpu
 Input Capacitance
 4.5
 pF
 Voc = 6.0V

 Cpp
 Power Dissipation
 40.0
 pF
 Vcc = 6.0V

 Capacitance
 Capacitance
 40.0
 pF
 Vcc = 6.0V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: Icc for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of Data Inputs defined as (n). n-1 Data Inputs are driven 0V to 3V. One Data Input @ VIN = GND.

Note 4: Max number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

# AC Operating Requirements: See Section 2 for Waveforms

|                  | MACTO  |                   | 744  | CQ         | 54ACQ  |      | 74ACQ  |       |      |
|------------------|--|-------------------|--|------------|--|------|--|-------|------|
| Symbol Parameter | Parameter                                      | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|                  |  |                   | Тур  |            | Guaranteed   | Mini | mum  |       |      |
| ts Vea.c         | Setup Time, HIGH or LOW<br>Dn to CP            | 3.3<br>5.0        | 1.0  | 3.0<br>3.0 |  | 5.5  | 3.0<br>3.0   | ns ns | 2-7  |
| th 50            | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP | 3.3<br>5.0        | 0  | 1.5<br>1.5 |  | 8.5  | 1.5 no m   | ns    | 2-7  |
| t <sub>w</sub>   | CP Pulse Width<br>HIGH or LOW                  | 3.3<br>3.3        | 2 2  | 4.0<br>4.0 | 1.1  | 5.0  | 4.0  | ns    | 2-3  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$ 0.5V, Voltage Range 3.3 is 3.3V  $\pm$  0.3V

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  | serom) V                            |                   |       | 74ACTQ               |      | 54ACTQ   | 74   | CTQ                          | District Courses | GHIA              |
|------------------|-------------------------------------|-------------------|-------|----------------------|------|--|------|------------------------------|------------------|-------------------|
| Symbol           | Parameter                           | V <sub>CC</sub> * |       | A = +25<br>CL = 50 p |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | to - | -40°C<br>-85°C<br>-50 pF     | Units            | Fig.<br>No.       |
|                  |                                     | +                 | Min   | Тур                  | Max  | Min Max  | Min  | Max                          | obsol atop       | NIO IIA*          |
| f <sub>max</sub> | Maximum Clock<br>Frequency          | 5.0               | 85    |                      |      | londed at a time.<br>to 74ACTO @ 281C.                         | 80   | enion 2:0 ms,<br>ACTO @ 251C | MHz              | nixaMit<br>I stoM |
| tphL, tpLH       | Propagation Delay<br>CP to Qn       | 5.0               | 2.0   | 7.0                  | 9.0  | es (n), n - 1 Data Inputs i                                    | 2.0  | 9.5                          | ns               | 2-3, 4            |
| tPZL, tPZH       | Output Enable Time                  | 5.0               | 2.0   | 7.0                  | 9.0  |  | 2.0  | 9.5                          | ns               | 2-5, 6            |
| tpHZ, tpLZ       | Output Disable Time                 | 5.0               | 1.0   | 8.0                  | 10.0 | and mentiodyna   | 1.0  | 10.5                         | ns               | 2-5, 6            |
| toshl,<br>toslh  | Output to Output<br>Skew** CP to Qn | 5.0               | SAACO | 0.5                  | 1.0  | N I I  |      | 1.0                          | ns               |                   |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

## AC Operating Requirements: See Section 2 for Waveforms

|        | 68   |                   | 74A0   | CTQ    | 54AC   | TQ         | 74ACTQ   | Freq  |             |
|--------|--|-------------------|--|--------|--|------------|--|-------|-------------|
| Symbol | Parameter  a.21 0.6 0.0 0.8                    | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |        | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig.<br>No. |
| 2-5, 6 |  |                   | Тур  | 6,5, - | Guarante   | eed Mini   | mum  |       | 7 04        |
| ts     | Setup Time, HIGH or LOW<br>Dn to CP            | 5.0               | 1.0  | 3.0    | 1.0  | 3.3<br>5.0 | smiT eldesiG h<br>3.0  | ns T  | 2-7         |
| th     | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0               | 1.6 0  | 1.5    |  | 8.8<br>5.0 | 1.5 90 **  | ns    | 2-7         |
| tw     | CP Pulse Width<br>HIGH or LOW                  | 5.0               | 2.0  | 4.0    | is 3.3V ± 03   | ELE agmini | 4.0  | ns    | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

| Symbol          | Parameter                        | Тур  | Units | Conditions             |
|-----------------|----------------------------------|------|-------|------------------------|
| CIN             | Input Capacitance                | 4.5  | pF    | V <sub>CC</sub> = 5.0V |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40.0 | pF    | V <sub>CC</sub> = 5.0V |

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.



# 54ACQ/74ACQ543 • 54ACTQ/74ACTQ543 **Quiet Series Octal Registered Transceiver with TRI-STATE® Outputs**

#### **General Description**

The ACQ/ACTQ543 is a non-inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

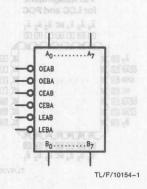
The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### Features

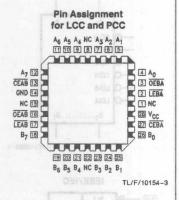
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- 8-bit octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity

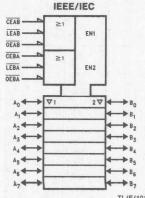
#### **Logic Symbols**

#### **Connection Diagrams**









TL/F/10154-4

#### ADVANCE INFORMATION



# 54ACQ/74ACQ544 • 54ACTQ/74ACTQ544 Quiet Series Octal Registered Transceiver with TRI-STATE® Outputs

#### **General Description**

The ACQ/ACTQ544 is an inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow. The '544 inverts data in both directions.

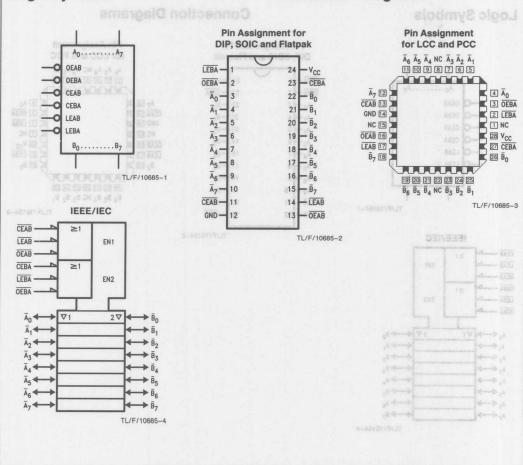
The ACQ/ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- 8-bit inverting octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity
- 300 mil slim PDIP/SOIC

#### **Logic Symbols**

#### **Connection Diagrams**



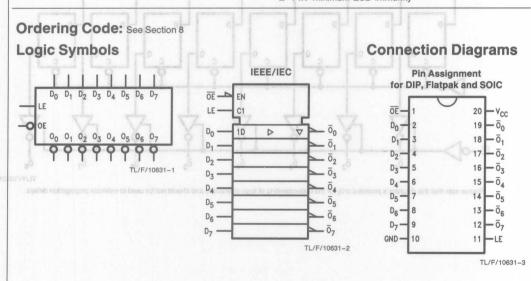
# 54ACQ/74ACQ563 • 54ACTQ/74ACTQ563 Quiet Series Octal Latch with TRI-STATE® Outputs

#### **General Description**

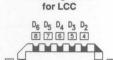
The 'ACQ/'ACTQ563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs. The 'ACQ/'ACTQ563 is functionally identical to the 'ACQ/'ACTQ573, but with inverted outputs. The ACQ/ACTQ utilizes NSC Quiet Series technology to quarantee quiet output switching and improved dynamic threshold performance. FACT Quiet SeriesTM features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

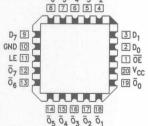
- Guaranteed simultaneous switching noise level and dynamic threshold perforfmance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard ACT563
- Functionally identical to the ACQ/ACTQ573 but with inverted outputs
- 4 kV minimum ESD immunity



| Pin Names                         | Description                   |  |  |  |  |  |
|-----------------------------------|-------------------------------|--|--|--|--|--|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                   |  |  |  |  |  |
| LE                                | Latch Enable Input            |  |  |  |  |  |
| ŌĒ                                | TRI-STATE Output Enable Input |  |  |  |  |  |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Latch Outputs       |  |  |  |  |  |



Pin Assignment



TL/F/10631-4

latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the buffers are in the bi-state mode. When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

|   | VL      | -       | U | u      | 0      |             |
|---|---------|---------|---|--------|--------|-------------|
|   | Н       | X       | X | X      | Z      | High-Z      |
| 1 | Н       | Н       | L | H      | Z      | High-Z      |
|   | H       | oH I    | H | and a  | Z      | High-Z      |
|   | Н       | L       | X | NC     | Z      | Latched     |
|   | L       | Н       | L | Н      | Н      | Transparent |
|   | L       | Н       | Н | notigi | 1]0880 | Transparent |
|   | sivLrio | isi Lub | X | NC NC  | NC NC  | Latched     |
|   |         |         |   |        |        |             |

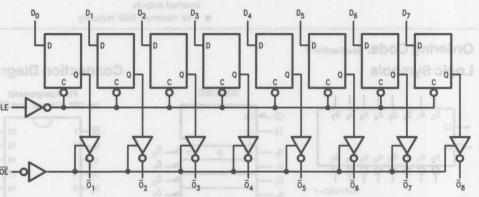
H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial W STROTTO A LOCAL Sett of Isolinesia

Z = High Impedance DO ORM assists OTOALOOA SAT

NC = No Change

#### **Logic Diagram**



TL/F/10631-5
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| Description |  |
|-------------|--|
|             |  |
|             |  |
|             |  |
|             |  |

#### Recommended Operating Absolute Maximum Rating (Note 1) If Military/Aerospace specified devices are required, **Conditions** please contact the National Semiconductor Sales Supply Voltage (V<sub>CC</sub>) Office/Distributors for availability and specifications. 'ACQ 2.0V to 6.0V Supply Voltage (V<sub>CC</sub>) -0.5V to +7.0V 'ACTQ 4.5V to 5.5V DC Input Diode Current (IIK) Input Voltage (V<sub>I</sub>) OV to Vcc $V_1 = -0.5V$ Output Voltage (Vo) OV to V<sub>CC</sub> $V_I = V_{CC} + 0.5V$ +20 mA Operating Temperature (TA) DC Input Voltage (V<sub>I</sub>) -0.5V to V<sub>CC</sub> + 0.5V 74ACQ/ACTQ -40°C to +85°C -55°C to +125°C DC Output Diode Current (IOK) 54ACQ/ACTQ $V_0 = -0.5V$ -20 mA Minimum Input Edge Rate ΔV/Δt $V_O = V_{CC} + 0.5V$ +20 mA 'ACQ Devices DC Output Voltage (Vo) -0.5V to V<sub>CC</sub> + 0.5V VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.0V, 4.5V, 5.5V DC Output Source or Sink Current (IO) ±50 mA Minimum Input Edge Rate ΔV/Δt DC Vcc or Ground Current 'ACTQ Devices $\pm$ 50 mA VIN from 0.8V to 2.0V per Output Pin (ICC or IGND) V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns Storage Temperature (TSTG) -65°C to +150°C DC Latchup Source or Sink Current ±300 mA Junction Temperature (T<sub>.1</sub>) CDIP 175°C PDIP 140°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recom-

#### **DC Characteristics for 'ACQ Family Devices**

mend operation of FACTTM circuits outside databook specifications.

|                 |  |                     | 74/                     | ACQ                  | 54ACQ                             | 74ACQ                           | 0.07 ale g | Service of any one page of  |  |
|-----------------|--|---------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|------------|---|--|
| Symbol          | Parameter                                  | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units      | Conditions  |  |
| Dipriestrat     | 5V to breedfold (V <sub>ILD</sub> ), 0V to | RINCORNE            | Тур                     | ugm (SDA)            | Guaranteed Li                     | mits                            | NeO 16 166 | Voto 4: Maximum nur<br>Vatoù 1 = 1 MHz.   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage        | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | ٧          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage         | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | V          | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage       | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | v          | $I_{OUT} = -50 \mu$ A   |  |
|                 |  | 3.0<br>4.5<br>5.5   |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | V          | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>I</sub><br>-12 m<br>I <sub>OH</sub> -24 m<br>-24 m |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage        | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | V          | $I_{OUT} = 50 \mu A$  |  |
|                 |  | 3.0<br>4.5<br>5.5   |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              | 0.44<br>0.44<br>0.44            | v          | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>I</sub> 12 m 1 <sub>OL</sub> 24 m 24 m             |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'ACQ Family Devices (Continued)

|                  |   | 11.0                   | 74                             | ACQ        | 54ACQ                            | 74ACQ  | ga soss                           | if Military/Aeros  |
|------------------|---|------------------------|--------------------------------|------------|----------------------------------|--|-----------------------------------|--|
| Symbol           | Parameter                                       | V <sub>CC</sub><br>(V) | T <sub>A</sub> =               | + 25°C     | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C                          | Units                             | Conditions   |
| 10 Vcc           | 70  |                        | Тур                            | stloV fign | Guaranteed Li                    | mits   | nent (h                           | DC Input Diode Co  |
| IMO A ot .       | Maximum Input<br>Leakage Current                | 5.5                    | oV) egal<br>Tempera            | ±0.1       | ±1.0                             | ±1.0   | μА                                | V <sub>I</sub> = V <sub>CC</sub> , GND (Note 2)                                |
| IOLD             | †Minimum Dynamic                                | 5.5                    | ACTO -                         | YANGON     | 50                               | 75 (sm)  | mA                                | V <sub>OLD</sub> = 1.65V Max   |
| IOHD             | Output Current                                  | 5.5                    | iput Edg                       | I muminit  | -50                              | -75  | mA                                | V <sub>OHD</sub> = 3.85V Min   |
| lcc              | Maximum Quiescent<br>Supply Current             | 5.5                    | 30% to                         | 8.0        | 160.0 + aoV                      | of V6.0-80.0   | μΑ                                | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)                           |
| loz              | Maximum TRI-STATE Leakage Current               | 5.5                    | sput Edg<br>levices<br>0,8V to |            | Am 08 ± ± 10.0<br>Am 08 ±        | ±5.0   | ο)<br>πε <b>μΑ</b> ο<br>εο οι Ιοι | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |
| V <sub>OLP</sub> | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1.1                            | 1.5        | 2 to + 150°C                     | 198- (g  | V ST                              | Figures 1, 2<br>(Notes 2, 3)   |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6                           | -1.2       | 178°C                            |  | (LTVeru                           | Figures 1, 2<br>(Notes 2, 3)   |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage     | 5.0                    | 3.1                            | 3.5        | 146°C<br>I which dentage         | incyad sautav saudi eta s                                | grida V mior                      | (Notes 2, 4)   |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.9                            | 1.5        | a power supply, one not recom-   | m design is religible over a<br>ding variables. National | PATRICIA SOLICE                   | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @5.5V V<sub>CC</sub>.

I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Maximum number of Data Inputs (n) switching. (n-1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

| S.B. | 2.75 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.75 | 3.86 | 3.75 | 3.86 | 3.75 | 3.86 | 3.75 | 3.86 | 3.75 | 3.85 | 3.85 | 3.75 | 3.85 | 3.85 | 3.75 | 3.85 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.75 | 3.85 | 3.85 | 3.75 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 | 3.85 |

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  |   | 74ACQ                              | DAN                    | 74A0                              | CTQ          | 54ACTQ                       |            | 74ACTQ                          |         |   |  |
|------------------|---|------------------------------------|------------------------|-----------------------------------|--------------|------------------------------|------------|---------------------------------|---------|---|--|
| Symbol           | alinU                                   | Parameter                          | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C            |              | T <sub>A</sub> = -55°C to +1 | 25°C       | T <sub>A</sub> = -40°C to +85°C | Units   | Conditions  |  |
|                  |   | pF C <sub>L</sub> = 80 pF          | DB =                   | Тур                               |              | Guarant                      | eed L      | imits.                          |         |   |  |
| V <sub>IH</sub>  |   | um High Level<br>/oltage           | 4.5<br>5.5             | 1.5<br>1.5                        | 2.0          | 2.0<br>2.0                   |            | 2.0<br>2.0 (Sie                 | V       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>IL</sub>  |   | um Low Level<br>/oltage            | 4.5<br>5.5             | 1.5<br>1.5                        | 0.8          | 0.8                          |            | 0.8<br>0.8 (ale)                | V       | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| V <sub>OH</sub>  |   | um High Level<br>t Voltage         | 4.5<br>5.5             | 4.49<br>5.49                      | 4.4<br>5.4   | 4.4<br>5.4                   |            | 4.4<br>5.4                      | E V bla | $I_{OUT} = -50 \mu\text{A}$   |  |
|                  | en                                      | 1.0 15.0<br>1.0 10.0               | 4.5<br>5.5             |                                   | 3.86<br>4.86 | 3.70<br>4.70                 |            | 3.76<br>4.76                    | V       | $^*V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |  |
| V <sub>OL</sub>  | 100000000000000000000000000000000000000 | um Low Level<br>t Voltage          | 4.5<br>5.5             | 0.001<br>0.001                    | 0.1<br>0.1   | 0.1<br>0.1                   |            | 0.1<br>0.1                      | ni di   | $I_{OUT} = 50 \mu A$  |  |
|                  |   |                                    | 4.5<br>5.5             | ryna sot yali<br>Hilli to Hilli ( | 0.36         | 0.50                         | wied s     | 0.44<br>0.44                    | oe vs.  | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{IOL}$ $^{24 \text{ mA}}$ $^{24 \text{ mA}}$         |  |
| I <sub>IN</sub>  | Maxim                                   | um Input Leakage Current           | 5.5                    | amtote                            | ±0.1         | ±1.0                         | :83        | ±1.0                            | μΑ      | $V_I = V_{CC}$ , GND  |  |
| loz              |   | um TRI-STATE<br>ge Current         | 5.5                    |                                   | ±0.5         | ±10.0                        |            | ±5.0                            | μА      | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |
| ICCT             | Maxim                                   | um I <sub>CC</sub> /Input          | 5.5                    | 0.6                               | 3,53         | = AT 1.6                     | ,00/       | 1.5                             | mA      | $V_I = V_{CC} - 2.1V$   |  |
| I <sub>OLD</sub> | †Minin                                  | num Dynamic                        | 5.5                    | 20                                | 40.0         | 50                           | (8)        | 75                              | mA      | V <sub>OLD</sub> = 1.65V Max  |  |
| I <sub>OHD</sub> | Output                                  | t Current muminist b               | 5.5                    | Guan                              |              | 47-50                        |            | -75                             | mA      | V <sub>OHD</sub> = 3.85V Min  |  |
| Icc              | 2011                                    | um Quiescent<br>Current            | 5.5                    |                                   | 8.0          | 160.0                        | 8.8<br>6.0 | 80.0                            | μΑ      | V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)   |  |
| V <sub>OLP</sub> | V                                       | um High Level<br>Noise             | 5.0                    | 1.1                               | 1.5          | 0                            | 3,3        | MOLI or LOW                     | V       | Figures 1, 2<br>(Notes 2, 3)  |  |
| V <sub>OLV</sub> | Maxim<br>Output                         | um Low Level<br>Noise              | 5.0                    | -0.6                              | -1.2         | 2.0<br>2.0                   | 8.8        | RDIN, HIGH                      | V       | Figures 1, 2<br>(Note 2, 3)   |  |
| V <sub>IHD</sub> |   | um High Level<br>nic Input Voltage | 5.0                    | 1.9                               | 2.2          |                              |            | AS:                             | VO. B   | (Notes 2, 4)  |  |
| V <sub>ILD</sub> |   | um Low Level<br>nic Input Voltage  | 5.0                    | 1.2                               | 0.8          | See Section 1                | :00)       | naracterist                     | ٧       | (Notes 2, 4)  |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching; 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

#### AC Electrical Characteristics: See Section 2 for Waveforms Total and additional add

|                                     | METQ                             | 7                 |            | 74ACQ            |             | 54   | ACQ                        | 74         | ACQ                    |         | Fig.   |
|-------------------------------------|----------------------------------|-------------------|------------|------------------|-------------|------|----------------------------|------------|------------------------|---------|--------|
| Symbol                              | Parameter                        | V <sub>CC</sub> * |            | = + 25<br>= 50 p |             | to + | -55°C<br>-125°C<br>= 50 pF | to +       | -40°C<br>85°C<br>50 pF | Units   |        |
|                                     | V                                | GAIITING          | Min        | Тур              | Max         | Min  | Max                        | Min        | Max                    | min(8.8 |        |
| tphi, tpih                          | Propagation Delay Dn to On       | 3.3<br>5.0        | 2.5<br>1.5 | 8.5<br>5.5       | 11.5<br>7.5 | 1.6  | 5.6                        | 2.5<br>1.5 | 12.0<br>8.0            | ns      | 2-3, 4 |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation Delay<br>LE to On    | 3.3<br>5.0        | 2.5        | 8.5<br>6.0       | 13.0<br>8.5 |      | 8.8                        | 2.5<br>2.0 | 13.5<br>9.0            | ns      | 2-3, 4 |
| tpzL, tpzH                          | Output Enable Time               | 3.3<br>5.0        | 2.5<br>1.5 | 8.5<br>6.0       | 13.0<br>8.5 | 5,48 | 5.5                        | 2.5<br>1.5 | 13.5<br>9.0            | ns      | 2-5, 6 |
| t <sub>PHZ</sub> , t <sub>PLZ</sub> | Output Disable Time              | 3.3<br>5.0        | 1.0        | 9.0<br>6.5       | 14.5<br>9.5 |      | 4.5                        | 1.0<br>1.0 | 15.0<br>10.0           | ns      | 2-5, 6 |
| toshl,                              | Output to Output Skew** Dn to On | 3.3<br>5.0        | 1.0        | 1.0<br>0.5       | 1.5         | 00.0 | 4,5                        | lava       | 1.5<br>1.0             | ns      | JO,    |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V Voltage Range 3.3 is 3.3V ±0.3V

# AC Operating Requirements: See Section 2 for Waveforms

| C VIH               |  |                   | 74         | ACQ               | 54ACQ  | 74ACQ         | numpasivi I | 20          |
|---------------------|--|-------------------|------------|-------------------|--|---------------|-------------|-------------|
| Symbol              | Parameter Am                                   | V <sub>CC</sub> * |            | + 25°C<br>= 50 pF | T <sub>A</sub> = -5!<br>to + 125°<br>C <sub>L</sub> = 50 | C to +85°C    | Units       | Fig.<br>No. |
| = 3.85V Min         |  |                   | е Тур      |                   | Guaranteed   | Minimum Inemu | Output O    | GHO         |
| ts oo\              | Setup Time, HIGH or LOW                        | 3.3<br>5.0        | 0000       | 3.0<br>3.0        | a.a  | 3.0 aniu 0 1  | ns          | 2-7         |
| t <sub>H</sub> S, t | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE | 3.3<br>5.0        | 0          | 1.5<br>1.5        | 5.0 1.1  | 1.5 mil-1     | ns V        | 2-7         |
| tw s.r              | LE Pulse Width, HIGH                           | 3.3<br>5.0        | 2.0<br>2.0 | 4.0               | 8.0 - 0.8  | 4.0<br>4.0    | ns          | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$ 0.5V Voltage Range 3.3V is 3.3  $\pm$ 0.3V

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |  |                   |     | 74ACTQ                           |      | 54A  | СТО          | 74A  | СТО  | Dynami     |             |
|-------------------------------------|--|-------------------|-----|----------------------------------|------|--|--------------|--|------|------------|-------------|
| Symbol                              | Parameter  | V <sub>CC</sub> * |     | A = +25<br>C <sub>L</sub> = 50 p |      | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF |              | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units      | Fig.<br>No. |
|                                     |  |                   | Min | Тур                              | Max  | Min  | Max          | Min  | Max  | no Jarow n | etoM        |
| t <sub>PHL</sub> , t <sub>PLH</sub> | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | 5.0               | 2.0 | 6.0                              | 8.0  | ofiwe attignt  | (h-n) gnirto | 2.0  | 8.5  | ns         | 2-3, 4      |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation Delay<br>LE to On                      | 5.0               | 2.5 | 7.0                              | 9.0  |  |              | 2.5  | 9.5  | ns         | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub> | Output Enable Time                                 | 5.0               | 2.0 | 7.0                              | 9.0  |  |              | 2.0  | 9.5  | ns         | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PHL</sub> | Output Disable Time                                | 5.0               | 1.0 | 8.0                              | 10.0 |  |              | 1.0  | 10.5 | ns         | 2-5, 6      |
| toshl,                              | Output to Output Skew** Dn to On                   | 5.0               |     | 0.5                              | 1.0  |  |              |  | 1.0  | ns         |             |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (tosh) or LOW to HIGH (tosh). Parameter guaranteed by design.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshi) or LOW to HIGH (toshi). Parameter guaranteed by design.

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#### AC Operating Requirements: See Section 2 for Waveforms

|                |   |                   | 74A0               | CTQ  | 54ACTQ  | 74ACTQ   | ma9 l | Fig.<br>No. |
|----------------|---|-------------------|--------------------|------|---|--|-------|-------------|
| Symbol         | Parameter                                       | V <sub>CC</sub> * | T <sub>A</sub> = - |      | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 pF$ | Units |             |
|                |   |                   | Тур                | ao!" | Guaranteed Min  | lmum ) a a lis   | et Se |             |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0               | 0                  | 3.0  | Outputs   | 3.0  | ns    | 2-7         |
| t <sub>H</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 5.0               | 0910)89            | 1.5  | A -   | noi1.5 hose  | ns    | 2-7         |
| tw             | LE Pulse Width, HIGH                            | 5.0               | 2.0                | 4.0  | gon qui bayr-u (a)  | 4.0  | ns    | 2-3         |

is stored in the flip-flops on the low-to-high clock (CP) train- at improved latch-up immunity

\*Voltage Range 5.0 a 5.0V ±0.5Vc presented to the D inputs M Quaranteed pin-to-pin stow AC psVc.0± store 5.0V at 10 presented to the D inputs

# Capacitance to sales elicognostic and a studio and stud

| Symbol          | Parameter                        | Тур           | Units        | Conditions             | aup eemaang o<br>topaa hindering |
|-----------------|----------------------------------|---------------|--------------|------------------------|----------------------------------|
| CIN             | Input Capacitance                | 4.5           | -bpFil rotos | V <sub>CC</sub> = 5.0V | TOTAl output contr               |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | mumin42 Val A | pF .eona     | $V_{CC} = 5.0V$        | a spik ground bu                 |

Connection Diagrams

| EEE/IEC | For DiP, Fishpak and SOIC |
| EEE/IEC | For DiP, Fishpak and SOIC |
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| TRI-STATE Output Enable input |  |
|-------------------------------|--|
| TRI-STATE Outputs             |  |



# 54ACQ/74ACQ564 • 54ACTQ/74ACTQ564 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'ACTQ564 is a high speed octal D-type flip-flop with buffered common clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the low-to-high clock (CP) transition. The 'ACQ/'ACTQ564 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTOT™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

 Guaranteed simultaneous switching noise level and dynamic threshold performance

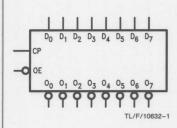
AC Operating Requirements: See Section 2 for W

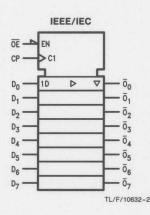
Symbol

- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with μP's
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'ACT564
- 4 kV minimum ESD immunity

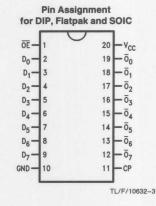
Ordering Code: See Section 8

#### **Logic Symbols**



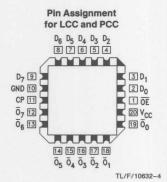


5-66



**Connection Diagrams** 

| Pin Names                         | Description                   |
|-----------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                   |
| CP                                | Clock Pulse Input             |
| ŌĒ                                | TRI-STATE Output Enable Input |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Outputs             |



#### Functional Description

The 'ACQ/'ACTQ564 consists of eight edge-triggered flipflops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

#### Function Table mumixsM stuloadA

| - 1 | nputs | t 700 - o<br>andress | Internal | Outputs    | Function            |  |  |
|-----|-------|----------------------|----------|------------|---------------------|--|--|
| OE  | CP    | D                    | s brQ    | ON         | anosudipiel(C\soff) |  |  |
| Н   | HV    | L                    | NC       | Z          | Hold Balley viggs   |  |  |
| Н   | Н     | Н                    | NC       | (Z) in     | Hold bold hand      |  |  |
| H   | 5     | L                    | Н        | Z          | Load                |  |  |
| Н   | 1     | Н                    | L        | Z          | Load                |  |  |
| L   | 1     | L                    | 6.0 H    | Н          | Data Available      |  |  |
| L   | _     | Н                    | L        | (NOI) toes | Data Available      |  |  |
| L   | Н     | L                    | NC       | NC         | No Change in Data   |  |  |
| L   | Н     | Н                    | NC       | NC         | No Change in Data   |  |  |

H = HIGH Voltage Level

L = LOW Voltage Level

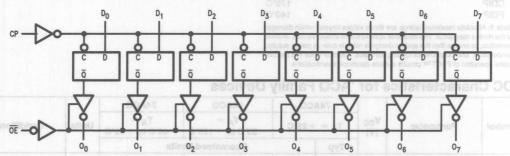
X = Immaterial

Z = High Impedance

= LOW-to-HIGH Transition

NC = No Change

#### **Logic Diagram**



TL/F/10632-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

|                              |  | 3.85                 | 3,85 | 3,85 |   |  |
|------------------------------|--|----------------------|------|------|---|--|
|                              |  |                      |      |      |   |  |
| Minimum Hig<br>Output Voltai |  |                      |      |      |   |  |
|                              |  | 2.56<br>3.86<br>4.86 |      |      |   | $^{4}V_{IN} = V_{IL} \text{ or } V_{IH}$ $-12 \text{ mA}$ $-14 \text{ mA}$ $-24 \text{ mA}$ $-24 \text{ mA}$ |
|                              |  |                      |      |      | ٧ |  |
|                              |  |                      |      |      |   | $V_{IM} = V_{IL} \text{ or } V_{IH}$ 12 mA 12 mA 10 L 24 mA 24 mA  |
|                              |  |                      |      |      |   |  |
|                              |  |                      |      |      |   | $V_{\rm OLD}=1.65 V$ Mex   |
|                              |  |                      |      |      |   |  |

| and the same of th | ny ana opeomeanons.                                 | clock and buffered Chaput En QOA's   | 2.0V to 6.0V           |
|--|---|--|------------------------|
| Supply Voltage (V <sub>CC</sub> )  | -0.5V to $+7.0V$                                    | er'ACTQ liw eqoff-qift trigle exT .eqoff   | 4.5V to 5.5V           |
| DC Input Diode Current ( $I_{IK}$ )<br>$V_I = -0.5V$<br>$V_I = V_{CC} + 0.5V$<br>DC Input Voltage ( $V_I$ )  | -20 mA<br>+20 mA<br>-0.5V to V <sub>CC</sub> + 0.5V | Input Voltage (V <sub>I</sub> ) Output Voltage (V <sub>O</sub> ) Operating Temperature (T <sub>A</sub> )           | 0V to Vcc<br>0V to Vcc |
| DC Output Diode Current ( $I_{OK}$ )<br>$V_O = -0.5V$<br>$V_O = V_{CC} + 0.5V$   | -20 mA<br>+20 mA                                    | 74ACQ/ACTQ 54ACQ/ACTQ Minimum Input Edge Rate ΔV/Δt 'ACQ Devices   |                        |
| DC Output Voltage (V <sub>O</sub> ) DC Output Source or Sink Current (I <sub>O</sub> )   | $-0.5$ V to to V <sub>CC</sub> + 0.5V $\pm$ 50 mA   | $V_{IN}$ from 30% to 70% of $V_{CC}$<br>$V_{CC}$ @ 3.0V, 4.5V, 5.5V<br>Minimum Input Edge Rate $\Delta V/\Delta t$ | 125 mV/ns              |
| DC V <sub>CC</sub> or Ground Current per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> )   | ± 50 mA   | 'ACTQ devices<br>V <sub>IN</sub> from 0.8V to 2.0V   |                        |
| Storage Temperature (T <sub>STG</sub> )  | -65°C to +150°C                                     | V <sub>CC</sub> @ 4.5V, 5.5V   | 125 mV/ns              |
| DC Latch-Up Source or Sink Curre<br>Junction Temperature (T,I)   | ent ±300 mA   | ma   | Logic Diagn            |
| CDIP   | 175°C   |  |                        |

#### DC Characteristics for 'ACQ Family Devices

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

|  | VAVA                                 |                     | 74A                     | CQ                   | 54ACQ                            | 74ACQ                           | VA                |  |  |
|--|--------------------------------------|---------------------|-------------------------|----------------------|----------------------------------|---------------------------------|-------------------|--|--|
| Symbol Parameter                                 | Parameter                            | V <sub>CC</sub> (V) | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units             | Conditions   |  |
|  | 0 09                                 |                     | Тур                     | 50                   | Guaranteed Lir                   | mits                            | 00                |  |  |
| V <sub>IH</sub> Minimum High Level Input Voltage |                                      | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85              | 2.1<br>3.15<br>3.85             | alb <b>V</b> a ta | $V_{OUT} = 0.1V$<br>or $V_{CC} = 0.1V$   |  |
| V <sub>IL</sub>                                  | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5   | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65              | 0.9<br>1.35<br>1.65             | ٧                 | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |  |
| V <sub>OH</sub>                                  | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5   | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                | 2.9<br>4.4<br>5.4               | ٧                 | $I_{OUT} = -50 \mu\text{A}$  |  |
|  |                                      | 3.0<br>4.5<br>5.5   |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                | 2.46<br>3.76<br>4.76            | ٧                 | $\label{eq:VIN} \begin{array}{ll} ^{*}\text{V}_{\text{IN}} = \text{V}_{\text{IL}}  \text{or}  \text{V}_{\text{IH}} \\ -  12  \text{mA} \\ \text{I}_{\text{OH}} & -  24  \text{mA} \\ -  24  \text{mA} \end{array}$ |  |
| V <sub>OL</sub>                                  | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5   | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                | 0.1<br>0.1<br>0.1               | V                 | I <sub>OUT</sub> = 50 μA   |  |
|  |                                      | 3.0<br>4.5<br>5.5   |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50             | 0.44<br>0.44<br>0.44            | ٧                 | $^{*} V_{\text{IN}} = V_{\text{IL}} \text{ or } V_{\text{IH}}$ 12 mA $^{\text{I}}_{\text{OL}} \qquad \qquad 24 \text{ mA}$ 24 mA   |  |
| I <sub>IN</sub>                                  | Maximum Input<br>Leakage Current     | 5.5                 | FILE                    | ±0.1                 | ±1.0                             | ±1.0                            | μА                | V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)  |  |
| IOLD   | †Minimum Dynamic                     | 5.5                 |                         |                      | 50                               | 75                              | mA                | V <sub>OLD</sub> = 1.65V Max   |  |
| I <sub>OHD</sub>                                 | Output Current                       | 5.5                 |                         |                      | -50                              | -75                             | mA                | V <sub>OHD</sub> = 3.85V Min   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

# DC Characteristics for 'ACQ Family Devices (Continued)

|                  |   | MACT                   | 744              | CQ         | 54ACQ                             |       | 74ACQ                            |       |   |
|------------------|---|------------------------|------------------|------------|-----------------------------------|-------|----------------------------------|-------|---|
| Symbol           | Parameter O'88                                  | V <sub>CC</sub><br>(V) | T <sub>A</sub> = | + 25°C     | T <sub>A</sub> = -55°C to + 125°C | -40   | T <sub>A</sub> =<br>0°C to +85°C | Units | Conditions  |
|                  |   |                        | Тур              | uarinariau | Guaranteed Li                     | imits |                                  |       |   |
| Icc -            | Maximum Quiescent<br>Supply Current             | 5.5                    |                  | 8.0        | 160.0                             | 8,0   | 80.0                             | μА    | V <sub>IN</sub> = V <sub>CC</sub> or GND (Note 1)     |
| loz              | Maximum TRI-STATE<br>Leakage Current            | 5.5                    |                  | ± 0.5      | ±10.0                             |       | ±5.0                             | μΑ    | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$ |
|                  | Leakage Culterit                                | 0.0                    |                  | 10.5       | 10.0                              | -     | ± 9.0                            | μπ    | $V_O = V_{CC}$ , GND                                  |
| VOLP             | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1.1              | 1.5        | 0.8                               |       | 8.8                              | *V    | Figures 1 and 2<br>(Notes 2 and 3)                    |
| V <sub>OLV</sub> | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6             | -1.2       | 1.5                               | N.T.  | 5.0                              | ٧     | Figures 1 and 2<br>(Notes 2 and 3)                    |
| V <sub>IHD</sub> | Minimum High Level<br>Dynamic Input Voltage     | 5.0                    | 3.1              | 3.5        | 8.1- 8                            | 0-    | 0,8                              | ٧٠    | (Notes 2 and 4)                                       |
| V <sub>ILD</sub> | Maximum Low Level<br>Dynamic Input Voltage      | 5.0                    | 1.9              | 1.5        | 8.8                               | 1.9   | fage 5.0                         | V     | (Notes 2 and 4)                                       |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 5V (\*ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

#### **DC Characteristics for 'ACTQ Family Devices**

|                 |                                      |                        | 74A                           | СТО          | 54ACTQ                            | 0.22 (0.1)                      | 74ACTQ       | P. 1150  | 111100000000000000000000000000000000000   |  |
|-----------------|--------------------------------------|------------------------|-------------------------------|--------------|-----------------------------------|---------------------------------|--------------|----------|---|--|
| Symbol          | Parameter                            | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C        |              | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C |              | Units    | Conditions  |  |
| No.             | to + 86°C Units                      |                        | Тур                           | (3)          | Guaranteed Li                     | mits                            | 1976         | Paran    | Symbol  |  |
| VIH             | Minimum High Level Input Voltage     | 4.5<br>5.5             | 1.5<br>1.5                    | 2.0          | 2.0                               | 2.0<br>2.0                      |              | ٧        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| VIL             | Maximum Low Level Input Voltage      | 4.5<br>5.5             | 1.5<br>1.5                    | 0.8          | 0.8<br>0.8                        | 8.8                             | 0.8          | V        | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |  |
| Voh             | Minimum High Level<br>Output Voltage | 4.5<br>5.5             | 4.49<br>5.49                  | 4.4<br>5.4   | 4.4<br>5.4                        | 8.8                             | 4.4<br>5.4   | V        | $I_{OUT} = -50 \mu A$   |  |
|                 | 3.0 13.5 ns<br>2.0 9.0<br>1.0 15.0   | 4.5<br>5.5             |                               | 3.86<br>4.86 | 3.70<br>4.70                      | 8.8                             | 3.76<br>4.76 | dselCi h | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$  |  |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 4.5<br>5.5             | 0.001<br>0.001                | 0.1          | 0.1                               | 0.0                             | 0.1          | uo V     | I <sub>OUT</sub> = 50 μA  |  |
|                 | 0.1                                  | 4.5<br>5.5             |                               | 0.36<br>0.36 | 0.50<br>0.50                      | 0.8                             | 0.44<br>0.44 | 10 V/0.1 | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IN} = V_{IL} \text{ or } V_{IH}$ |  |
| I <sub>IN</sub> | Maximum Input<br>Leakage Current     | 5.5                    | any two sepa<br>SH (tosta). F | ±0.1         | 1.0 ±1.0                          | rence f                         | ±1.0         | μА       | $V_I = V_{CC}$ , GND  |  |
| loz             | Maximum TRI-STATE<br>Leakage Current | 5.5                    |                               | ±0.5         | ±10.0                             |                                 | ±5.0         | μΑ       | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1:  $I_{|N}$  and  $I_{|CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{|CC}$  for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 5V. One output @ GND

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

#### DC Characteristics for 'ACTQ Family Devices (Continued) 101 2012 1913 1913 1913

|                  |   | THACH                  | 74A                    | СТО         | 54ACTQ                            | 74ACT                       | 2         |        |  |
|------------------|---|------------------------|------------------------|-------------|-----------------------------------|-----------------------------|-----------|--------|--|
| Symbol           | Parameter                                   | V <sub>CC</sub><br>(V) | T <sub>A</sub> = +25°C |             | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to + | 85°C      | Units  | Conditions (a  |
|                  |   |                        | Тур                    | เลาสารเกล่า | Guaranteed Li                     | mits                        |           | ->     |  |
| ICCT 00          | Maximum<br>I <sub>CC</sub> /Input           | 5.5                    | 0.6                    | 0.001       | 1.6 8                             | 1.5                         | int       | mA     | $V_{\rm I} = V_{\rm CC} - 2.1V_{\odot}$              |
| IOLD IV          | †Minimum Dynamic                            | 5.5                    |                        |             | 50                                | 75                          | 317       | mA     | V <sub>OLD</sub> = 1.65V Max                         |
| IOHD             | Output Current                              | 5.5                    |                        | 0.01 ±      | -50                               | -75                         |           | mA     | V <sub>OHD</sub> = 3.85V Min                         |
| Icc bas t        | Maximum Quiescent<br>Supply Current         | 5.5                    |                        | 8.0         | 160.0                             | 80.0                        |           | μΑ     | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |
| V <sub>OLP</sub> | Maximum High Level<br>Output Noise          | 5.0                    | 1.1                    | 1.5         | 5 -1.2                            | 0- 0.8                      | 30A 2     | V      | Figures 1 and 2<br>(Notes 2 and 3)                   |
| Volv             | Maximum Low Level Output Noise              | 5.0                    | -0.6                   | -1.2        | 3.5                               | 6.0 8.1                     | Jov       | e Vel  | Figures 1 and 2<br>(Notes 2 and 3)                   |
| V <sub>IHD</sub> | Maximum High Level<br>Dynamic Input Voltage | 5.0                    | 1.9                    | 2.2         | 7.5                               | 5.0 1.9                     | ies       | ol Kon | (Notes 2 and 4)                                      |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage     | 5.0                    | 1.2                    | 0.8         | tput under test.                  | sagglated with ou           | e tuqni e | V      | (Notes 2 and 4)                                      |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold  $(V_{ILD})$ , 0V to threshold  $(V_{IHD})$ , f=1 MHz.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |               |                  |         |                   |  |            | 74ACC   | 2           | 5  | 4ACQ  | 33   | 74/        | ACQ          |       |        |
|-------------------------------------|---------------|------------------|---------|-------------------|--|------------|---|-------------|--|-------|------|------------|--------------|-------|--------|
| Symbol                              | Parameter     |                  | ef 0    | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$ |             | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |       | 85°C | Units      | Fig.<br>No.  |       |        |
| Vt.0 =                              | ruoV          | V                |         | 2.0               |  | Min        | Тур   | Max         | Min  | Max   | A.A  | Min        | Max          | Minim | HIV    |
| f <sub>max/1.0</sub> =              | TELEVISION    | mum Clo<br>uency | ock     | 8.0               | 3.3<br>5.0                                       | 75<br>90   | 8.0   |             | 8.0  | 1.5   | 4.5  | 70<br>85   | a.I wo.J mur | MHz   | ΛIΓ    |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Prop<br>CP to | agation [<br>On  | Delay   | \$.\$<br>\$.3     | 3.3<br>5.0                                       | 3.0<br>2.0 | 9.5<br>6.5  | 13.0<br>8.5 | 4.4  |       | 4.5  | 3.0        | 13.5<br>9.0  | ns    | 2-3, 4 |
| <sup>†</sup> PZH, tPZL              | Outp          | ut Enabl         | e Time  | 2.78              | 3.3<br>5.0                                       | 3.0        | 9.5<br>6.5  | 13.0<br>8.5 | 20.0   |       | 24   | 3.0<br>2.0 | 13.5<br>9.0  | ns    | 2-5, 6 |
| t <sub>PHZ</sub> , t <sub>PHL</sub> | Outp          | ut Disabl        | le Time | 4.76              | 3.3<br>5.0                                       | 1.0        | 9.5   | 14.5<br>9.5 | 4.86   | 100.0 | 5.5  | 1.0        | 15.0<br>10.0 | ns    | 2-5, 6 |
| toshl,                              | Outp<br>CP to | ut to Out        | put Ske | **                | 3.3<br>5.0                                       |            | 1.5   | 1.0<br>1.0  | 1.0  | 100.0 | 6.5  |            | 1.5          | ns    | 30     |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$ 0.5V.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Voltage Range 3.3 is 3.3V ±0.3V.

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.

| Symbol         | nbol Parameter                                  |            |     | + 25°C<br>50 pF | $T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$ | $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 pF$ | Units | Fig. |
|----------------|---|------------|-----|-----------------|--|--|-------|------|
|                | Outpute   | ATE        | Тур | T ritiu         | Guaranteed Min   | imum   | a2 to | inc) |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 3.3<br>5.0 | 0   | 3.0             |  | 3.0<br>3.0   | ns    | 2-7  |
| t <sub>H</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 3.3<br>5.0 | 0   | 1.5<br>1.5      | ed ootal latch with  | 1.5<br>1.5   | ns    | 2-7  |
| t <sub>W</sub> | LE Pulse Width,                                 | 3.3<br>5.0 | 2.0 | 4.0             | ACTOS73 is functionally with inputs and out                        | 4.0 A 00   | ns    | 2-3  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V. Voltage Range 3.3 is 3.3V ±0.3V.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                     |                                  | V <sub>CC</sub> * | 74ACTQ                                     |     | 54ACTQ  T <sub>A</sub> = -55°C  to + 125°C  C <sub>L</sub> = 50 pF |        | $74ACTQ$ $T_A = -40^{\circ}C$ $to +85^{\circ}C$ $C_L = 50 \text{ pF}$ |         | Units | Fig.  |        |
|-------------------------------------|----------------------------------|-------------------|--|-----|--|--------|---|---------|-------|-------|--------|
| Symbol                              | Parameter                        |                   | $T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$ |     |  |        |   |         |       |       |        |
| 8                                   | meetion Diagram                  |                   | Min  | Тур | Max  | Min    | Max   | Min     | Max   | c Syn | Logi   |
| f <sub>max</sub>                    | Maximum Clock<br>Frequency       | 5.0               | 85   |     |  |        |   | 80      |       | MHz   |        |
| t <sub>PLH</sub> , t <sub>PHL</sub> | Propagation Delay<br>CP to On    | 5.0               | 2.0  | 7.0 | 9.0  |        |   | 2.0     | 9.5   | ns    | 2-3, 4 |
| t <sub>PZH</sub> , t <sub>PZL</sub> | Output Enable Time               | 5.0               | 2.0  | 7.0 | 9.0  | Jul 35 |   | 2.0     | 9.5   | ns    | 2-5, 6 |
| t <sub>PHZ</sub> , t <sub>PHL</sub> | Output Disable Time              | 5.0               | 1.0  | 8.0 | 10.0   | 37 31  |   | 1.0     | 10.5  | ns    | 2-5, 6 |
| toshl,<br>toslh                     | Output to Output Skew** CP to On | 5.0               |  | 0.5 | 1.0  | 00     |   | 40 g0 g | 1.0   | ns    | 20 0-  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V.

#### AC Operating Requirements: See Section 2 for Waveforms

| Symbol         | 70-727 0 m-70                                   |                          | 74A  | СТО | 54ACTQ   | 74ACTQ   |       |             |
|----------------|---|--------------------------|--|-----|--|--|-------|-------------|
|                | Parameter                                       | V <sub>CC</sub> *<br>(V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -55°C<br>to + 125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig.<br>No. |
|                |   |                          | Тур  | -   | Guaranteed Min   | imum   |       |             |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0                      | 0  | 3.0 | Boulgroot  | atugni 3.0g  | ns    | 2-7         |
| t <sub>H</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 5.0                      | 0  | 1.5 | Output Enable Input<br>atch Outputs                            | 1.5  | ns    | 2-7         |
| t <sub>W</sub> | LE Pulse Width,<br>HIGH or LOW                  | 5.0                      | 2.0  | 4.0 |  | 4.0  | ns    | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm$ 0.5V.

# Capacitance

| Symbol          | Parameter                        | Тур | Units | Conditions             |  |
|-----------------|----------------------------------|-----|-------|------------------------|--|
| CIN             | Input Capacitance                | 4.5 | pF    | $V_{CC} = 5.0V$        |  |
| C <sub>PD</sub> | Power Dissipation<br>Capacitance | 40  | pF    | V <sub>CC</sub> = 5.0\ |  |

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL) or LOW to HIGH (toSLH). Parameter guaranteed by design.



# 54ACQ/74ACQ573 • 54ACTQ/74ACTQ573 Quiet Series Octal Latch with TRI-STATE® Outputs

#### **General Description**

The 'ACQ/'ACTQ573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ( $\overline{OE}$ ) inputs. The 'ACQ/'ACTQ573 is functionally identical to the 'ACQ/'ACTQ373 but with inputs and outputs on opposite sides of the package. The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series<sup>TM</sup> features GTO<sup>TM</sup> output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- Guaranteed simultaneous switching raise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Improved latch-up immunity
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Outputs source/sink 24 mA
- Faster prop delays than standard 'ACT573
- 4 kV minimum ESD immunity

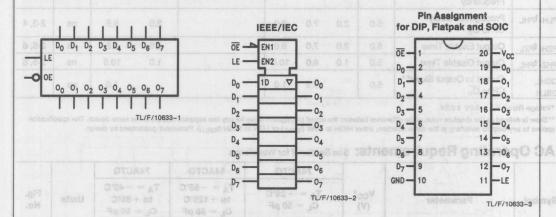
Ordering Code: See Section 8

**Logic Symbols** 

#### **Connection Diagrams**

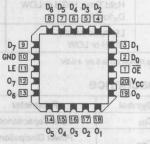
Symbol

AC Operating Requirements: seese



| Description                   |  |
|-------------------------------|--|
| Data Inputs                   | C  |
| Latch Enable Input            |  |
| TRI-STATE Output Enable Input |  |
| TRI-STATE Latch Outputs       |  |
|                               | Data Inputs Latch Enable Input TRI-STATE Output Enable Input |

Pin Assignment for LCC



TL/F/10633-4

#### Functional Description

The 'ACQ/'ACTQ573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable  $(\overline{\rm OE})$  input. When  $\overline{\rm OE}$  is LOW, the buffers are enabled. When  $\overline{\rm OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

#### Truth Table its I mumixsM stuload A

| ole2 votes | Inputs      | Miosas sos<br>nantali ed | Outputs         |
|------------|-------------|--------------------------|-----------------|
| ŌĒ         | ego LE vill | for <b>O</b> milat       | O <sub>n</sub>  |
| DA FOLAS   | Н           | Н                        | by Vellage (Vol |
| L          | Н           | (SEI) then               | nput Plode Out  |
| m 05_      | L           | X                        | 00              |
| Н          | X           | X                        | Z               |

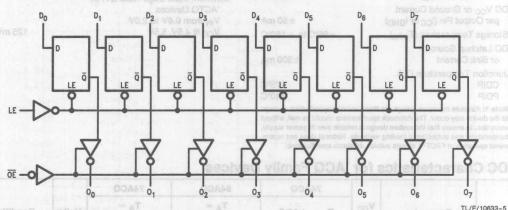
H = HIGH Voltage

L = LOW Voltage Z = High Impedance

X = Immaterial

O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW transition of Latch Enable

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Supply Voltage (V <sub>CC</sub> )         | -0.5V to $+7.0$ V               |
|---|---------------------------------|
| DC Input Diode Current (I <sub>IK</sub> ) |                                 |
| $V_1 = -0.5V$                             | -20 mA                          |
| $V_I = V_{CC} + 0.5V$                     | + 20 mA                         |
| DC Input Voltage (V <sub>I</sub> )        | -0.5V to V <sub>CC</sub> + 0.5V |

DC Output Diode Current (IOK)

 $V_0 = -0.5V$ -20 mA + 20 mA  $V_O = V_{CC} + 0.5V$ 

DC Output Voltage (Vo) -0.5V to to VCC + 0.5V DC Output Source

or Sink Current (IO) DC V<sub>CC</sub> or Ground Current

±50 mA per Output Pin (ICC or IGND) Storage Temperature (TSTG) 65°C to + 150°C

DC Latchup Source or Sink Current

±300 mA

Junction Temperature (T,I) CDIP PDIP

175°C 140°C

 $\pm 50 \, \text{mA}$ 

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

#### Recommended Operating Conditions of triple selection \$780 TOA'\QQA' self

Supply Voltage (V<sub>CC</sub>) 2.0V to 6.0V 'ACQ 'ACTQ 4.5V to 5.5V Input Voltage (V<sub>I</sub>) 0V to V<sub>CC</sub> Output Voltage (Vo)

Operating Temperature (TA) 74ACQ/ACTQ -40°C to +85°C

54ACQ/ACTQ -55°C to +125°C

Minimum Input Edge Rate ΔV/Δt 'ACQ Devices

VIN from 30% to 70% of VCC V<sub>CC</sub> @ 3.0V, 4.5V, 5.5V

125 mV/ns

Minimum Input Edge Rate ΔV/Δt 'ACTQ Devices V<sub>IN</sub> from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V

125 mV/ns

# **DC Characteristics for 'ACQ Family Devices**

| Symbol V <sub>IH</sub> | Parameter                            | .0                | 74                      | ACQ                  | 54ACQ   | 74ACQ                |       |   |
|------------------------|--------------------------------------|-------------------|-------------------------|----------------------|---|----------------------|-------|---|
|                        |                                      | V <sub>CC</sub>   |                         |                      | T <sub>A</sub> = T <sub>A</sub> =<br>-55°C to +125°C -40°C to +85°C |                      | Units | Conditions  |
|                        |                                      |                   | Тур                     |                      | Guaranteed Lin  | nits                 |       |   |
|                        | Minimum High Level<br>Input Voltage  | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85   | 2.1<br>3.15<br>3.85  | ٧     | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |
| V <sub>IL</sub>        | Maximum Low Level<br>Input Voltage   | 3.0<br>4.5<br>5.5 | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65   | 0.9<br>1.35<br>1.65  | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$  |
| V <sub>OH</sub>        | Minimum High Level<br>Output Voltage | 3.0<br>4.5<br>5.5 | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4   | 2.9<br>4.4<br>5.4    | ٧     | $I_{OUT} = -50 \mu$ A   |
|                        |                                      | 3.0<br>4.5<br>5.5 |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7   | 2.46<br>3.76<br>4.76 | V     | $V_{IN} = V_{IL} \text{ or } V_{IN} = V_{IL} \text{ or } V_{IN} = 12 \text{ m}$ $V_{IOH} = -24 \text{ m}$ $V_{IOH} = -24 \text{ m}$ |
| VoL                    | Maximum Low Level<br>Output Voltage  | 3.0<br>4.5<br>5.5 | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1   | 0.1<br>0.1<br>0.1    | ٧     | $I_{OUT} = 50 \mu A$  |
|                        |                                      | 3.0<br>4.5<br>5.5 |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50  | 0.44<br>0.44<br>0.44 | ٧     | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>II</sub><br>12 m.<br>I <sub>OL</sub> 24 m.<br>24 m.                                    |

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time

| Symbol              |   | PACTO                  |      |           | 54ACQ                             | 24                              | 74ACQ |                 |  |  |
|---------------------|---|------------------------|------|-----------|-----------------------------------|---------------------------------|-------|-----------------|--|--|
|                     | Parameter 3 aa                                  | V <sub>CC</sub><br>(V) |      |           | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C |       | Units           | Conditions   |  |
|                     |   |                        | Тур  | l bestrer | Guaranteed Li                     | mits                            |       |                 |  |  |
| I <sub>IN</sub> GMD | Maximum Input<br>Leakage Current                | 5.5                    |      | ±0.1      | ± ±1.0.0±                         |                                 | ±1.0  | μА              | V <sub>I</sub> = V <sub>CC</sub> , GND (Note 1)                                |  |
| IOLD H              | †Minimum Dynamic                                | 5.5                    |      | 0.0       | 50                                |                                 | 75    | mA              | V <sub>OLD</sub> = 1.65 V <sub>Max</sub>                                       |  |
| IOHD                | Output Current                                  | 5.5                    |      |           | -50                               |                                 | -75   | mA              | V <sub>OHD</sub> = 3.85 V <sub>Min</sub>                                       |  |
| Icc                 | Maximum Quiescent<br>Supply Current             | 5.5                    |      | 8.0       | 160.0                             | 8.0                             | 80.0  | μА              | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)                           |  |
| loz<br>nim Ves      | Maximum TRI-STATE<br>Leakage Curent             | 5.5                    |      | ±0.5      | ±11.0                             |                                 | ±5.0  | μА              | $V_{I}(OE) = V_{IL}, V_{IH}$<br>$V_{I} = V_{CC}, GND$<br>$V_{O} = V_{CC}, GND$ |  |
| V <sub>OLP</sub>    | Quiet Output<br>Maximum Dynamic V <sub>OL</sub> | 5.0                    | 1.1  | 1.5       | 0.5                               |                                 | 0.0   | trest<br>V      | Figures 1, 2<br>(Note 2, 3)  |  |
| V <sub>OLV</sub>    | Quiet Output<br>Minimum Dynamic V <sub>OL</sub> | 5.0                    | -0.6 | -1.2      | 0.1                               | 1.1                             | 0.6   | Isna I wo.      | Figures 1, 2<br>(Notes 2, 3)   |  |
| V <sub>IHD</sub>    | Minimum High Level Dynamic Input Voltage        | 5.0                    | 3.1  | 3.5       | \$.1-                             | 0.0                             | 0.6   | v <sup>és</sup> | (Notes 2, 4)   |  |
| V <sub>ILD</sub>    | Maximum Low Level Dynamic Input Voltage         | 5.0                    | 1.9  | 1.5       | 5,5                               | 8.1                             | 0.0   | and o V purque  | (Notes 2, 4)   |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One output @ GND.

Note 4: Max number of Data Inputs (n) switching. (n - 1) Inputs switching 0V to 5V ('ACQ). Input-under-test switching: 5V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>), f = 1 MHz.

## DC Characteristics for 'ACTQ Family Devices

| Symbol          | Parameter                            | V <sub>CC</sub> (V) | 74ACTQ 5           |              | 54ACTQ                           | 74ACTQ                          | ald the                             | MINDER JA  |
|-----------------|--------------------------------------|---------------------|--------------------|--------------|----------------------------------|---------------------------------|-------------------------------------|--|
|                 |                                      |                     | T <sub>A</sub> + 2 |              | T <sub>A</sub> = -55°C to +125°C | T <sub>A</sub> = -40°C to +85°C | Units                               | Conditions   |
|                 | to +85°C Unit                        |                     | Тур                |              | Guaranteed I                     | Limits (%)                      | retement                            | 4 ledmyi   |
| V <sub>IH</sub> | Minimum High Level Input Voltage     | 4.5<br>5.5          | 1.5<br>1.5         | 2.0          | 2.0<br>2.0                       | 2.0<br>2.0                      | ٧                                   | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| VIE             | Maximum Low Level Input Voltage      | 4.5<br>5.5          | 1.5<br>1.5         | 0.8          | 0.8                              | 0.8<br>0.8                      | V V                                 | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 4.5<br>5.5          | 4.49<br>5.49       | 4.4<br>5.4   | 4.4<br>5.4                       | 4.4<br>5.4                      | V                                   | $I_{OUT} = -50 \mu\text{A}$  |
| 2-5, 6          | 1.5 9.0 ns                           | 4.5<br>5.5          |                    | 3.86<br>4.86 | 3.70<br>4.70                     | 3.76<br>4.76                    | aT eVise                            | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = V_{IL} \text{ or } V_{IH}$ $V_{IOH} = V_{IL} \text{ or } V_{IH}$ |
| V <sub>OL</sub> | Maximum Low Level Output Voltage     | 4.5<br>5.5          | 0.001<br>0.001     | 0.1<br>0.1   | 0.1<br>0.1                       | 0.1                             | hr <b>y</b> u0                      | l <sub>OUT</sub> = 50 μA   |
| ocilication     | ds of the same device. The ap        | 4.5<br>5.5          | ny two sept        | 0.36         | 0.50<br>0.50                     | 0.44                            | 5.0± V0.8<br>8.3ñ0.8<br>etalosolute | $^*V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{1}V_{IN} = V_{IL} \text{ or } V_{IH}$ $^{24} \text{ mA}$   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub> as he besided hard I<sub>CC</sub> for 54ACQ @ 25°C is identical to 74ACQ @ 25°C.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                  |  |     | Тур  | Guaranteed i | <b>Guaranteed Limits</b> | 3             |                 |                           |  |
|------------------|--|-----|------|--------------|--------------------------|---------------|-----------------|---------------------------|--|
| IN CHO           | Maximum Input<br>Leakage Current         | 5.5 |      | ±0.1         | ±1.0 0±                  | ±1.0          |                 | μА                        | V <sub>I</sub> = V <sub>CC</sub> , GND               |
| loz V 88.        | Maximum TRI-STATE<br>Leakage Current     | 5.5 |      | ±0.5         | ±10.0                    | ±5.0          |                 | μА                        | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$        |
| ГССТ             | Maximum<br>I <sub>CC</sub> /Input        | 5.5 | 0.6  | 160.0        | 1.6                      | 1.5           | te              | mA                        | $V_{\rm I} = V_{\rm CC} - 2.1V$                      |
| lold             | †Minimum Dynamic                         | 5.5 |      |              | 50                       | 75            |                 | mA                        | V <sub>OLD</sub> = 1.65V Max                         |
| I <sub>OHD</sub> | Output Current                           | 5.5 |      | ± 1.0        | -50                      | -75           |                 | mA                        | V <sub>OHD</sub> = 3.85V Min                         |
| lcc MO           | Maximum Quiescent<br>Supply Current      | 5.5 |      | 8.0          | 160.0                    | 80.0          |                 | μΑ                        | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1) |
| VOLP             | Maximum High Level Output Noise          | 5.0 | 1.1  | 1.5          | 0.1                      | 0.0           | VOL             | Vynamic<br>V              | Figures 1, 2<br>(Notes 2, 3)                         |
| V <sub>OLV</sub> | Maximum Low Level Output Noise           | 5.0 | -0.6 | -1.2         | 200                      | 0.0           | JO/             | V<br>V<br>Itgh Levi       | Figures 1, 2<br>(Notes 2, 3)                         |
| V <sub>IHD</sub> | Maximum High Level Dynamic Input Voltage | 5.0 | 1.9  | 2.2          | 2.5                      | 0.0           | 996             | loV fugi<br>V<br>we I wo, | (Notes 2, 4)   |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage  | 5.0 | 1.2  | 0.8          | teat retinu turtud       | Tilw balsloos | age<br>input as | V so ablerts              | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

## AC Electrical Characteristics: See Section 2 for Waveforms

|  |   | - AT       |  | 74ACQ      |             | 54A   | CQ    | 74/  | ACQ          |               |             |
|--|---|------------|--|------------|-------------|---|-------|--|--------------|---------------|-------------|
| Symbol                                 | Parameter   |            | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            |             | T <sub>A</sub> = -<br>to + 1:<br>C <sub>L</sub> = ! | 25°C  | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |              | Units         | Fig.<br>No. |
| 0.1V                                   | = TUOV V  | 2.0        | Min  | Тур        | Max         | Min   | Max   | Min  | Max          | niniM<br>tued | FIIA        |
| t <sub>PHL</sub> ,<br>t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.3<br>5.0 | 2.5<br>1.5                                       | 8.5<br>5.5 | 10.5<br>7.0 | 1.5 0.1   | 40.40 | 2.5  | 11.0<br>7.5  | ns            | 2-3, 4      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 3.3<br>5.0 | 2.5<br>2.0                                       | 8.5<br>6.0 | 12.0<br>8.0 | 1.49 43   | 4.6   | 2.5  | 12.5<br>8.5  | ns            | 2-3, 4      |
| t <sub>PZL</sub> ,                     | Output Enable Time                                    | 3.3<br>5.0 | 2.5<br>1.5                                       | 8.5<br>6.0 | 13.0<br>8.5 | 66 64.0   | 6.0   | 2.5<br>1.5   | 13.5<br>9.0  | ns            | 2-5, 6      |
| t <sub>PHZ</sub> ,<br>t <sub>PLZ</sub> | Output Disable Time                                   | 3.3<br>5.0 | 1.0  | 9.0<br>6.0 | 14.5<br>9.5 | 8.4   | 6,5   | 1.0  | 15.0<br>10.0 | ns            | 2-5, 6      |
| toshl,                                 | Output to Output Skew** Dn to On                      | 3.3<br>5.0 |  | 1.0<br>0.5 | 1.5<br>1.0  | .0 100.   |       | Level  | 1.5<br>1.0   | ns            | JOY         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data Inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n - 1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ), f = 1 MHz.

Noltage Range 3.3 is 3.3V ±0.3V

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHL or LOW to HIGH (toShL)). Parameter guaranteed by design.

| Symbol         | Parameter                                       | V <sub>CC</sub> * |            | + 25°C<br>50 pF | $T_A = -55^{\circ}C$<br>to + 125°C<br>$C_L = 50 \text{ pF}$           | $T_A = -40^{\circ}C$<br>to $+85^{\circ}C$<br>$C_L = 50 \text{ pF}$ | Units | Fig. |
|----------------|---|-------------------|------------|-----------------|---|--|-------|------|
|                |   |                   | Тур        | aal             | Guaranteed Min  | imum 3 0 0 1   | 92 te | lu O |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 3.3<br>5.0        | 0          | 3.0<br>3.0      | Outputs   | 3.0<br>3.0   | ns    | 2-7  |
| t <sub>H</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 3.3<br>5.0        | 0          | 1.5<br>1.5      |   | 1.5<br>1.5   | ns    | 2-7  |
| tw             | LE Pulse Width, HIGH                            | 3.3<br>5.0        | 2.0<br>2.0 | 4.0<br>4.0      | ed, low-power column<br>r Clock (CP) and a b<br>ha information column | 4.0<br>4.0   | ns of | 2-3  |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V Dis of language on a study of the study of the Color of the Col

#### AC Electrical Characteristics: See Section 2 for Waveforms

|  |   | n 30 de                  | e autoro (e  | 74ACTQ                           |      | 54A  | СТО | 74A  | СТО  | and use | lounos      |
|--|---|--------------------------|--|----------------------------------|------|--|-----|--|------|---------|-------------|
| Symbol                                 | Parameter Age   | V <sub>CC</sub> *<br>(V) | Autority Contraction Contracti | A = +25<br>C <sub>L</sub> = 50 p |      | $T_{A} = -55^{\circ}C$ to +125°C $C_{L} = 50 \text{ pF}$ |     | T <sub>A</sub> = +40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |      | Units   | Fig.<br>No. |
|  |   |                          | Min  | Тур                              | Max  | Min  | Max | Min  | Max  |         |             |
| t <sub>PHL</sub> ,<br>t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 5.0                      | 2.0  | 6.5                              | 7.5  |  |     | 2.0  | 8.0  | ns      | 2-3, 4      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | 5.0                      | 2.5  | 7.0                              | 8.5  |  |     | 2.5  | 9.0  | ns      | 2-3, 4      |
| t <sub>PZL</sub> , t <sub>PZH</sub>    | Output Enable Time                                    | 5.0                      | 2.0  | 7.0                              | 9.0  | 10   |     | 2.0  | 9.5  | ns      | 2-5, 6      |
| t <sub>PHZ</sub> , t <sub>PLZ</sub>    | Output Disable Time                                   | 5.0                      | 1.0  | 8.0                              | 10.0 | fel 30   | - 1 | 1.0  | 10.5 | ns      | 2-5, 6      |
| toshl<br>toslh                         | Output to Output Skew** Dn to On                      | 5.0                      |  | 0.5                              | 1.0  | 90   |     |  | 1.0  | ns      | 40          |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V

### AC Operating Requirements: See Section 2 for Waveforms

|                | 8-15 B-00                                       | I br                     | 74A                               | СТО             | 54ACTQ                       | 74ACTQ   |       |             |
|----------------|---|--------------------------|-----------------------------------|-----------------|------------------------------|--|-------|-------------|
| Symbol         | Parameter Parameter                             | V <sub>CC</sub> *<br>(V) | T <sub>A</sub> = C <sub>L</sub> = | +25°C<br>50 pF  |                              | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig.<br>No. |
|                | PLIFFIGER                                       |                          | Тур                               | Guaranteed Mini |                              | imum   |       |             |
| ts             | Setup Time, HIGH or LOW<br>D <sub>n</sub> to LE | 5.0                      | 0                                 | 3.0             |                              | 3.0  | ns    | 2-7         |
| t <sub>H</sub> | Hold Time, HIGH or LOW<br>D <sub>n</sub> to LE  | 5.0                      | 0                                 | 1.5             | 1100001100                   | etugal 1.5 G   | ns (G | 2-7         |
| tw             | LE Pulse Width, HIGH                            | 5.0                      | 2.0                               | 4.0             | nguit<br>Output Enable Input | 4.0  | ns    | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V

#### Capacitance

| Symbol          | Parameter                     | Тур  | Units | Conditions      |
|-----------------|-------------------------------|------|-------|-----------------|
| CIN             | Input Capacitance             | 4.5  | pF    | $V_{CC} = 5.0V$ |
| C <sub>PD</sub> | Power Dissipation Capacitance | 42.0 | pF    | $V_{CC} = 5.0V$ |

5

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toshl or LOW to HIGH (toslh). Parameter guaranteed by design.



# 54ACQ/74ACQ574 • 54ACTQ/74ACTQ574 Quiet Series Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'ACQ/'ACTQ574 is a high-speed, low-power octal D-type flip-flop with a buffered Common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH clock (OP) transition.

'ACQ/'ACTQ574 utilizes Quiet Series technology to guarantee quiet output switching and improve dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

The 'ACQ/'ACTQ574 is functionally identical to the 'ACTQ374 but with different pin-out.

#### **Features**

Guaranteed simultaneous switching noise level and dynamic threshold performance

AC Operating Requirements: see Section 2 for

Symbol

Sym

- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of the package allowing easy interface with microprocessors
- Functionally identical to the 'ACQ/ACTQ374
- TRI-STATE outputs drive bus lines or buffer memory address registers

14 15 16 17 18 0<sub>5</sub> 0<sub>4</sub> 0<sub>3</sub> 0<sub>2</sub> 0<sub>1</sub>

TL/F/10634-4

- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT574
- 4 kV minimum ESD immunity

#### Ordering Code: See Section 8 **Logic Symbols Connection Diagrams** IEEE/IEC **Pin Assignment** for DIP, Flatpak and SOIC OE -EN D4 D2 D<sub>5</sub> D<sub>6</sub> D3 OE CP . > C1 20 Do 19 -00 -01 1D D $\nabla$ 18 Do D4 17 02 D<sub>1</sub> 0, 02 16 D2 02 D3 . -03 -04 TL/F/10634-1 15 DA D3 . 03 14 D5 --05 04 D4 · -06 D<sub>6</sub> -13 05 D5 -12 -06 D7 07 D6 -GND . 10 11 CP D7 --07 TL/F/10634-2 TL/F/10634-3 Pin Assignment **Pin Names** Description for LCC and PCC D0-D7 **Data Inputs** D6 D5 D4 D3 D2 CP Clock Pulse Input 87654 OE TRI-STATE Output Enable Input $\overline{O}_0 - \overline{O}_7$ TRI-STATE Outputs D<sub>7</sub> 9 GND 10 CP 11 0 0 12 0 6 13 3 D4 2 D<sub>0</sub> 1 OE 20 V<sub>CC</sub> 19 00 06 13

#### Functional Description

The 'ACQ/'ACTQ574 consists of eight edge-triggered flipflops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

#### **Function Table**

| bou  | nputs | ris i | Internal | Outputs   | Function              |  |  |  |
|------|-------|-------|----------|-----------|-----------------------|--|--|--|
| OE   | CP D  |       | Q        | ON        | grobulatel (A as the  |  |  |  |
| VH:  | - HV  | L     | NC       | Z         | (Hold apatio V yloqua |  |  |  |
| Н    | Н     | Н     | NC       | Z         | Hold                  |  |  |  |
| AHO  | 1     | L     | L        | Z         | Load Va.0 V           |  |  |  |
| AHO  | 5     | Н     | Н        | Z         | Load + soV = V        |  |  |  |
| V/LO | 1     | di    | 8.0-L    | L         | Data Available        |  |  |  |
| L    | 5     | Н     | Н        | (self the | Data Available        |  |  |  |
| ALO  | Н     | L     | NC       | NC        | No Change in Data     |  |  |  |
| ALO  | Н     | Н     | NC       | NC        | No Change in Data     |  |  |  |

H = HIGH Voltage Level

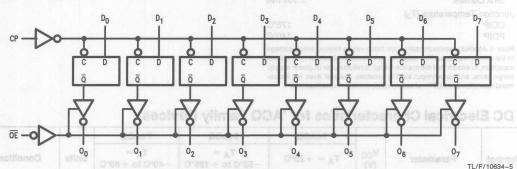
L = LOW Voltage Level

X = Immaterial

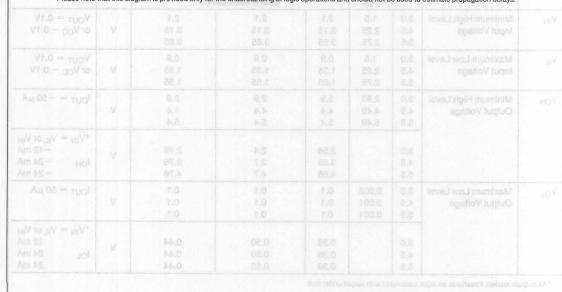
Z = High Impedance
\_\_ = LOW-to-HIGH Transition

NC = No Change

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/Distributors for avail                         | ability and specifications. |
|---|-----------------------------|
| Supply Voltage (V <sub>CC</sub> )                     | -0.5V  to  +7.0V            |
| DC Input Diode Current (IIK)                          |                             |
| $V_1 = -0.5V$ baod $\Sigma$                           | -20 mA                      |
| $V_I = V_{CC} + 0.5V$                                 | + 20 mA                     |
| DC Input Voltage (V <sub>I</sub> )                    | $-0.5V$ to $V_{CC} + 0.5V$  |
| DC Output Diode Current (IOK                          | ) H H C                     |
| $V_0 = -0.5V$   | -20 mA                      |
| $V_O = V_{CC} + 0.5V$                                 | ОИ H H+ 20 mA               |
| DC Output Voltage (V <sub>O</sub> )                   | $-0.5V$ to $V_{CC} + 0.5V$  |
| DC Output Source<br>or Sink Current (I <sub>O</sub> ) | ±50 mA                      |
| DC V <sub>CC</sub> or Ground Current                  |                             |
| per Output Pin (I <sub>CC</sub> or I <sub>GND</sub> ) | ±50 mA                      |
| Storage Temperature (T <sub>STG</sub> )               | -65°C to +150°C             |
| DC Latch-Up Source or                                 |                             |
| Sink Current  | ±300 mA                     |
| Junction Temperature (T <sub>J</sub> ) CDIP           | 175°C<br>140°C              |
| PDIP  | 140 C                       |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

## Recommended Operating

|  | SERVICE CHARLES SERVICE CONTRACTOR |
|--|------------------------------------|
| Supply Voltage (V <sub>CC</sub> )                  |                                    |
| 'ACQ and hugued baselind bas sooi                  | 2.0V to 6.0V                       |
| 'ACTQ IIIW agoit-oilt Ingle ent age                |                                    |
| Input Voltage (V <sub>I</sub> )                    | 0V to V <sub>CC</sub>              |
| Output Voltage (V <sub>O</sub> )                   | 0V to V <sub>CC</sub>              |
| Operating Temperature (T <sub>A</sub> )            |                                    |
| 74ACQ/ACTQ   | -40°C to +85°C                     |
| 54ACQ/ACTQ   | -55°C to +125°C                    |
| Minimum Input Edge Rate ΔV/Δt<br>'ACQ Devices      |                                    |
| V <sub>IN</sub> from 30% to 70% of V <sub>CC</sub> |                                    |
| V <sub>CC</sub> @ 3.0V, 4.5V, 5.5V                 | 125 mV/ns                          |
| Minimum Input Edge Rate ΔV/Δt<br>'ACTQ Devices     |                                    |
| V <sub>IN</sub> from 0.8V to 2.0V                  | 105 111                            |
| V <sub>CC</sub> @ 4.5V, 5.5V                       | 125 mV/ns                          |

### **DC Electrical Characteristics for 'ACQ Family Devices**

|                 |   | Description of                        | 74                      | ACQ                  | 54ACQ                             | 74ACQ                           | and the second | -< O− 30  |  |
|-----------------|---|---------------------------------------|-------------------------|----------------------|-----------------------------------|---------------------------------|----------------|---|--|
| Symbol          | Parameter  Minimum High Level Input Voltage | V <sub>CC</sub><br>(V)                | T <sub>A</sub> = +25°C  |                      | T <sub>A</sub> = -55°C to + 125°C | T <sub>A</sub> = -40°C to +85°C | Units          | Conditions  |  |
|                 |   | resel to estimate propagation delays. | Тур                     | bee anothere         | Guaranteed Lir                    | mits and babble on all mange    | that this di   | Please note   |  |
| V <sub>IH</sub> |   |                                       |                         | 2.1<br>3.15<br>3.85  | 2.1<br>3.15<br>3.85               | 2.1<br>3.15<br>3.85             | ٧              | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage          | 3.0<br>4.5<br>5.5                     | 1.5<br>2.25<br>2.75     | 0.9<br>1.35<br>1.65  | 0.9<br>1.35<br>1.65               | 0.9<br>1.35<br>1.65             | V              | V <sub>OUT</sub> = 0.1V<br>or V <sub>CC</sub> - 0.1V  |  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage        | 3.0<br>4.5<br>5.5                     | 2.99<br>4.49<br>5.49    | 2.9<br>4.4<br>5.4    | 2.9<br>4.4<br>5.4                 | 2.9<br>4.4<br>5.4               | V              | $I_{OUT} = -50 \mu\text{A}$   |  |
|                 |   | 3.0<br>4.5<br>5.5                     |                         | 2.56<br>3.86<br>4.86 | 2.4<br>3.7<br>4.7                 | 2.46<br>3.76<br>4.76            | V              | *V <sub>IN</sub> = V <sub>IL</sub> or V <sub>II</sub><br>-12 m/<br>I <sub>OH</sub> -24 m/<br>-24 m/ |  |
| V <sub>OL</sub> | Maximum Low Level<br>Output Voltage         | 3.0<br>4.5<br>5.5                     | 0.002<br>0.001<br>0.001 | 0.1<br>0.1<br>0.1    | 0.1<br>0.1<br>0.1                 | 0.1<br>0.1<br>0.1               | V              | I <sub>OUT</sub> = 50 μA  |  |
|                 |   | 3.0<br>4.5<br>5.5                     |                         | 0.36<br>0.36<br>0.36 | 0.50<br>0.50<br>0.50              | 0.44<br>0.44<br>0.44            | V              | $*V_{IN} = V_{IL} \text{ or } V_{IH}$ $12 \text{ mA}$ $I_{OL}$ $24 \text{ mA}$ $24 \text{ mA}$      |  |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

|                     |  | 74AC                   | 74        | ACQ             | 54ACQ                       | 745                 |            | 74ACQ                        |                    |   |        |
|---------------------|--|------------------------|-----------|-----------------|-----------------------------|---------------------|------------|------------------------------|--------------------|---|--------|
| Symbol              | Parameter  | V <sub>CC</sub><br>(V) | TA =      | + 25°C          | T <sub>A</sub> = -55°C to + | 125°C               | -40        | T <sub>A</sub> = °C to +85°C | Units              | Conditions  |        |
|                     |  |                        | Тур       | เการาสบอ        | Guaranteed Lim              |                     | mits       | mits                         |                    |   |        |
| I <sub>IN</sub> Vt. | Maximum Input<br>Leakage Current   | 5.5                    |           | ±0.1            | ±1.0                        |                     | 4.5        | ±1.0                         | μΑ                 | V <sub>I</sub> = V <sub>CC</sub> , GI<br>(Note 1)                     | ND H   |
| lold VI             | †Minimum Dynamic   | 5.5                    |           | 8,0             | 50                          | 8.7                 | 8.5        | 75                           | mA                 | V <sub>OLD</sub> = 1.65   | 5V Max |
| IOHD                | Output Current   | 5.5                    |           | 8.0             | 0_50                        | 1.5                 | 8.5        | -75                          | mA                 | V <sub>OHD</sub> = 3.85   | 5V Min |
| Icc 08              | Maximum Quiescent<br>Supply Current  | 5.5                    |           | 8.0             | 160.0                       | 6,49<br>6,49        | 4.5<br>5.5 | 80.0                         | μΑ                 | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note                     | e 1)   |
| loz                 | Maximum TRI-STATE<br>Leakage Current   | 5.5                    |           | ±0.5            | ±10.0                       |                     | 4.5        | ±5.0                         | μΑ                 | $V_{I}(OE) = V_{IL}$<br>$V_{I} = V_{CC}$ , GI<br>$V_{O} = V_{CC}$ , G | ND     |
| V <sub>OLP</sub>    | Quiet Output<br>Maximum Dynamic V <sub>OL</sub>                                | 5.0                    | 1.1       | 1.5             | 0.1                         | 100.0               | 4.5<br>5.5 |                              | V <sub>eg</sub>    | Figures 1, 2<br>(Notes 2, 3)  | 105    |
| Volv                | Quiet Output<br>Minimum Dynamic V <sub>OL</sub>                                | 5.0                    | -0.6      | <sub>-1.2</sub> | 86,0                        |                     | 4,5        |                              | ٧                  | Figures 1, 2<br>(Notes 2, 3)  |        |
| V <sub>IHD</sub>    | Minimum High Level Dynamic Input Voltage                                       | 5.0                    | 3.1       | 3.5             | 1.0±                        |                     | 5.5        | tage Current                 | se V <sub>he</sub> | (Notes 2, 4)  | M      |
| V <sub>ILD</sub>    | Maximum Low Level Dynamic Input Voltage  | 5.0                    | 1.9       | 0.9.5           | ±0.5                        |                     | 8.6        |                              | Vien               | (Notes 2, 4)  | 20     |
|                     | uts loaded; thresholds on input a<br>m test duration 2.0 ms, one outp          |                        |           | ut under test.  |                             | 0.6                 | 6.5        |                              |                    | mumbasM<br>tuqnf\qoi  | T00    |
|                     | IN and I <sub>CC</sub> @ 3.0V are guarantee                                    |                        |           | equal to the re | spective limit @            | 5.5V V <sub>C</sub> | 5.ē        |                              |                    |   |        |
|                     | Vorst case package.  | 1 10 7470              | JQ 6 20 0 |                 |                             |                     |            |                              |                    |   |        |
| Note 4: N           | Max number of outputs defined a<br>Maximum number of data inputs (<br>= 1 MHz. |                        |           |                 |                             |                     | inder-tes  |                              |                    | f (V <sub>ILD</sub> ), 0V to three                                    | eshold |
| 2                   | Pigues 1,<br>(Notes 2, 1   |                        |           |                 |                             | 1.1                 |            |                              |                    |   |        |
|                     |  |                        |           |                 |                             |                     | 6.0        |                              |                    | Maximum Lo<br>Output Noise  |        |
|                     |  |                        |           |                 |                             | 9.1                 |            |                              |                    | Maximum Hi<br>Dynamic Inp   |        |
|                     |  |                        |           |                 |                             |                     |            |                              |                    |   |        |

|                    |   | asle       | Тур                   | Gueran       | Guaranteed   | Limits                             |       |  |
|--------------------|---|------------|-----------------------|--------------|--------------|------------------------------------|-------|--|
| V <sub>IH</sub> QV | Minimum High Level<br>Input Voltage         | 4.5<br>5.5 | 1.5<br>1.5            | 2.0<br>2.0   | 2.0<br>2.0   | 2.0<br>2.0                         | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| SV Man             | Maximum Low Level<br>Input Voltage          | 4.5<br>5.5 | 1.5<br>1.5            | 0.8          | 0.8<br>0.8   | 0.8                                | ٧     | $V_{OUT} = 0.1V$<br>or $V_{CC} - 0.1V$   |
| VoH                | Minimum High Level<br>Output Voltage        | 4.5<br>5.5 | 4.49<br>5.49          | 4.4<br>5.4   | 4.4<br>5.4   | 4.4<br>5.4                         | ٧     | $I_{OUT} = -50 \mu\text{A}$  |
|                    |   | 4.5<br>5.5 |                       | 3.85<br>4.86 | 3.70<br>4.70 | 3.76<br>4.76                       | B-IRI | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $-24 \text{ mA}$ $-24 \text{ mA}$   |
| V <sub>OL</sub>    | Maximum Low Level<br>Output Voltage         | 4.5<br>5.5 | 0.001<br>0.001        | 0.1<br>0.1   | 0.1<br>0.1   | 0.1<br>0.1                         | ٧     | Ι <sub>ΟUT</sub> = 50 μΑ   |
|                    | V Agurés 1, 2<br>(Notes 2, 3)               | 4.5<br>5.5 |                       | 0.36<br>0.36 | 0.50<br>0.50 | 0.44<br>0.44                       | V     | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ $V_{IOL} = V_{IL} \text{ or } V_{IH}$ |
| I <sub>IN</sub>    | Maximum Input Leakage Current               | 5.5        |                       | ±0.1         | ±1.0         | ±1.0                               | μΑ    | $V_I = V_{CC}$ , GND   |
| loz                | Maximum TRI-STATE<br>Leakage Current        | 5.5        |                       | ±0.5         | ±10.0        | ±5.0                               | μΑ    | $V_I = V_{IL}, V_{IH}$<br>$V_O = V_{CC}, GND$  |
| ГССТ               | Maximum<br>I <sub>CC</sub> /Input           | 5.5        | 0.6                   |              | 1.6 1.6 m    | in the behavior to the behavior to | mA    | $V_{\rm I} = V_{\rm CC} - 2.1V$  |
| lold               | †Maximum Dynamic                            | 5.5        | Suby Vala             | Filmil evit  | 50           | 75                                 | mA    | V <sub>OLD</sub> = 1.65V Max   |
| IOHD               | Output Current                              | 5.5        |                       |              | -50          | -75                                | mA    | V <sub>OHD</sub> = 3.85V Min   |
| Icc<br>blone       | Maximum Quiescent<br>Supply Current         | 5.5        | e GND.<br>B. Input-un | 8.0          | 160.0        | 80.0                               | μА    | V <sub>IN</sub> = V <sub>CC</sub><br>or GND (Note 1)   |
| V <sub>OLP</sub>   | Maximum High Level<br>Output Noise          | 5.0        | 1.1                   | 1.5          |              |                                    | ٧     | Figures 1, 2<br>(Notes 2, 3)   |
| V <sub>OLV</sub>   | Maximum Low Level Output Noise              | 5.0        | -0.6                  | -1.2         |              |                                    | ٧     | Figures 1, 2<br>(Notes 2, 3)   |
| V <sub>IHD</sub>   | Maximum High Level<br>Dynamic Input Voltage | 5.0        | 1.9                   | 2.2          |              |                                    | ٧     | (Notes 2, 4)   |
| V <sub>ILD</sub>   | Maximum Low Level Dynamic Input Voltage     | 5.0        | 1.2                   | 0.8          |              |                                    | V     | (Notes 2, 4)   |

<sup>\*</sup>All outputs loaded; thresholds on input associated with output under test.

<sup>†</sup>Maximum test duration 2.0 ms, one output loaded at a time.

Note 1: I<sub>CC</sub> for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 2: Worst case package.

Note 3: Max number of outputs defined as (n). Data inputs are driven 0V to 3V. One output @ GND.

Note 4: Max number of data inputs (n) switching. (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold ( $V_{ILD}$ ), 0V to threshold ( $V_{IHD}$ ), f = 1 MHz.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |       | ZAACTO                 | OTO               | ANG  | 74ACC      | OTO/  | 54  | ACQ  | 744        | CQ                      |             |       |
|------------------|-------|------------------------|-------------------|--|------------|---|-----|--|------------|-------------------------|-------------|-------|
| Symbol           | Unite | Parameter              | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |     | $T_A = -40$ °C<br>to $+85$ °C<br>$C_L = 50 \text{ pF}$ |            | Units                   | Fig.<br>No. |       |
|                  |       | zella nila             | Max               | Min  | Тур        | Max   | Min | Max  | Min        | Max                     |             |       |
| f <sub>max</sub> |       | imum Clock 08<br>uency | 3.3<br>5.0        | 75<br>90   |            |   | 86  | 5.0  | 70<br>85   | mum Glack<br>southon De | MHz         | xemi  |
| t <sub>PLH</sub> |       | agation Delay          | 3.0<br>5.0        | 3.0<br>2.0                                       | 9.5<br>6.5 | 13.0<br>8.5   | 2.0 | 0.6  | 3.0<br>2.0 | 13.5<br>9.0             | ns          | 2-3,4 |
| t <sub>PZH</sub> | Outp  | out Enable Time        | 3.3<br>5.0        | 3.0<br>2.0                                       | 9.5<br>6.5 | 13.0<br>8.5   | 95  | 0.8  | 3.0<br>2.0 | 13.5<br>9.0             | ns          | 2-5,6 |
| t <sub>PH7</sub> | Outp  | out Disable Time       | 3.3<br>5.0        | 1.0  | 9.5<br>8.0 | 14.5<br>9.5   | 0.1 | 0.8  | 1.0        | 15.0<br>10.0            | ns          | 2-5,6 |
| toshl,           |       | out to Output Skew**   | 3.3<br>5.0        |  | 1.0        | 1.5   |     | 0.6  | V/a        | 1.5 0                   | ns          |       |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V and the arranges own years and positional

#### AC Operating Requirements: See Section 2 for Waveforms

|                    | 8°C TA = -40°C Unit              | TA = -12          | 74   | ACQ AT     | 54ACQ  | 74ACQ              |             | oloma 2     |
|--------------------|----------------------------------|-------------------|--|------------|--|--------------------|-------------|-------------|
| Symbol             | Parameter                        | V <sub>CC</sub> * | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |            | T <sub>A</sub> = -59<br>to + 125°<br>C <sub>L</sub> = 50 p | C to +85°C         | Units       | Fig.<br>No. |
| 7-S                | en 0.8                           |                   | Тур  | 0          | Guaranteed   | d Minimum          | Setu        | ts          |
| ts<br>T-S          | Setup Time, HIGH or LOW Dn to CP | 3.3<br>5.0        | 0  | 3.0<br>3.0 | 0.8  | WC J to H 3.0 smiT | ns ns       | 2-7         |
| t <sub>H</sub> 2-8 | Hold Time, HIGH or LOW           | 3.3<br>5.0        | 0  | 1.5<br>1.5 | 0.8  | 1.5<br>1.5         | ns          | 2-7         |
| t <sub>W</sub>     | LE Pulse Width,<br>HIGH or LOW   | 3.3<br>5.0        | 2.0<br>2.0                                       | 4.0<br>4.0 |  | 4.0<br>4.0         | 0.8 enserie | 2-3         |

<sup>\*</sup>Voltage Range 5.0 is 5.0V  $\pm 0.5$ V Voltage Range 3.3 is 3.3V  $\pm 0.3$ V

| Conditions  | Typ |  |
|-------------|-----|--|
| V0.8 = 0.0V | 4.6 |  |
| Vcc = 5.0V  |     |  |

Voltage Range 3.3 is 3.3V ± 0.3V sugnordements 4.4233 Highlight WOLT (4.435) WOLT WHOTH write protocols could entire griddens stropus and selection

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t<sub>OSHL</sub>) or LOW to HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

### AC Electrical Characteristics: See Section 2 for Waveforms (Size 1981) 1801 1901 1901 1901

| Symbol             | YAACG         | 004                 | 54                    | 74ACT  | 2 004 | 54ACTQ  |     | 74/  | 74ACTQ |                             |             |               |
|--------------------|---------------|---------------------|-----------------------|--|-------|---|-----|--|--------|-----------------------------|-------------|---------------|
|                    | dinU          | Parameter           | V <sub>CC</sub> * (V) | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |       | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF |        | Units                       | Fig.<br>No. |               |
|                    | xoM niM       | Min Max             | 2012                  | Min  | Тур   | Max   | Min | Max  | Min    | Max                         |             |               |
| f <sub>max</sub>   | Maxi          | mum Clock Frequency | 5.0                   | 85   |       |   | 76  | 3.3  | 80     | mum Clock                   | MHz         | xanti         |
| t <sub>PLH</sub> , | Prop<br>CP to | agation Delay       | 5.0                   | 2.0  | 7.0   | 9.0   | 3,0 | 3.0  | 2.0    | 9.5                         | ns<br>ns    | 2-3, 4        |
| t <sub>PZH</sub> , | Outp          | ut Enable Time      | 5.0                   | 20   | 7.0   | 9.0   | 0.9 | 8.0  | 2.0    | 0.0<br>7.0<br>1.0 En able T | 190<br>ns   | 2-5, 6        |
| t <sub>PHZ</sub> , | Outp          | ut Disable Time     | 5.0                   | 1.0  | 8.0   | 10.0  | 2.0 | 9.9  | 1.0    | 10.5                        | ns          | 2-7           |
| toshl,             | Outp<br>CP to | ut to Output Skew** | 5.0                   |  | 0.5   | 1.0   | 0.1 | 9.0  | Skew** | 1.0                         | ns          | roshr<br>priz |

<sup>\*</sup>Voltage Range 5.0 is 5.0V ±0.5V.

#### AC Operating Requirements: See Section 2 for Waveforms

|        |   | 0.00 | 74A  | CTQ    | 54ACTQ  | 74ACTQ   | Opera | DA          |
|--------|---|------|--|--------|---|--|-------|-------------|
| Symbol | Parameter                                       | 100  | T <sub>A</sub> = +25°C<br>C <sub>L</sub> = 50 pF |        | T <sub>A</sub> = -55°C<br>to +125°C<br>C <sub>L</sub> = 50 pF | T <sub>A</sub> = -40°C<br>to +85°C<br>C <sub>L</sub> = 50 pF | Units | Fig.<br>No. |
|        | 8°C to +86°C Unit                               |      | Тур  | CL = 5 | Guaranteed Mi   | nimum  | 10    | Symb        |
| ts     | Setup Time, HIGH or LOW<br>D <sub>n</sub> to CP | 5.0  | 0  | 3.0    |   | 3.0  | ns    | 2-7         |
| tHS    | Hold Time, HIGH or LOW<br>D <sub>n</sub> to CP  | 5.0  | 0.8  | 1.5    | 8.0   | 1.5 90 0   | ns    | 2-7         |
| tw     | LE Pulse Width,<br>HIGH or LOW                  | 5.0  | 2.0  | 4.0    | 6.6 W   | 4.0 90   | ns    | 2-3         |

\*Voltage Range 5.0 is 5.0V ±0.5V

### Capacitance

| Symbol  | Parameter         | Тур  | Units | Conditions             |  |
|---|-------------------|------|-------|------------------------|--|
| CIN   | Input Capacitance | 4.5  | pF    | V <sub>CC</sub> = 5.0V |  |
| C <sub>PD</sub> Power Dissipation Capacitance |                   | 40.0 | pF    | $V_{CC} = 5.0V$        |  |

<sup>\*\*</sup>Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (toSHI) or LOW to HIGH (toSLH). Parameter guaranteed by design.



# 54ACQ/74ACQ646 • 54ACTQ/74ACTQ646 Quiet Series Octal Transceiver/Register with TRI-STATE® Outputs

#### **General Description**

The 'ACQ/'ACTQ646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA).

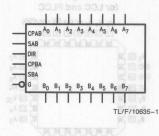
The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

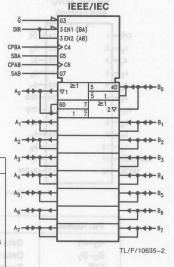
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Independent registers for A and B busses
- Multiplexed real-time and stored data transfers
- 300 mil slim dual-in-line package
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/'ACT646
- 4 kV minimum ESD immunity

The information on the ACQ646 is Advanced Information only.

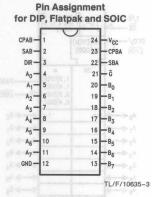
#### **Logic Symbols**

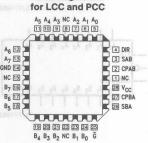


| Pin Names                      | Description             |
|--------------------------------|-------------------------|
| A <sub>0</sub> -A <sub>7</sub> | Data Register A Inputs  |
|                                | Data Register A Outputs |
| B <sub>0</sub> -B <sub>7</sub> | Data Register B Inputs  |
|                                | Data Register B Outputs |
| CPAB, CPBA                     | Clock Pulse Inputs      |
| SAB, SBA                       | Transmit/Receive Inputs |
| G                              | Output Enable Input     |
| DIR                            | Direction Control Input |



#### **Connection Diagrams**





**Pin Assignment** 

TL/F/10635-4

### 54ACQ/74ACQ657 • 54ACTQ/74ACTQ657 Quiet Series Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

#### **General Description**

The 'ACQ/'ACTQ657 contains eight non-inverting buffers with TRI-STATE outputs and an 8-bit parity generator/ checker. Intended for bus oriented applications, the device combines the '245 and the '280 functions in one package.

The 'ACQ/'ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series<sup>TM</sup> features GTOTM output control and undershoot corrector in addition to a split ground bus for superior performance.

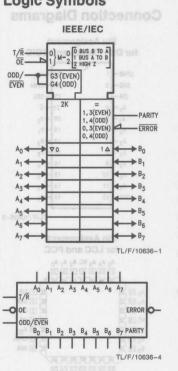
#### **Features**

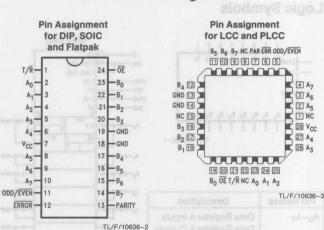
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Combines the '245 and the '280 functions in one package
- 300 mil 24-pin slim dual-in-line package
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity

The information on the ACQ657 is Advanced Information only.

#### **Logic Symbols**

#### **Connection Diagrams**





| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| A <sub>0</sub> -A <sub>7</sub> | Data Inputs/TRI-STATE Outputs |
| B <sub>0</sub> -B <sub>7</sub> | Data Inputs/TRI-STATE Outputs |
| T/R                            | Transmit/Receive Input        |
| ŌĒ                             | Enable Input                  |
| PARITY                         | Parity Input/TRI-STATE Output |
| ODD/EVEN                       | ODD/EVEN Parity Input         |
| ERROR                          | Error Output                  |

# 54ACQ/74ACQ821 Quiet Series 10-Bit D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

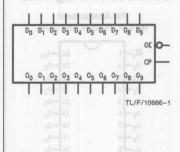
The 'ACQ821 is a 10-bit D flip-flop with non-inverting TRI-STATE outputs arranged in a broadside pinout. The ACQ821 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

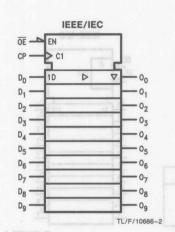
#### **Features**

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Non-inverting TRI-STATE outputs for bus interfacing
- 4 kV minimum ESD immunity
- Outputs source/sink 24 mA
- Functionally identical to the AM29821

#### **Logic Symbols**

#### **Connection Diagrams**

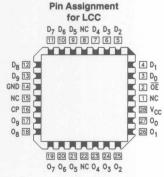






TL/F/10686-3

| Pin Names                      | Description         |
|--------------------------------|---------------------|
| D <sub>0</sub> -D <sub>9</sub> | Data Inputs         |
| 00-09                          | Data Outputs        |
| ŌĒ                             | Output Enable Input |
| CP                             | Clock Input         |



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5



## 54ACTQ/74ACTQ827 Quiet Series 10-Bit Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'ACTQ827 10-bit bus buffer provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility. The 'ACTQ827 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ feature GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

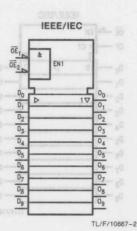
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- Functionally and pin-compatible to AMD's AM29827
- 'ACTQ827 has TTL-compatible inputs
- 4 kV minimum ESD immunity

#### **Logic Symbols**



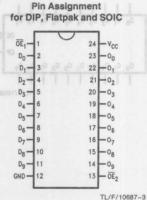
Connection Diagrams

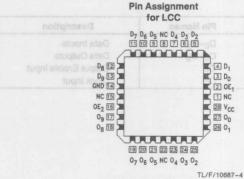
| Pin Names                          | Description   |
|------------------------------------|---------------|
| $\overline{OE}_1, \overline{OE}_2$ | Output Enable |
| D <sub>0</sub> -D <sub>7</sub>     | Data Inputs   |
| 00-07                              | Data Outputs  |



#### **Connection Diagrams**

Logic Symbols







## 54ACTQ/74ACTQ841 Quiet Series 10-Bit Transparent Latch with TRI-STATE® Outputs

#### **General Description**

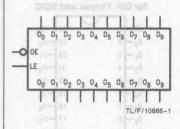
The 'ACTQ841 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The '841 is a 10-bit transparent latch, a 10-bit version of the '373, The 'ACTQ841 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance, FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

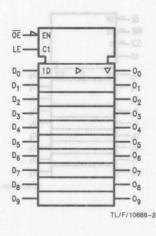
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on opposite sides of package allow easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- 'ACTQ841 has TTL-compatible inputs
- 4 kV minimum ESD immunity

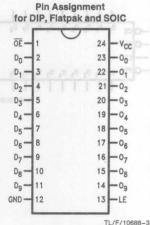
#### **Logic Symbols**

#### **Connection Diagrams**



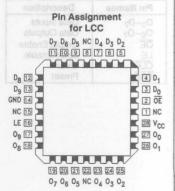
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| Pin Names                      | Description       |
|--------------------------------|-------------------|
| D <sub>0</sub> -D <sub>9</sub> | Data Inputs       |
| 00-09                          | TRI-STATE Outputs |
| ŌĒ                             | Output Enable     |
| LE                             | Latch Enable      |

ME (E) 3919



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# 54ACTQ/74ACTQ843 Quiet Series 8-Bit Transparent Latch

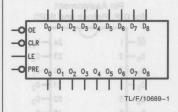
#### **General Description**

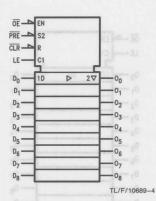
The 'ACTQ843 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths. The 'ACTQ843 utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series<sup>TM</sup> features GTO<sup>TM</sup> output control and undershoot corrector in addition to a split ground bus for superior performance.

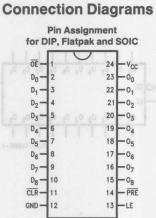
#### **Features**

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed pin-to-pin skew AC performance
- Inputs and outputs on oppostie sides of package for easy interface with microprocessors
- Improved latch-up immunity
- Outputs source/sink 24 mA
- 'ACTQ843 has TTL-compatible inputs
- Functionally and pin-compatible to AMD's AM29843
- 4 kV minimum ESD immunity
- 'ACT843 has TTL-compatible inputs
- TRI-STATE® outputs for bus interfacing

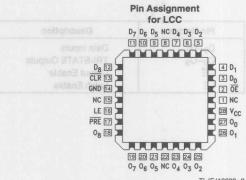
#### **Logic Symbols**







| Pin Names                      | Description   |
|--------------------------------|---------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs   |
| 00-07                          | Data Outputs  |
| OE 30 20 30                    | Output Enable |
| LE BBC                         | Latch Enable  |
| CLR                            | Clear         |
| PRE                            | Preset        |
|                                |               |



TI /F/10689-2



#### Section 6 Contents

| 54FCTV74FCT138 1-to-8 Multiplexer,                                     |
|--|
| 54FCT/74FCT240 Octal Buffer/Line Driver with TRI-STATE Outputs         |
| 54FCT/74FCT241 Octal Buffer/Line Driver with TRI-STATE Outputs.        |
|  |
| 54FCT/74FCT245 Octal Buffer/Line Driver with TRI-STATE Outputs         |
| 54FCT/74FCT273 Octal D Flip-Flop                                       |
| 54FCT/74FCT373 Octal Transparent Latch with TRI-STATE Outputs          |
| 54FCT/74FCT374 Octal D Flip-Flop with TRI-STATE Outputs                |
| 54FCT/74FCT377 Octal D Flip 6 notion 6 Section 6                       |
| 54FCT/74FCT521 8-Bit Identity Comparator                               |
| FCT Series Datasheets 1946   |
| 54FCT/74FCT534 Octal D Flip-Flop with TRI-STATE Outputs                |
| 54FCT540 Inverting Octal Buffer/Line Driver with TRI-STATE Outputs     |
| 54PCT541 Non-Inverting Octal Buffer/Line Driver with TRI-STATE Outputs |
| 54FCT/74FCT543 Octal Registered Transpelver with TRI-STATE Outputs     |
| 54FCT/74FCT544 Octal Registered Transcelver with TRI-STATE Outputs     |
|  |
| 54FCT/74FCT564 Octal D Flip-Flop with TRI-STATE Outputs                |
|  |
|  |
|  |



### **Section 6 Contents**

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|--|------|
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| 54FCT/74FCT373 Octal Transparent Latch with TRI-STATE Outputs          | 6-25 |
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| 54FCT/74FCT544 Octal Registered Transceiver with TRI-STATE Outputs     | 6-60 |
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| 54FCT/74FCT573 Octal Transparent Latch with TRI-STATE Outputs          | 6-70 |
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| 54FCT/74FCT646 Octal Transceiver/Register with TRI-STATE Outputs       | 6-80 |

#### 34FU1//4FU1138

### 1-of-8 Decoder/Demultiplexer

#### **General Description**

The 'FCT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'FCT138 devices or a 1-of-32 decoder using four 'FCT138 devices and one inverter.

FACTTM FCT utilizes NSC quiet series technology to provide improved guiet output switching and dynamic threshold

FACT FCT features GTOTM output control and undershoot corrector in addition to a split ground bus for superior per-

#### **Features**

- NSC 54FCT/74FCT138 is pin and functionally equivalent to IDT 54FCT/74FCT138
- Demultiplexing capability sac bevolume ad at bencia
- Multiple input enable for easy expansion
- Active LOW mutually exclusive outputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OI</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels

Vcc

15 - On

11 -04

10 -05

-06

TL/F/10657-2

12  $-\bar{o}_3$ 

 $-\bar{o}_2$ 

**Pin Assignment** for DIP, Flatpak and SOIC

E3

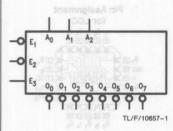
07

GND -

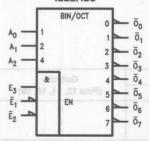
- ESD immunity ≥ 4 kV typ
- Military Product compliant to MIL-STD 883 and Standard Military Drawing #5962-87654

#### **Logic Symbol**

#### **Connection Diagrams**

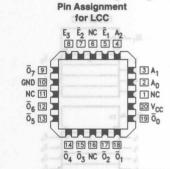


IEEE/IEC



TL/F/10657-4

| Pin Names                                 | Description                     |
|---|---------------------------------|
| $A_0-A_2$ $\overline{E}_1-\overline{E}_2$ | Address Inputs<br>Enable Inputs |
| $\overline{O}_0 - \overline{O}_7$         | Enable Input<br>Outputs         |



TL/F/10657-3



### 54FCT/74FCT240 **Inverting Octal Buffer/Line Driver** with TRI-STATE® Outputs

#### General Description

The 'FCT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance. Eas GTE-JiM of Insilation Toubons yushilid as

#### **Features**

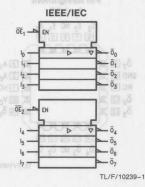
- NSC 54FCT/74FCT240 is pin and functionally equivalent to IDT 54FCT/74FCT240
- Inverting TRI-STATE outputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (commercial), 48 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ

**Connection Diagrams** 

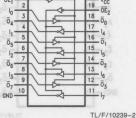
■ Military product compliant to MIL-STD 883 and standard military drawing #5962-87655

#### Ordering Code: See Section 8

#### **Logic Symbol**



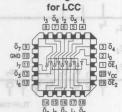




Pin Assignment

for DIP, Flatpak and SOIC

#### Pin Assignment for LCC



TL/F/10239-3

| Pin Names                             | Description                    |
|---------------------------------------|--------------------------------|
| $\overline{OE}_1$ , $\overline{OE}_2$ | TRI-STATE Output Enable Inputs |
| 10-17                                 | Inputs                         |
| $\overline{O}_0 - \overline{O}_7$     | Outputs                        |

#### **Truth Table**

| Inpu     | ts o   | Outputs               |  |  |
|----------|--------|-----------------------|--|--|
| OE1 I so |        | (Pins 12, 14, 16, 18) |  |  |
| L        | L 30 4 | Н                     |  |  |
| L        | H +0 + | L                     |  |  |
| Н        | X      | Z                     |  |  |

| Inpu | ts          | Outputs       |        |  |
|------|-------------|---------------|--------|--|
| OE2  |             | (Pins 3, 5, 7 | , 9)   |  |
| L    | noticina    | esti Hem      | all mi |  |
| L    | Hitugal ger | erbbA L       |        |  |
| Н    | Xatuonisi   | dena Z        |        |  |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTERM) 74FCT -0.5V to 7.0V 54FCT -0.5V to 7.0V Temperature under Bias (TBIAS) -55°C to +125°C -65°C to +135°C 74FCT 54FCT Storage Temperature (T<sub>STG</sub>) -55°C to +125°C 74FCT 54FCT ONV S MV -65°C to +150°C Power Dissipation (P<sub>T</sub>) negO stugtuO 0.5W 

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

## Recommended Operating

| Supply Voltage (V <sub>CC</sub> )           | specimed for the appropriate dewrite $\pm 1.252$ C, $V_{HC} = V_{CC} - 0.2V$ |
|---|--|
| 54FCT                                       | 4.5V to 5.5V   |
| 74FCT                                       | 4.75V to 5.25V   |
| Input Voltage                               | OV to V <sub>CC</sub>  |
| Output Voltage                              | 0V to V <sub>CC</sub>  |
| Operating Temperature (T                    | A) —55°C to +125°C   |
| 74FCT                                       | -0°C to +70°C  |
| Junction Temperature (T <sub>J</sub> ) CDIP | 175°C  |
| PDIP  | yloguð rewol lateT 140°C   |

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at  $V_{CC}=5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_{A}=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_{A}=-55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC}=V_{CC}-0.2V$ .

| Symbol           | Parameter SMO V                              | 54                            | FCT/74                        | FCT                            | Units           | Conditions  |   |
|------------------|--|-------------------------------|-------------------------------|--------------------------------|-----------------|---|---|
| Symbol           | raidilletei 6000 V                           | Min                           | Тур                           | Max                            |                 | Con   | ultions   |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                           | SI 28 USB (DEL                | 12020 210                      | V<br>1949 10 35 |   | Note 3: This parameter guarant<br>Note 8: Per TTL driven input (V                                       |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage              |                               | ipply calculi<br>guaranteed   | 0.8                            | oT al esu vi    |   | Note 4: This parameter is not di<br>Note 5: Values for these conditi                                    |
| l <sub>IH</sub>  | Input High Current                           |                               |                               | 5.0<br>5.0                     | μΑ              | V <sub>CC</sub> = Max   | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| IIL              | Input Low Current                            |                               |                               | -5.0<br>-5.0                   | μΑ              | V <sub>CC</sub> = Max   | $V_I = 0.5V$ (Note 2)<br>$V_I = GND$  |
| loz              | Maximum TRI-STATE Current                    |                               |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ              |   |   |
| VIK              | Clamp Diode Voltage                          |                               | -0.7                          | -1.2                           | ٧               | $V_{CC} = Min; I_N = -18$   | mA Sin sin sin sin sin sin sin sin sin sin s  |
| los              | Short Circuit Current                        | -60                           | -120                          | et conditions                  | mA              | V <sub>CC</sub> = Max (Note 1); V <sub>0</sub>  | O = GND   |
| V <sub>OH</sub>  | Minimum High Level                           | 2.8                           | 3.0                           |                                |                 | $V_{CC} = 3V; V_{IN} = 0.2V$  | or $V_{HC}$ ; $I_{OH} = -32 \mu A$  |
|                  | Output Voltage                               | V <sub>HC</sub><br>2.4<br>2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧               | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OH} = -300 \mu\text{A}$ $I_{OH} = -12 \text{mA} (\text{Mil})$ $I_{OH} = -15 \text{mA} (\text{Com})$ |
| V <sub>OL</sub>  | Maximum Low Level                            |                               | GND                           | 0.2                            |                 | $V_{CC} = 3V; V_{IN} = 0.2V$  | or $V_{HC}$ ; $I_{OL} = 300 \mu A$  |
|                  | Output Voltage                               |                               | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55            | V               | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OL} = 300 \mu A$ $I_{OL} = 48 \text{ mA (Mil)}$ $I_{OL} = 64 \text{ mA (Com)}$                      |
| lcc              | Maximum Quiescent<br>Supply Current          |                               | 0.001                         | 1.5                            | mA              | $\begin{aligned} &V_{CC} = \text{Max} \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V \\ &f_I = 0 \end{aligned}$ |   |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                               | 0.5                           | 2.0                            | mA              | $V_{CC} = Max$ $V_{IN} = 3.4V \text{ (Note 3)}$   |   |

|  | Parame  | eter   | 6  | Гур                | Max                                  | Units   | or Va.o -   | Cond   | ditions of foegas  |                                    |
|--|---|--|--|--------------------|--------------------------------------|---|---|--|--|------------------------------------|
| Iccd<br>Order +  | Dynamic Power Supply Current  | nt (Note 4)  | emperatus<br>emperatus   | 0.25               | 0.55                                 | mA/MHz  | V <sub>CC</sub><br>Outpool  | = Max uts Open = $\overline{OE}_B$ = GND nput Toggling Duty Cycle  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$   | SAFCI<br>Tempera<br>7AFCI<br>SAFCI |
| lc Coat  | Total Power S<br>Current (Note  |  |  |                    | 5.0                                  | 0.5W<br>0.5W<br>0.5W<br>0.5N<br>smage   | V <sub>CC</sub><br>Outpo<br>OE <sub>A</sub><br>f <sub>I</sub> =   | = Max uts Open = $\overline{OE}_B$ = GND   | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$ $V_{IN} = 3.4V$  | Power Di<br>BC Outp                |
|  |   |  |  | 1.8                | 8.0                                  | mA  | 50%<br>(Note  | Bit Toggling Duty Cycle  5)  Max   | $V_{IN} = GND$ $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$   | f leve sids                        |
|  | n as Max, uso<br>N ±10%, T <sub>A</sub>   |  |  |                    |                                      |   | Outp  | uts Open = $\overline{OE}_B$ = GND 2.5 MHz   | ratues are at Vo   | Typical v                          |
|  | enoblis   | neO  |  | 5.0                | 14.5                                 | TORATA  | Eight   | Bits Toggling Duty Cycle   | $V_{IN} = 3.4V$ $V_{IN} = GND$   |                                    |
| Note 2: Thi  | eximum test duration<br>is parameter guarant<br>or TTL driven input (V  | eed but not test   | ed.  |                    |                                      | e output shorte   | d at one tim  |  | Minimum High I   | HIV                                |
| Note 4: Thi  | is parameter is not di  | irectly testable, I  |  | -                  |                                      | Power Supply  | calculations.   |  |  |                                    |
|  | = IQUIESCENT + IN   |  |  | formu              | la. These I                          | imits are guara   | inteed but no   | t tested.  | Input Voltage  |                                    |
| Note 6: Ic   | = I <sub>QUIESCENT</sub> + I <sub>IN</sub><br>= I <sub>CC</sub> + ΔI <sub>CC</sub> D <sub>H</sub> N <sub>T</sub><br>= Quiescent Currer  | PUTS + IDYNAM<br>+ ICCD (fcp/2<br>nt   | + f <sub>I</sub> N <sub>I</sub> )                                |                    |                                      | imits are guara   | inteed but no   | t tested.  |  |                                    |
| Note 6: I <sub>C</sub> Ic Icc AIc DH   | = IQUIESCENT + IN<br>= ICC + AICC DHNT<br>= Quiescent Currer<br>= Power Supply C<br>= Duty Cycle for TT   | PUTS + IDYNAM + + ICCD (fCP/2 nt Current for a TTL TL Inputs High  | + f <sub>I</sub> N <sub>I</sub> )                                |                    | 3.4V)                                |   | inteed but no   | at tested.   | Input Voltage  |                                    |
| Note 6: Ic   | = I <sub>QUIESCENT</sub> + I <sub>IN</sub><br>= I <sub>CC</sub> + ΔI <sub>CC</sub> D <sub>H</sub> N <sub>T</sub><br>= Quiescent Currer<br>c <sub>C</sub> = Power Supply C   | PUTS + IDYNAM + + I <sub>CCD</sub> (f <sub>CP</sub> /2- nt Current for a TTL TL Inputs High at D <sub>H</sub> nt Caused by an for Register De  | High Input   | (V <sub>IN</sub> = | air (HLH or                          | 0.8<br>0.8<br>0.8-<br>0.8-  | inteed but no   | t tested.  | Input Voltage<br>Input High Quan   |                                    |
| Note 6: I <sub>C</sub> I <sub>C</sub> I <sub>C</sub> ΔI <sub>C</sub> DH  NT  I <sub>C</sub> f <sub>C</sub> f <sub>P</sub> N <sub>1</sub> All | = Iquiescent + Inn = Icc + AIcc D <sub>H</sub> N <sub>T</sub> = Quiescent Currer c = Power Supply C = Duty Cycle for T = Number of Inputs D = Dynamic Currer = Clock Frequency = Input Frequency = Number of Inputs currents are milliamp   | PUTS + IDYNAM + + ICCD (fcp/2- nt Current for a TTI TL Inputs High t at D <sub>H</sub> nt Caused by an for Register De at f <sub>I</sub> ss and all freque                           | High Input Input Transivices (Zero f                             | (V <sub>IN</sub> = | : 3.4V)<br>air (HLH or<br>n-Register | LHL)  |   | t tested.  | input Voltage<br>Input High Cum<br>Input Low Cum   |                                    |
| Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic   | = Iquiescent + Inn = Icc + ΔIcc D <sub>H</sub> N <sub>T</sub> = Quiescent Currer cc = Power Supply C = Duty Cycle for T = Number of Inputs D = Dynamic Currer = Clock Frequency = Input Frequency = Number of Inputs  | PUTS + IDYNAM + + ICCD (fcp/2 nt Current for a TTI TL Inputs High a t DH nt Caused by an for Register De at f <sub>I</sub> as and all freque 0 mA/MHz.                               | High Input Input Transivices (Zero f                             | (V <sub>IN</sub> = | air (HLH or<br>n-Register<br>ertz.   | O.B.<br>O.B.<br>LHL)<br>Devices)  |   | treeted.  tree   | Input Voltage Input High Cum Input Low Cum Maximum TRI-5   |                                    |
| Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic   | = Iquiescent + Inn = Icc + ΔIcc D <sub>H</sub> N <sub>T</sub> = Quiescent Currer c = Power Supply C = Duty Cycle for TT = Number of Inputs D = Dynamic Currer = Clock Frequency = Input Frequency = Number of Inputs currents are milliamp r 54FCT, Iccp = 0.4                                  | PUTS + IDYNAM + + ICCD (fcp/2 nt Current for a TTI TL Inputs High nt Caused by an for Register De at f <sub>I</sub> ss and all freque 0 mA/MHz. dard military dra                    | High Input Input Transi vices (Zero f                            | (VIN =             | air (HLH or<br>n-Register<br>ertz.   | Devices)  |   | treeted.  tree  tr | Input Voltage Input High Ours Input Low Gurs Maximum TRI-5 Clamp Diode Vi Short Circuit Cu             |                                    |
| Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic   | = IQUIESCENT + InN = ICC + ΔICC DHNT = Quiescent Currer C = Power Supply C = Duty Cycle for TT = Number of Inputs D = Dynamic Currer = Clock Frequency = Input Frequency = Number of Inputs currents are milliamp - 54FCT, ICCD = 0.4 er to applicable stan                                     | PUTS + IDYNAM r + ICCD (fcp/2 nt Current for a TTL IT Inputs High at DH nt Caused by an for Register De at fi us and all freque 0 mA/MHz, dard military dra                          | High Input Input Transi vices (Zero f                            | (VIN =             | air (HLH or<br>n-Register            | 0.8<br>0.8<br>0.8<br>0.8<br>LHL)<br>Devices)<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0. | I <sub>C</sub> /I <sub>CC</sub> limits  | trested.  Ine  Ine  Ine  Ine  Ine  Ine  Ine  In  | Input Voltage Input High Curr Input Low Curr Maximum TRI-5 Clamp Diode V                               |                                    |
| Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic   | = Iquiescent + Inn = Iqc + ΔIqc D <sub>H</sub> N <sub>T</sub> = Quiescent Currer <sub>ICC</sub> = Power Supply C = Duty Cycle for TT = Number of Inputs D = Dynamic Currer = Clock Frequency Input Frequency = Number of Inputs currents are milliamp - 54FCT, IqcD = 0.4 er to applicable stan | PUTS + IDYNAM r + ICCD (fcp/2 nt Current for a TTL ITL Inputs High at D <sub>H</sub> nt Caused by an for Register De at f <sub>1</sub> ps and all freque 0 mA/MHz. dard military dra | High Input Input Transi vices (Zero f                            | (V <sub>IN</sub> = | 3.4V) atir (HLH or n-Register leftz. | 0.8<br>0.8<br>0.8<br>0.8<br>LHL)<br>Devices)<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0.0<br>0. | lo/loc limits   | trested.  The trested tree tree tree tree tree tree tree t   | Input Voltage Input High Ours Input Low Gurs Maximum TRI-5 Clamp Diode Vi Short Circuit Cu             |                                    |
| Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic   | = Iquiescent + Inn = Iqc + ΔIqc D <sub>H</sub> N <sub>T</sub> = Quiescent Currer (C = Power Supply C = Duty Cycle for TT = Number of Inputs D = Dynamic Currer = Clock Frequency = Input Frequency = Number of Inputs currents are milliamp = 54FCT, IqcD = 0.4 er to applicable stan           | PUTS + IDYNAM + + ICCD (fcp/2 nt Current for a TTI TL Inputs High hat DH nt Caused by an for Register De at fi os and all freque 0 mA/MHz. dard military dra                         | High Input Input Transi vices (Zero f                            | (V <sub>IN</sub> = | 3.4V) air (HLH or n-Register leftz.  | Devices) Occonditions and   | 0-<br>lo/loc limits<br>8 8.5<br>9V OH<br>4 8.5<br>4 8.5   | trested.  The trested tree tree tree tree tree tree tree t   | Input Hilgh Curn Input Low Curn Maximum TRI-5 Clamp Diode VI Short Circuit Cu Minimum High I           |                                    |
| Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic   | = IQUIESCENT + InN = ICC + ΔICC DHNT = Quiescent Currer cc = Power Supply C = Duty Cycle for TT = Number of Inputs D = Dynamic Currer = Clock Frequency = Input Frequency = Number of Inputs currents are milliamp r 54FCT, ICCD = 0.4 er to applicable stan                                    | PUTS + IDYNAM  + ICCD (fcp/2  nt  Current for a TTI  TL Inputs High  at D <sub>H</sub> nt Caused by an  for Register De  at f <sub>I</sub> o mA/MHz.  dard military dra              | High Input Input Transi vices (Zero fincies are in inwing or NSC | (V <sub>IN</sub> = | 3.4V) air (HLH or n-Register leftz.  | 0.8<br>0.8<br>0.8<br>0.8<br>0.8<br>0.8<br>0.0<br>0.0<br>0.0<br>0.0  | lo/loc limits & 8.5 V OH! A A S.4 A A | STATE Current olkage  Level  Level   | Input Fligh Curn Input Low Curn Maximum TRI-5 Short Circuit Cu Minimum High Output Voltage Maximum Low |                                    |

0

#### AC Electrical Characteristics: See Section 2 for Waveforms

|  |   | 54FCT/74FCT                          | 74               | 4FCT                            | 54   | FCT        | Semio         |       |
|--|---|--------------------------------------|------------------|---------------------------------|--|------------|---------------|-------|
| Symbol                                     | Parameter   | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$ | R <sub>L</sub> = | C = Com<br>= 500Ω<br>= 50 pF    | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$ |            | Units         | Fig.  |
|  | Sutputs   | Тур                                  | Min<br>(Note 1)  | Max                             | Min  | Max        | it Butt       | oto O |
| t <sub>PLH</sub><br>t <sub>PHL</sub> -avia | Propagation Delay  D <sub>n</sub> to O <sub>n</sub> | TOS 0.5                              | 1.5              | 8.0<br>of bengaseb to           | 1.5<br>whb and br                                      | 9.0        | ns<br>ns      | 2-8   |
| t <sub>PZL</sub>                           | Output Enable Time                                  | NOT SECTIVATED NOTING 0.70-STATE     | i-nok1.5         | one revito doc<br>one a 10.0 rg | noin 1.5 evi   | ntibe your | ineriens bei  | 2-11  |
| t <sub>PHZ</sub>                           | Output Disable Timed                                | of 2000 gmsio                        | 1.5              | 9.5                             | 1.5  | 12.5       | a stilling of | 2-11  |

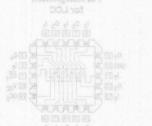
Note 1: Minimum limits are guaranteed but not tested on propagation delays.

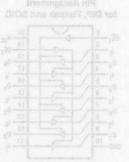
### Capacitance TA = +25°C, f = 1.0 MHz flourum Q22 w -req rollegue not suid bruising filique a of notifibbs ni reformos

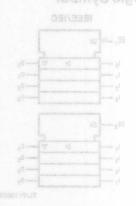
| Symbol           | Parameter (Note)   | Тур | Max | Units | Condition             |               |
|------------------|--------------------|-----|-----|-------|-----------------------|---------------|
| CIN              | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         | Ordering Code |
| C <sub>OUT</sub> | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |               |

Note: This parameter is measured at characterization but not tested.

C<sub>OUT</sub> for 74FCT only.







| 1 |  |  |
|---|--|--|
|   |  |  |
|   |  |  |
|   |  |  |

| Outputs           |  |
|-------------------|--|
| (Plns 3, 5, 7, 9) |  |
|                   |  |
|                   |  |
|                   |  |



## 54FCT/74FCT241 Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'FCT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

FACT<sup>TM</sup> FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

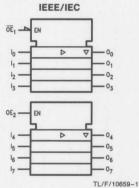
- NSC 54FCT/74FCT241 is pin and functionally equivalent to IDT 54FCT/74FCT241
- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (Com), 48 mA (Mil)

**Connection Diagrams** 

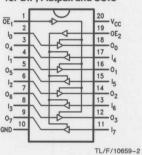
- CMOS power levels
- ESD immunity ≥4 kV typical
- Military product compliant to MIL-STD 883

Ordering Code: See Section 8

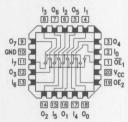
#### **Logic Symbol**



## Pin Assignment for DIP, Flatpak and SOIC



## Pin Assignment for LCC



TL/F/10659-3

## Description Truth Tables

| Pin<br>Names                   | Description                                 |
|--------------------------------|---|
| OE <sub>1</sub> ,              | TRI-STATE Output Enable Input               |
| OE <sub>2</sub>                | TRI-STATE Output Enable Input (Active HIGH) |
| I <sub>0</sub> -I <sub>7</sub> | Inputs                                      |
| O <sub>0</sub> -O <sub>7</sub> | Outputs                                     |

| Inpu            | its | Outputs               |
|-----------------|-----|-----------------------|
| OE <sub>1</sub> | 1   | (Pins 12, 14, 16, 18) |
| L               | L   | L                     |
| L               | Н   | Н                     |
| Н               | X   | Z                     |

| Inputs          |   | Outputs           |
|-----------------|---|-------------------|
| OE <sub>2</sub> | 1 | (Pins 3, 5, 7, 9) |
| Н               | L | L                 |
| Н               | Н | Н                 |
| L               | X | Z                 |

H = HIGH Voltage Level

X = Immaterial

L = LOW Voltage Level

Z = High Impedance

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTERM) -0.5V to 7.0V 74FCT 54FCT -0.5V to 7.0V

Temperature under Bias (TBIAS) 74FCT VS.0 2 MV -55°C to +125°C 54FCT -65°C to +135°C

Storage Temperature (T<sub>STG</sub>) -55°C to +125°C 74FCT 54FCT -65°C to +150°C 0.5W Power Dissipation (PT) DC Output Current (IOUT)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

#### Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>) 54FCT 4.5V to 5.5V 74FCT 4.75V to 5.25V Paremeter OV to Vcc Input Voltage OV to VCC Output Voltage Operating Temperature (TA) -55°C to +125°C 54FCT 74FCT -0°C to +70°C

Junction Temperature (T<sub>J</sub>)

CDIP 175°C PDIP 140°C

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ 

| Symbol           | Parameter                                    | 54                      | FCT/74                         | FCT                            | Units  | 6.8  | Conditions  |
|------------------|--|-------------------------|--------------------------------|--------------------------------|--------|--|---|
| Symbol           | Parameter eloy0 v                            | Min                     | Тур                            | Max                            | Oilito |  |   |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                     | У                              | m                              | V      | 20   | H Input Hysteresia on Clock Only  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           | ,86180 600              | o as usation                   | 0.8                            | V      | beteet )  beteet )  the alugar and of a              | Note 2: This parameter guaranteed but not<br>Note 2: Per TTL driven input (Ver ~ 3.4V)  |
| lн               | Input High Current                           | ensite<br>and not lie   | ilisələrə yilgə<br>Baetninində | 5.0<br>5.0                     | μΑ     | V <sub>CC</sub> = Max                                | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| I <sub>IL</sub>  | Input Low Current                            |                         |                                | -5.0<br>-5.0                   | μΑ     | V <sub>CC</sub> = Max                                | $V_1 = 0.5V \text{ (Note 2)}$<br>$V_1 = \text{GND}$   |
| loz              | Maximum TRI-STATE Current                    |                         |                                | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ     | solitions Transition                                 | $\begin{array}{c} V_O = V_{CC} \\ V_O = 2.7V \text{ (Note 2)} \\ V_O = 0.5V \text{ (Note 2)} \\ V_O = \text{GND} \end{array}$ |
| VIK              | Clamp Diode Voltage                          |                         | -0.7                           | -1.2                           | ٧      | V <sub>CC</sub> = Min; I <sub>N</sub>                | = -18 mAn ni ere almento IIA  |
| los              | Short Circuit Current                        | -60                     | -120                           | enpillorioo ta                 | mA     | V <sub>CC</sub> = Max (N                             | lote 1); V <sub>O</sub> = GND   |
| V <sub>OH</sub>  | Minimum High Level                           | 2.8                     | 3.0                            |                                |        | $V_{CC} = 3V; V_{IN}$                                | $_{\rm I} = 0.2 \rm V \ or \ V_{HC}; I_{OH} = -32 \ \mu A$  |
|                  | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3  |                                | ٧      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V$       | $I_{OH} = -300 \mu\text{A}$ $I_{OH} = -12 \text{mA (Mil)}$ $I_{OH} = -15 \text{mA (Com)}$                                     |
| VoL              | Maximum Low Level                            |                         | GND                            | 0.2                            |        | $V_{CC} = 3V; V_{IN}$                                | $_{I}$ = 0.2V or $V_{HC}$ ; $I_{OL}$ = 300 $\mu A$  |
|                  | Output Voltage                               |                         | GND<br>0.3<br>0.3              | 0.2<br>0.55<br>0.55            | ٧      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V$       | $I_{OL} = 300 \mu A$ $I_{OL} = 48 \text{ mA (Mil)}$ $I_{OL} = 64 \text{ mA (Com)}$  |
| Icc              | Maximum Quiescent<br>Supply Current          |                         | 0.001                          | 1.5                            | mA     | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN}$ $f_I = 0$ | v ≤ 0.2V  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                            | 2.0                            | mA     | $V_{CC} = Max$ $V_{IN} = 3.4V$ (No                   | ote 3)  |

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55$ °C to +125°C,  $V_{HC}=V_{CC}-0.2V$ 

| Symbol                     | Parameter  | 74FC        | 74F(T | Units          | MASTV) CIVID of toegee  | MASTY) CIVID of respect filly egation lanimat Conditions |  |  |
|----------------------------|--|-------------|-------|----------------|---|--|--|--|
| Symbol                     |  | Min Typ Max |       | VOX of         | /8.0- Conditions  |  |  |  |
| CCD<br>O'CST 4<br>O'OV 4 O | Dynamic Power<br>Supply Current (Note 4)                                 | 0.25        | 0.55  | mA/MHz         | $V_{CC} = Max$ Outputs Open $\overline{OE}_A = \overline{OE}_B = GND$ One Input Toggling 50% Duty Cycle | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$                    |  |  |
| 140°GI                     | Total Power Supply<br>Current (Note 6)                                   | 1.5         | 5.5   | VS.0<br>Am 0SI | $V_{CC} = Max$ Outputs Open $\overline{OE}_A = \overline{OE}_B = GND$                                   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                 |  |  |
|                            |  | 1.8         | 6.0   | mA             | f <sub>I</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND          |  |  |
|                            | tons shown as Max, use to V <sub>CC</sub> = 8.0V ± 10%, T <sub>A</sub> = |             |       | nily Devi      | (Note 5)<br>$V_{CC} = Max$<br>Outputs Open<br>$\overline{OE}_A = \overline{OE}_B = GND$                 |  |  |  |
|                            | Conditions   | 5.0         | 14.5  | ST/74FCT       | f <sub>I</sub> = 2.5 MHz<br>Eight Bits Toggling<br>50% Duty Cycle                                       | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND          |  |  |
| V <sub>H</sub>             | Input Hysteresis<br>on Clock Only  | 200         | V     | mV             | Level 2.0   | Alle Minimum High  |  |  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   $I_{CC} = Quiescent Current$ 

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>1</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I<sub>CCD</sub> = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I<sub>C</sub>/I<sub>CC</sub> limits.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  | 54FCT/74FCT   |                                      | T <sub>A</sub> = +25°C  T <sub>A</sub> , V <sub>CC</sub> = Com R <sub>1</sub> = 5000 |     | $\begin{array}{c} \textbf{54FCT} \\ \textbf{T_A, V_{CC} = Mil} \\ \textbf{R_L = 500} \Omega \\ \textbf{C_L = 50 pF} \end{array}$ |      | Units  | Fig. |
|------------------|---|--------------------------------------|--|-----|--|------|--------|------|
| Symbol Parameter |   | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$ |  |     |  |      |        |      |
|                  | utputs  | Тур                                  | Min (Note 1)   | Max | Min  | Max  | tu8 te | Jot! |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 4.0                                  | 1.5  | 6.5 | 1.5  | 9.0  | ns     | 2-8  |
| t <sub>PZH</sub> | Output Enable Time                                    | # 45.5 AFOT                          | a DSM as of b  | 8.0 | 1.5 2601   | 12.5 | ns     | 2-10 |
| t <sub>PHZ</sub> | Output Disable Time                                   | 4.5                                  | 1.5  | 7.0 | 1.5  | 11.5 | ns     | 2-10 |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

#### 

| Symbol                   | Parameter (Note)   | Тур            | Max | Units | Conditions            |
|--------------------------|--------------------|----------------|-----|-------|-----------------------|
| C <sub>IN</sub> at a bas | Input Capacitance  | y pro6uct c    | 10  | pF    | $V_{IN} = 0V$         |
| C <sub>OUT</sub>         | Output Capacitance | warb a stillin | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

Cout for 74FCT only.

Connection Diagrams







|  | JIST TREATE |  |
|--|-------------|--|
|  |             |  |
|  |             |  |
|  |             |  |
|  |             |  |
|  |             |  |
|  |             |  |

| Description |  |
|-------------|--|
|             |  |
|             |  |
|             |  |



## 54FCT/74FCT244 Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'FCT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT and GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- NSC 54FCT/74FCT244 is pin and functionally equivalent to IDT 54FCT/74FCT244
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections

Electrical Characteristics: See Section 2 for Waveforms

- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (commercial) and 48 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883C and standard military drawing #5962-87630

#### Ordering Code: See Section 8

#### **Logic Symbol**

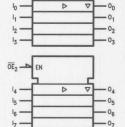
**Pin Names** 

OE<sub>1</sub>, OE<sub>2</sub>

10-17

00-07

# IEEE/IEC



TL/F/10240-1

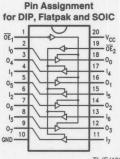
Inputs

Outputs

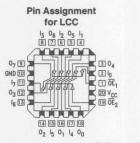
Description

TRI-STATE Output Enable Inputs

### **Connection Diagrams**



TL/F/10240-2



TL/F/10240-3

#### **Truth Tables**

| Inpu            | its    | Outputs               |  |
|-----------------|--------|-----------------------|--|
| OE <sub>1</sub> | puts I | (Pins 12, 14, 16, 18) |  |
| L               | L      | L                     |  |
| L               | Н      | Н                     |  |
| Н               | X      | Z                     |  |

| Inpu              | ts | Outputs           |
|-------------------|----|-------------------|
| $\overline{OE}_2$ | 1  | (Pins 3, 5, 7, 9) |
| L                 | L  | L                 |
| L                 | Н  | Н                 |
| Н                 | X  | Z                 |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

| 74FCT          | 4.75V to 5.25V        |
|----------------|-----------------------|
| nput Voltage   | 0V to V <sub>CC</sub> |
| Output Voltage | 0V to V <sub>CC</sub> |

| and the same of the same of |             |         |
|-----------------------------|-------------|---------|
| Operating                   | Temperature | $(T_A)$ |

| Operating remperature (1A) |                 |
|----------------------------|-----------------|
| 54FCT                      | -55°C to +125°C |
| 74FCT                      | -0°C to +70°C   |

| Storage Temperature (TSTG) |                |
|----------------------------|----------------|
| 74FCT                      | -55°C to +125° |
| 54FCT                      | -65°C to +150° |

Terminal Voltage with Respect to GND (VTERM)

Temperature under Bias (T<sub>BIAS</sub>) 74FCT VS.0 ≥ MV

54FCT

74FCT

54FCT

| 74FCT                               | -55°C to +125°C | Junction Ten |
|-------------------------------------|-----------------|--------------|
| 54FCT                               | -65°C to +150°C | CDIP         |
| Power Dissipation (P <sub>T</sub> ) | xat4 = 55V 0.5W | PDIP         |
|                                     |                 |              |

-0.5V to 7.0V

-0.5V to 7.0V

-55°C to +125°C

-65°C to +135°C

| DC Output Current (IOUT)  |
|---|
| Note 1: Absolute maximum ratings are those values beyond which damage       |
| to the device may occur. Exposure to absolute maximum rating conditions     |
| for extended periods may affect reliability. The databook specifications    |
| should be met, without exception, to ensure that the system design is reli- |

able over its power supply, temperature, and output/input loading variables.

| Junction Temperature (T <sub>J</sub> ) |                      |      |
|--|----------------------|------|
| CDIP                                   | 1                    | 75°C |
| PDIP                                   | 1 Total Power Supply | 40°C |

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55^{\circ}C$ to + 125°C. VHC = VCC - 0.2V

| Symbol           | Parameter Parameter                          | 54                      | FCT/74                        | FCT                            | Units    | 3   | Conditions   |
|------------------|--|-------------------------|-------------------------------|--------------------------------|----------|---|--|
| Symbol           | y Cycle                                      | Min                     | Тур                           | Max                            | Ointo    | Conditions  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                     | V                             |                                | V        | 03.   |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           | and en                  | o la benori                   | 0.8                            | V        | to expect one second, not but not tested.  2.4VG ell other incide at 1.                         | Note 1: Maximum lest duration nor<br>Note 2: This parameter gueranteed<br>Note 3: Per TTL driven land Muse |
| l <sub>IH</sub>  | Input High Current                           |                         | ipply calcul<br>gurusnteed    |                                | μΑ       | V <sub>CC</sub> = Max   | $V_{I} = V_{CC}$ $V_{I} = 2.7V \text{ (Note 2)}$   |
| IL               | Input Low Current                            |                         |                               | -5.0<br>-5.0                   | μΑ       | V <sub>CC</sub> = Max   | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND   |
| loz              | Maximum TRI-STATE Current                    |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ       | 116   | $V_D = V_{CC}$ $V_D = 2.7V \text{ (Note 2)}$ $V_D = 0.5V \text{ (Note 2)}$ $V_D = GND$                     |
| VIK              | Clamp Diode Voltage                          |                         | -0.7                          | -1.2                           | st V gos | $V_{CC} = Min; I_N = -18 \text{ mA}$  |  |
| los              | Short Circuit Current                        | -60                     | -120                          | anoifibren fa                  | mA       | V <sub>CC</sub> = Max (Note 1   | ); V <sub>O</sub> = GND  |
| V <sub>OH</sub>  | Minimum High Level                           | 2.8                     | 3.0                           |                                |          | $V_{CC} = 3V; V_{IN} = 0.$  | .2V or $V_{HC}$ ; $I_{OH} = -32 \mu A$   |
|                  | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧        | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$   | 011  |
| V <sub>OL</sub>  | Maximum Low Level                            |                         | GND                           | 0.2                            | 7.1      | $V_{CC} = 3V; V_{IN} = 0.$  | .2V or $V_{HC}$ ; $I_{OL}=300~\mu A$   |
|                  | Output Voltage                               |                         | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55            | ٧        | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OL}=300~\mu A$<br>$I_{OL}=48~mA~(Mil)$<br>$I_{OL}=64~mA~(Com)$   |
| lcc              | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                            | mA       | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0 \\ &f_I = 0 \end{aligned}$ | .2V  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                            | mA       | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)  |  |

DC Characteristics for 'FCT Family Devices (Continued) Typical values are at  $V_{CC}=5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC}=V_{CC}-0.2V$ 

|  | Paramete  | 74   | 74FCT  |   | Jnits of                                   | (MRSV) QVD of begaeR ritiv egstoV<br>78.0— Conditions<br>78.0— |   |  | 54FCT<br>74FCT                           |
|--|---|--|--|---|--|--|---|--|--|
| Symbol   | raramete  | 200  | Гур М  | Max Vo.To   |  |  |   | itions                                   |  |
| 000<br>000<br>0 + 125°C  | Dynamic Power<br>Supply Current (   |  | 0.15   |   | A/MHz                                      |  | Open DE <sub>2</sub> = GND                | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$    |  |
| 175°C  |   | (LT) eruteracum  | netion Te<br>CBIP  | WL .  | + 125°C                                    | 50% Du   |   |  | 74FCT                                    |
| Total Power Supply Current (Note 6)  |   |  | 1.5 5  | 5.5   | 0.5W<br>120 mA                             | $V_{CC} = N$ Outputs $\overline{OE}_1 = \overline{0}$          |   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$ | Power Dis<br>DC Outpu                    |
|  |   |  | 1.8 6  | conditions | soffications<br>sign is roll-<br>verables. | f <sub>I</sub> = 10 MHz One Bit Toggling 50% Duty Cycle        |   | $V_{IN} = 3.4V$ $V_{IN} = GND$           |  |
| eulay art<br>Oraa – a  |   | r tast concilons sho<br>> +70°C; Mil: Voc =  |  |   | MA -                                       | Outputs  | Max<br>Open<br>DE <sub>2</sub> = GND      |  |  |
|  | anolillano  | э .  | 5.0 alinu  | 4.5   | CT/78FC                                    | f <sub>1</sub> = 2.5   | MHz<br>s Toggling                         | $V_{IN} = 3.4V$ $V_{IN} = GND$           | lodmy                                    |
| /н   | Input Hysteresis<br>on Clock Only   | 2  | 200  |   | mV   | 0.9  | leva_l                                    | Minimum High                             | HI                                       |
| Note 1: Ma   | ximum test duration not   | to exceed one second, n  | ot more tha  | in one outpu  | it shorted at                              | one time.  |   |  |  |
| Note 2: This   | s parameter guaranteed  |  |  |   |  |  |   |  | 3  |
| Note 2: This<br>Note 3: Per<br>Note 4: This  | s parameter guaranteed<br>TTL driven input (V <sub>IN</sub><br>s parameter is not direc   | d but not tested.  | t V <sub>CC</sub> or GN<br>I for use in  | ND.<br>Total Power  | Supply calc                                | culations.   |   |  | -  |
| Note 2: This<br>Note 3: Per<br>Note 4: This<br>Note 5: Val<br>Note 6: Ic                           | s parameter guaranteed TTL driven input (V <sub>IN</sub> s parameter is not direct ues for these conditions =   <sub>QUIESCENT</sub> +   <sub>INPUT</sub> =   <sub>CC</sub> + $\Delta$   <sub>CC</sub> D <sub>H</sub> N <sub>T</sub> + = Quiescent Current  | d but not tested.  3.4V); all other inputs a style testable, but is derived as are examples of the I <sub>CC</sub> are examples of the I <sub>CC</sub> I <sub>CCD</sub> (f <sub>CP</sub> /2 + f <sub>1</sub> N <sub>1</sub> )  | t V <sub>CC</sub> or GN<br>I for use in formula. Th  | ND.<br>Total Power<br>nese limits ar  | Supply calc                                | culations.   | sted.                                     |  | b  |
| Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic = Ic = Ic = AIc DH NT Iccc fcP fi =   | s parameter guaranteed TTL driven input (V <sub>IN</sub> s parameter is not direct uses for these condition: =   QuiesCent +   Inpu'  =   QC + A  QC D  NT +   = Quiescent Current C = Power Supply Cur = Duty Cycle for TTL   = Number of Inputs at D = Dynamic Current C D = Clock Frequency for Input Frequency  | d but not tested.  = 3.4V); all other inputs a stity testable, but is derived as are examples of the Icc rs + IDYNAMIC IccD (fcp/2 + f <sub>1</sub> N <sub>1</sub> ) rent for a TTL High Input inputs High.  DH  aussed by an Input Transit r Register Devices (Zero for   | t V <sub>CC</sub> or GN<br>I for use in formula. The<br>V <sub>IN</sub> = 3.4V   | ND. Total Power nese limits and   | Supply calc                                | culations.   | sted.                                     |  | 8  |
| Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic = Icc DH NT Icci fcp fi = Ni          | s parameter guaranteer TTL driven input (V <sub>IN</sub> s parameter is not direct uses for these conditions  | d but not tested.  = 3.4V); all other inputs a stity testable, but is derived as are examples of the Icc rs + IDYNAMIC IccD (fcp/2 + f <sub>1</sub> N <sub>1</sub> ) rent for a TTL High Input inputs High.  DH  aussed by an Input Transit r Register Devices (Zero for   | t V <sub>CC</sub> or GN<br>I for use in formula. The<br>V <sub>IN</sub> = 3.4v<br>ion Pair (HL<br>or Non-Reg                                     | ND. Total Power nese limits an  ()  LH or LHL) ister Devices  | Supply calc                                | culations.   | sted.  me STATE Gurrant                   |  | 20                                       |
| Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =  | s parameter guaranteed: TTL driven input (V <sub>IN</sub> s parameter is not directuse for these condition: =  coc + A cc D <sub>H</sub> NT +   HNPU' =  cc + A cc D <sub>H</sub> NT +   Quiescent Current C = Power Supply Cun = Duty Cycle for TTL   Number of Inputs at D = Dynamic Current C = Clock Frequency for Input Frequency   Number of Inputs at D = Dynamic Current C = Clock Frequency   Number of Inputs at Durrents are in milliampic Surrents are in milliampic 54FCT,  ccD = 0.40 m   | d but not tested.  = 3.4V); all other inputs a stity testable, but is derived as are examples of the I <sub>CC</sub> is a re-example of the I <sub>CC</sub> is a re-example of the I <sub>CC</sub> is a re-example of the I <sub>CC</sub> (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T <sub>CC</sub> ) (T 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| Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I | s parameter guaranteed: TTL driven input (V <sub>IN</sub> s parameter is not directues for these condition: =  cc + A cc D <sub>H</sub> NT +   = Quiescent Current   C = Power Supply Cun   = Number of Inputs at   D = Dynamic Current   C = Dynamic Current     Number of Inputs at     Clock Frequency for     Input Frequency     Number of Inputs at     Supple     S | d but not tested.  3.4V); all other inputs a city testable, but is derived as are examples of the I <sub>CC</sub> rs + I <sub>DYNAMIC</sub> I <sub>CCD</sub> (f <sub>CP</sub> /2 + f <sub>1</sub> N <sub>1</sub> ) rent for a TTL High Input inputs High DH caused by an Input Transit r Register Devices (Zero fins and all frequencies are installed.  | t V <sub>CC</sub> or GN I for use in formula. The V <sub>IN</sub> = 3.4V Ion Pair (HL or Non-Reg   | ND. Total Power less limits au  /) LH or LHL) ister Devices   | Supply calc                                | culations.   | STATE Current voltage                     |  | 20<br>Z0                                 |
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| Note 2: Thi Note 3: Per Note 4: Thi Note 5: Val Note 6: Ic :    | s parameter guaranteed: TTL driven input (VIN s parameter is not directure to the secondition: I a louisescent + Input   I continue to the secondition: I continue to the secondition: I continue to the secondition: I continue to the secondition: I continue to the secondition to t                      | d but not tested.  = 3.4V); all other inputs a stity testable, but is derived as are examples of the I <sub>CC</sub> is a re-example of the I <sub>CC</sub> is a re-example of the I <sub>CC</sub> (Cp/2 + f <sub>1</sub> N <sub>1</sub> ) rent for a TTL High Input inputs High DH caused by an Input Transit Pagister Devices (Zero fifs and all frequencies are in A/MHz. id military drawing or NSC  | t V <sub>CC</sub> or GN<br>I for use in 'i<br>formula. Th<br>V <sub>IN</sub> = 3.4V<br>ion Pair (HL<br>or Non-Reg<br>in megahert:<br>Table I for | ND. Total Power lesse limits au  ()  H or LHL) lister Devices z.  | Supply calcine guarantee                   | cc limits.   | STATE Gurrent STATE Gurrent Level         |  | NO NO                                    |
| Note 2: Thi Note 3: Per Note 4: Thi Note 5: Val Note 6: Ic: Ic: Alc Alc Alc Note 7: For Refi       | s parameter guaranteed: TTL driven input (VIN s parameter is not directure to the secondition of the secondi                      | d but not tested.  = 3.4V); all other inputs a stity testable, but is derived as are examples of the I <sub>CC</sub> rs + I <sub>D</sub> YNAMIC I <sub>CCD</sub> (fcp/2 + f <sub>1</sub> N <sub>1</sub> ) rent for a TTL High Input inputs High DH caused by an Input Transit Register Devices (Zero fifs and all frequencies are in nA/MHz.  d military drawing or NSC  | t V <sub>CC</sub> or GN<br>for use in 'formula. The<br>V <sub>IN</sub> = 3.4V<br>tion Pair (HL<br>or Non-Reg<br>n megahert:<br>Table I for       | ND. Total Power lesse limits au  () O.O. H. or L.H.D. ister Devices z. test condition   | Supply calcine guarantee                   | ed but not te  | STATE Gurrent STATE Gurrent College Levei |  | ) де де де де де де де де де де де де де |

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |   | 54FCT/74FCT                                      | 74FCT  | 54FCT  | Units | Fig.<br>No. |
|------------------|---|--|--|--|-------|-------------|
| Symbol           | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | $T_A$ , $V_{CC} = Com$<br>$R_L = 500\Omega$<br>$C_L = 50 pF$ | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$ |       |             |
|                  |   | Тур  | Min (Note 1) Max   | Min Max  |       |             |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 4.5  | 1.5 6.5  | 1.5 9.0  | ns    | 2-8         |
| t <sub>PZH</sub> | Output Enable Time                                    | 6.0  | 1.5 8.0  | 1.5 10.5   | ns si | 2-11        |
| t <sub>PHZ</sub> | Output Disable Time                                   | 4FCT/7 0.6 T245                                  | erdi e 1.5 - Hud isnot en 7.0 er                             | 1.5 12.5   | ns ns | 2-11        |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

#### Capacitance ( $T_A = +25^{\circ}C$ , f = 1.0 MHz)

| Symbol           | Parameter (Note)   | Тур | Max | Units           | Conditions            | ports to A ports. The Out |
|------------------|--------------------|-----|-----|-----------------|-----------------------|---------------------------|
| CIN              | Input Capacitance  | 6   | 10  | pF              | V <sub>IN</sub> = 0V  | dion.                     |
| C <sub>OUT</sub> | Output Capacitance | 8   | 12  | and application | V <sub>OUT</sub> = 0V | FACTIM FOT utilizes NSC   |

Note: This parameter is measured at characterization but not tested. C<sub>OUT</sub> for 74FCT only.

Som gh 82-4-4-



### 54FCT/74FCT245 **Octal Bidirectional Transceiver** with TRI-STATE® Inputs/Outputs

#### **General Description**

The 'FCT245 contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condi-

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- NSC54FCT/74FCT245 is pin and functionally equivalent to IDT54FCT/74FCT245
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity.
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- IOI = 64 mA (commercial) and 48 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and Standard Military Drawing #5962-87629

Ordering Code: See Section 8

#### **Logic Symbols**

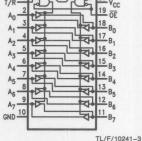


| Pin<br>Names                   | Description  |
|--------------------------------|--|
| ŌĒ                             | Output Enable Input                                |
| T/R                            | Transmit/Receive Input                             |
| A <sub>0</sub> -A <sub>7</sub> | Side A TRI-STATE<br>Inputs or TRI-STATE<br>Outputs |
| B <sub>0</sub> -B <sub>7</sub> | Side B TRI-STATE<br>Inputs or TRI-STATE<br>Outputs |

## EN1 (BA) EN2 (AB) 4 2 7 A2

IEEE/IEC

TL/F/10241-2



**Connection Diagrams** 

**Pin Assignment** for DIP, Flatpak and SOIC

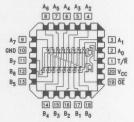
#### **Truth Table**

| Inp | uts | Outputs             |  |  |  |
|-----|-----|---------------------|--|--|--|
| ŌĒ  | T/R | Outputs             |  |  |  |
| L   | L   | Bus B Data to Bus A |  |  |  |
| L   | Н   | Bus A Data to Bus B |  |  |  |
| Н   | X   | HIGH-Z State        |  |  |  |

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

#### **Pin Assignment** for LCC and PCC



TL/F/10241-4

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Terminal Voltage with Respect 54FCT 74FCT                                 | t to GND (V <sub>TERM</sub> )<br>-0.5V to 7.0V<br>-0.5V to 7.0V |
|---|---|
| Temperature under Bias (T <sub>BIA</sub><br>74FCT<br>54FCT                | -55°C to +125°C<br>-65°C to +135°C                              |
| Storage Temperature (T <sub>STG</sub> )<br>74FCT<br>54FCT                 | -55°C to +125°C<br>-65°C to +150°C                              |
| Power Dissipation (P <sub>T</sub> ) DC Output Current (I <sub>OUT</sub> ) | 0.5W  |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

## Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> ) | to + 125°C, VHC = VCC - 0.2V.   |
|-----------------------------------|---------------------------------|
| 54FCT                             | 4.5V to 5.5V                    |
| 74FCT                             | 4.75V to 5.25V                  |
| Input Voltage                     | 0V to V <sub>CC</sub>           |
| Output Voltage                    | megaelu O mumakelu OV to VCC    |
| Operating Temperature             |                                 |
| 54FCT                             | -55°C to +125°C                 |
| 74FCT                             | 0°C to +70°C                    |
| Junction Temperature              | Algo Cuiescent Supply Curr (LT) |
| CDIP                              | HOIH eaught JTT 175°C           |
| PDIP                              | 140°C                           |
|                                   |                                 |

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55$ °C to +125°C,  $V_{HC}=V_{CC}-0.2V$ .

| Symbol          | Parameter                              | 54                      | FCT/74                        | FCT                            | Units            |  | onditions  |
|-----------------|--|-------------------------|-------------------------------|--------------------------------|------------------|--|--|
| Syllibol        | ONV S Marameter                        | Min                     | Тур                           | Max                            | Onits            | Conditions   |  |
| V <sub>IH</sub> | Minimum High Level Input Voltage       | 2.0                     |                               |                                | ٧                |  |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage        | fi = 2.1<br>Eight B     |                               | 0.8                            | V <sub>0.8</sub> |  |  |
| l <sub>IH</sub> | Input High Current (except I/O Pins)   | G %69                   | None.                         | 5.0<br>5.0                     | μΑ               | V <sub>CC</sub> = Max  | $V_I = V_{CC}$ $V_I = 2.7V \text{ (Note 2)}$                                       |
| I <sub>IH</sub> | Input High Current<br>(I/O Pins Only)  | ne time.                | o to befroit                  | 15<br>10015                    | μА               | V <sub>CC</sub> = Max  | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$                                    |
| I <sub>IL</sub> | Input Low Current<br>(except I/O Pins) | enoite                  | toolao vieta                  | -5.0<br>-5.0                   | μΑ               | V <sub>CC</sub> = Max  | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$                                |
| I <sub>IL</sub> | Input Low Current<br>(I/O Pins Only)   | et lon tud              | guarantaeu                    | -15<br>-15                     | μA               | V <sub>CC</sub> = Max  | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$                                |
| loz             | Maximum TRI-STATE Current              |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | pur.             | V <sub>CC</sub> = Max<br>V) mend not 4 ut a so then<br>right sound<br>p(0) | $V_1 = 0.5V \text{ (Note 2)}$  |
| VIK             | Clamp Diode Voltage                    |                         | -0.7                          | -1.2                           | V                | $V_{CC} = Min; I_N = -1$   | 18 mA respect tuget = 1  |
| los             | Short Circuit Current                  | -60                     | -120                          |                                | mA               | V <sub>CC</sub> = Max (Note 1);  | $V_0 = GND$  |
| V <sub>OH</sub> | Minimum High Level                     | 2.8                     | 3.0                           |                                | it vot Léida     | $V_{CC} = 3V; V_{IN} = 0.2$  | $2V \text{ or } V_{HC}; I_{OH} = -32 \mu\text{A}$                                  |
|                 | Output Voltage                         | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 | January 140                    | ٧                | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$                        | $I_{OH}=-300~\mu A$<br>$I_{OH}=-12~m A~(Mil)$<br>$I_{OH}=-15~m A~(Com$             |
| V <sub>OL</sub> | Maximum Low Level                      |                         | GND                           | 0.2                            |                  | $V_{CC} = 3V; V_{IN} = 0.2$  | 2V or V <sub>HC</sub> ; I <sub>OL</sub> = 300 μA                                   |
|                 | Output Voltage                         |                         | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55            | V                | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$                        | $I_{OL} = 300 \mu A$ $I_{OL} = 48 \text{ mA (Mil)}$ $I_{OL} = 64 \text{ mA (Com)}$ |

#### DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to  $+125^{\circ}$ C. VHC = VCC -0.2V.

| Symbol                 | Parameter  | 74FC        | 747  | Units   | Conditions  |   |                           |
|------------------------|--|-------------|------|---------|---|---|---------------------------|
| goV at VD              |  | Min Typ Max |      | 0-      |   |   |                           |
| lcc O'ast+             | Maximum Quiescent<br>Supply Current                              | 0.001       | 1.5  | mA +    | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V \\ &f_I = 0 \end{aligned}$      |   | Tempera<br>74FGT<br>54FGT |
| Δlcc                   | Quiescent Supply Current;<br>TTL Inputs HIGH                     | 0.5         | 2.0  | mA      | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)  |   | Storage<br>74FCT<br>54FCT |
| ICCD                   | Dynamic Power<br>Supply Current (Note 4)                         | 0.25        | 0.40 | mA/MHz  | $V_{CC} = Max$ Outputs Open $\overline{OE}_A = \overline{OE}_B = GND$ One Input Toggling 50% Duty Cycle | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$           |                           |
| lc                     | Total Power Supply<br>Current (Note 6)                           | 1.5         | 4.5  | mily De | V <sub>CC</sub> = Max<br>Outputs Open<br>T/R = OE = GND   | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$           | DC C                      |
|                        | conditions shown as Max, use I<br>*C. Mil: Voc = 5.0V ±10%, TA = |             |      |         | f <sub>I</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND |                           |
|                        | Conditions   | 3.0         | 10.0 | Typ N   | (Note 5)  V <sub>CC</sub> = Max  Outputs Open  T/R = OE = GND   | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$           | , lodno                   |
|                        | ooV = VV   | 5.0         | 14.5 | 0       | f <sub>I</sub> = 2.5 MHz Eight Bits Toggling 50% Duty Cycle   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND | ,                         |
| V <sub>H</sub> (S etc. | Input Hysteresis<br>on Clock Only                                | 200         | 0    | mV      | (8)   | (except I/O Pin                                 |                           |

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

IC = ICC + AICC DHNT + ICCD (fcp/2 + fl Ni)
ICC = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

Voc = Min

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I<sub>CCD</sub> = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I<sub>C</sub>/I<sub>CC</sub> limits.

| Symbol                               | Parameter                           | V <sub>CC</sub> = 5.0V  | _                | = 500Ω<br>= 50 pF   | 475 000  | 500Ω<br>50 pF     | Units                  | No.  |
|--------------------------------------|-------------------------------------|---|------------------|---------------------|----------|-------------------|------------------------|------|
|                                      | Тур                                 | Min (Note   | ) Max            | Min                 | Max      | a a la            | oct:                   |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>A to B, B to A | 5.0   | 1.5              | 7.0                 | 1.5      | 7.5               | ns                     | 2-8  |
| t <sub>PZH</sub>                     | Output Enable Time OE to A or B     | uffer for 0.60S micro   | 1.5              | Www.eq.9.5          | 7.5 eg   | 10.0              | eans 72                | 2-8  |
| t <sub>PHZ</sub>                     | Output Disable Time OE to A or B    | d common clock<br>0.0<br>d, seynchronous m  | nefluS<br>nefluS | 7.5                 | 1.5      | 10.0              | M bas (9)<br>equipment | 2-11 |
| t <sub>PZH</sub>                     | Output Enable Time                  | level fuction on the tuck seed out to the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of the tuck of t | 1.5              | -nsi di dossi lo si | H-o.1.50 | 10.0              | mit ns ea              | 2-11 |
| t <sub>PHZ</sub>                     | Output Enable Time                  | nig at 6.0 DRAT\a   | 0 0 8 / 1.5      | 7.5                 | 1.5      | 10.0<br>WOJ 56000 | ns<br>ed ilw ab        | 2-11 |

Note: Minimum limits guaranteed but not tested on propagation delays.

#### Capacitance TA = +25°C, f = 1.0 MHz

| Symbol           | Parameter (Note)   | Тур | Max | Units | Conditions            |               |
|------------------|--------------------|-----|-----|-------|-----------------------|---------------|
| CIN              | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         | rdering Gode. |
| C <sub>OUT</sub> | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V | aladeau2 ainc |

Note: This parameter is measured at characterization but not tested.

Cour for 74FCT245 only.



### 54FCT/74FCT273 Octal D Flip-Flop

#### **General Description**

The 'FCT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q out-

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

#### **Features**

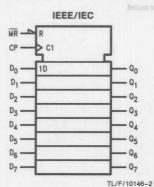
- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- Buffered common clock
- Buffered, asynchronous master reset
- TTL input and output level compatible
- TTL levels accept CMOS levels
- IOI = 48 mA (Com), 32 mA (Mil)
- NSC 54/74FCT273 is pin and functionally equivalent to IDT 54/74FCT273

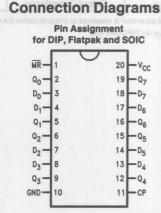
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Ordering Code: See Section 8

**Logic Symbols** 

# Q1 Q2 Q3 Q4 Q5 Q6 Q-TL/F/10146-1





20

19 -Q7

18

16 -Q6

15 -Q5

14 -D<sub>5</sub>

13 -D4

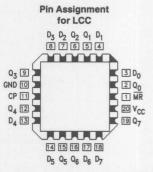
12

-D7

-Q<sub>4</sub>

TL/F/10146-3

| Pin Names                      | Description       |  |  |
|--------------------------------|-------------------|--|--|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs       |  |  |
| MR                             | Master Reset      |  |  |
| CP                             | Clock Pulse Input |  |  |
| Q <sub>0</sub> -Q <sub>7</sub> | Data Outputs      |  |  |



TL/F/10146-4

#### Mode Select-Function Table

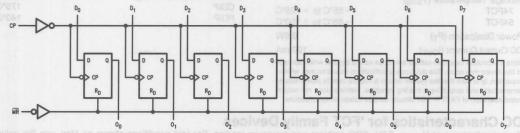
| Operating Mode |    | Outputs |                |               |
|----------------|----|---------|----------------|---------------|
| a of Va.A      | MR | СР      | D <sub>n</sub> | Qn            |
| Reset (Clear)  | L  | X       | X              | L             |
| Load '1'       | Н  | _       | Н              | V0.7 H of 8.6 |
| Load '0'       | H  | 5       | L              | A0'2 - 01 9'3 |

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

= LOW-to-HIGH Transition

#### **Logic Diagram**



TL/F/10146-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

 $\begin{array}{lll} \text{Storage Temperature (T_{STG})} \\ 74\text{FCT} & -55^{\circ}\text{C to} + 125^{\circ}\text{C} \\ 54\text{FCT} & -65^{\circ}\text{C to} + 150^{\circ}\text{C} \\ \text{Power Dissipation (P_{T})} & 0.5\text{W} \end{array}$ 

DC Output Current (IOUT)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

#### Recommended Operating

Conditions

 Supply Voltage (V<sub>CC</sub>)
 4.5V to 5.5V

 54FCT
 4.75 to 5.25V

 74FCT
 4.75 to 5.25V

 Input Voltage
 0V to V<sub>CC</sub>

 Output Voltage
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 -55°C to +125°C

 74FCT
 0°C to +70°C

Junction Temperature (T<sub>J</sub>)
CDIP
175°C
PDIP
140°C

**DC Characteristics for 'FCT Family Devices** 

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55$ °C to +125°C,  $V_{HC} = V_{CC} - 0.2V$ 

120 mA

| Symbol          | Parameter                            | 5                             | 4FCT/74F0                     | CT           | Units  | C   | onditions   |
|-----------------|--------------------------------------|-------------------------------|-------------------------------|--------------|--------|---|---|
| Symbol          | Farameter                            | Min                           | Тур                           | Max          | Office |   | Julions   |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage  | 2.0                           |                               |              | V      |   |   |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage   |                               |                               | 0.8          | ٧      |   |   |
| l <sub>IH</sub> | Input High Current                   |                               |                               | 5.0<br>5.0   | μΑ     | V <sub>CC</sub> = Max                               | $V_{l} = V_{CC}$ $V_{l} = 2.7V \text{ (Note 2)}$  |
| I <sub>IL</sub> | Input Low Current                    |                               |                               | -5.0<br>-5.0 | μΑ     | V <sub>CC</sub> = Max                               | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$   |
| V <sub>IK</sub> | Clamp Diode Voltage                  |                               | -0.7                          | -1.2         | ٧      | V <sub>CC</sub> = Min; I <sub>N</sub> = -           | -18 mA  |
| los             | Short Circuit Current                | -60                           | -120                          |              | mA     | V <sub>CC</sub> = Max (Note                         | 1); V <sub>O</sub> = GND  |
| V <sub>OH</sub> | Minimum High Level<br>Output Voltage | 2.8                           | 3.0                           |              |        | $V_{CC} = 3V; V_{IN} = 0$ $I_{OL} = 300 \mu A$      | 0.2V or V <sub>HC</sub> ;   |
|                 |                                      | V <sub>HC</sub><br>2.4<br>2.4 | V <sub>CC</sub><br>4.3<br>4.3 |              | V      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -300 \mu\text{A}$ $I_{OH} = -12 \text{mA} (\text{Mil})$ $I_{OH} = -15 \text{mA} (\text{Cor})$ |

DC Characteristics for 'FCT Family Devices (Continued) Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to +125°C, VHC = VCC - 0.2V

| Symbol           | Parameter                                    | 54FCT/74FCT  |              | Inits             | Cond  | litions   |
|------------------|--|--------------|--------------|-------------------|---|---|
| Symbol           | raidiletei = 10                              | Min Typ      | Max          | /iiito            | Cond  | itions  |
| VOL              | Maximum Low Level Output Voltage             | GND          | 0.2          | 179               | $V_{CC} = 3V; V_{IN} = 0.2$<br>$I_{OL} = 300 \mu\text{A}$                 |   |
|                  | Output voltage                               | GND GND      | 0.2          | V 0.7             | V <sub>CC</sub> = Min   | $I_{OL} = 300  \mu A$   |
| 8-8              | en   | 0.81 0.3 0.5 | 0.5<br>0.5   | 0.8               | $V_{IN} = V_{IH} \text{ or } V_{IL}$                                      | $I_{OL} = 48 \text{ mA (Mil)}$<br>$I_{OL} = 64 \text{ mA (Com}$ |
| Icc              | Maximum Quiescent<br>Supply Current          | 0.001        | 1.5          | mA <sup>0.8</sup> | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2$ $f_I = 0$              | or LVS  |
| Δl <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH | 0.5          |              | mA                | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)                  | or LO   |
| ICCD             | Dynamic Power<br>Supply Current (Note 4)     | 0.25         |              | A/MHz             | V <sub>CC</sub> Max Outputs Open  MR = V <sub>CC</sub> One Input Toggling | $V_{IN} \leq 0.2V$  |
| 01-9             | an   | 0.1          | 4            | 3,0               | 50% Duty Cycle  | 4000 J  |
| V <sub>H</sub>   | Input Hysteresis<br>on Clock Only            | 200          | ison Delays. | mV == 0           | p beleat for had bestiested o   | ne slimit numinik st stoli                                      |
| lc               | Total Power<br>Supply Current (Note 6)       | 1            | 1            | Tyr an            | V <sub>CC</sub> = Max<br>Outputs Open<br>MR = V <sub>CC</sub>             | $V_{\text{IN}} \ge V_{\text{CC}}$<br>$V_{\text{IN}} \le 0.2V$   |
|                  |  | 1.8          | 6.0          | 8 V6              | ono bit rogginig  | $V_{IN} = 3.4V$ $V_{IN} = GND$                                  |
|                  |  | 3.0          | 7.8          | mA                | (Note 5)  V <sub>CC</sub> = Max  Outputs Open  MR = V <sub>CC</sub>       | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                        |
|                  |  | 5.0          | 16.8         |                   | f <sub>I</sub> = 2.5 MHz<br>Eight Bits Toggling<br>50% Duty Cycle         | $V_{IN} = 3.4V$<br>$V_{IN} = GND$                               |
| VH               | Input Hysteresis on Clock Only               | 200          |              | mV                |   |   |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_{C} = I_{CC} + \Delta I_{CC} D_{H} N_{T} + I_{CCD} (f_{CP}/2 + f_{I} N_{I})$ 

I<sub>CC</sub> = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Curent for a TTL High Input ( $V_{IN}$  = 3.4V)

 $D_{H} = Duty Cycle for TTL inputs High$ 

 $N_T$  = Number of Inputs at  $D_H$ 

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

|                  | Conditions                           | V                         | CC = 5.0V         | CL  | = 50       | pF   | CL =  | 50 pF            | Ollito                   | No.  |
|------------------|--------------------------------------|---------------------------|-------------------|-----|------------|------|-------|------------------|--------------------------|------|
|                  | W.V. W. = 0.2V.VE =                  | asV                       | Тур               | Min | CHIC       | Max  | Min   | Max              | numivohi.                |      |
| t <sub>PHL</sub> | Propagation Delay<br>Clock to Output | = 101                     | 7.0               | 2.0 | CHAR       | 13.0 |       | oltage -         | ns                       | 2-8  |
| tplH Ama         | Propagation Delay MR to Output       | N/V                       | 8.0               | 2.0 | 6,0<br>8,0 | 13.0 |       |                  | ns                       | 2-8  |
| tsu              | Setup Time HIGH<br>or LOW Data to CP | VooV<br>V <sub>IN</sub> V | 3.0 <sub>Am</sub> | 3.0 |            |      |       |                  | Maximun<br>8<br>Supply C | 2-10 |
| th               | Hold Time HIGH or LOW Data to CP     | Vec                       | 1.0               | 2.0 | 2.6        |      | thren | t Supply Cun     | ns<br>leoseaco           | 2-10 |
| t <sub>w</sub>   | Clock Pulse Width<br>HIGH or LOW     | V <sub>IN</sub> +         | 4.0               | 7.0 |            |      |       | ts HIGH<br>Power | on Dynamic               | 2-9  |
| t <sub>w</sub>   | MR Pulse Width<br>HIGH or LOW        | QUO<br>FIM                | 4.0 AAm           | 7.0 | 0.25       |      | (4    | etol/I) friemu   | ns                       | 2-9  |
| t <sub>rec</sub> | Recovery Time MR to CP               | 50%                       | 3.0               | 4.0 |            |      |       |                  | ns                       | 2-10 |

Note 1: Minimum limits are guaranteed but not tested on Propagation Delays.

#### Capacitance TA = 25°C, f = 1.0 MHz

| Symbol | Parameter          | Conditions            | Тур | Max | Unit |
|--------|--------------------|-----------------------|-----|-----|------|
| CIN    | Input Capacitance  | V <sub>IN</sub> = 0V  | 6   | 10  | pF   |
| COUT   | Output Capacitance | V <sub>OUT</sub> = 0V | 8   | 12  | pF   |

Note: This parameter is guaranteed by characterization data and not tested.

Note 5: Values for these conditions are examples of the log formula. These finds are guaranteed but not rested.



# 54FCT/74FCT373 Octal Transparent Latch with TRI-STATE® Outputs

#### **General Description**

The 'FCT373 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable  $(\overline{\text{OE}})$  is LOW. When  $\overline{\text{OE}}$  is HIGH, the bus output is in the high impedance state.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

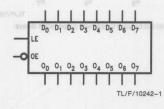
#### **Features**

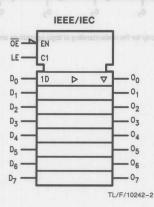
- NSC 54FCT/74FCT373 is pin and functionally equivalent to IDT 54FCT/74FCT373
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (commercial) and 32 mA (military)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and standard military drawing #5962-87644

Ordering Code: See Section 8

**Logic Symbols** 

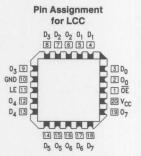
#### **Connection Diagrams**







| Pin Names                      | Description             |
|--------------------------------|-------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs             |
| LE                             | Latch Enable Input      |
| ŌĒ                             | Output Enable Input     |
| 00-07                          | TRI-STATE Latch Outputs |



TL/F/10242-4

#### **Functional Description**

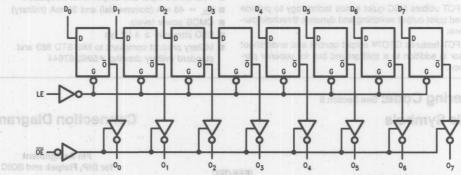
The 'FCT373 contains eight D-type latches with TRI-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the  $\mathsf{D}_\mathsf{D}$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE standard outputs are controlled by the Output Enable  $(\overline{\mathsf{OE}})$  input. When  $\overline{\mathsf{OE}}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{\mathsf{OE}}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches

## Truth Table

|    | Inputs | Outputs |           |
|----|--------|---------|-----------|
| LE | ŌĒ     | Dn      | On        |
| X  | PHOT   | X       | Z         |
| Н  | L.     | L       | L         |
| H  | 10018  | Н       | I STOHO ! |
| L  | L      | X       | On        |

- H = HIGH Voltage Level
- L = LOW Voltage Level
  Z = High Impedance
- X = Immaterial and took metaly a bestingground took astud
- O<sub>n</sub> = Previous O<sub>n</sub> before HIGH to Low transition of Latch Enable

#### **Logic Diagram**



TL/F/10242-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V<sub>TERM</sub>)
54FCT -0.5V to +7.0V
74FCT -0.5V to +7.0V

Temperature under Bias (T<sub>BIAS</sub>)

74FCT VS.0 > MIV = 65°C to + 125°C 54FCT = 65°C to + 135°C

Storage Temperature (T<sub>STG</sub>)

54FCT
Power Dissipation (P<sub>T</sub>)

DC Output Current (I<sub>OUT</sub>)

120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reli-

able over its power supply, temperature, and output/input loading variables.

## Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 4.5V to 5.5V

 54FCT
 4.75V to 5.25V

 74FCT
 4.75V to 5.25V

 Input Voltage
 0V to V<sub>CC</sub>

 Output Voltage
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 -55°C to +125°C

74FCT

Junction Temperature (T<sub>J</sub>)
CDIP
PDIP

175°C

-0°C to +70°C

**DC Characteristics for 'FCT Family Devices** 

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55$ °C to +125°C.  $V_{MC} = V_{CC} - 0.2V$ 

-55°C to +125°C -65°C to +150°C

| Symbol          | QVD = Parameter pallogoT a                   | 54                      | FCT/74                        | FCT                            | Units               | 0.8  | Conditions   |  |
|-----------------|--|-------------------------|-------------------------------|--------------------------------|---------------------|--|--|--|
| Cymbol          | sloyO'y                                      | Min                     | Тур                           | Max                            | Oints               |  |  |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage          | 2.0                     | ν                             | 173                            | V                   | 200  |  | /H Input Hyster on Clock Or  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage           | sinit and               | th barrons                    | 0.8                            | more than V         |  |  | Note 1: Modmum test duralli<br>Rots 2: This parameter guera  |
| lін             | Input High Current                           | lations.                |                               | F 0                            | μΑ                  | V <sub>CC</sub> = Max                        | is (VP.6 = p(V)<br>I directly testable<br>muse are exami | $V_l = V_{CC}$<br>$V_l = 2.7V \text{ (Note 2)}$  |
| l <sub>IL</sub> | Input Low Current                            |                         |                               | -5.0<br>-5.0                   | μА                  | V <sub>CC</sub> = Max                        | NASAL + STANTA   | $V_I = 0.5V$ (Note 2)<br>$V_I = GND$   |
| loz             | Maximum TRI-STATE Current                    |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | (VA.8 = )<br>μΑ     |  | HG to sit  | $V_{O} = V_{CC}$<br>$V_{O} = 2.7V \text{ (Note 2)}$<br>$V_{O} = 0.5V \text{ (Note 2)}$<br>$V_{O} = \text{GND}$           |
| V <sub>IK</sub> | Clamp Diode Voltage                          |                         | -0.7                          | -1.2                           | alge V noi 1        | V <sub>CC</sub> = Min;                       | $I_N = -18  \text{m}$                                    | Ice = Clock Frague   |
| los             | Short Circuit Current                        | -60                     | -120                          |                                | mA                  | V <sub>CC</sub> = Max                        | (Note 1); Vo   | = GND  |
| V <sub>OH</sub> | Minimum High Level                           | 2.8                     | 3.0                           |                                | .predagen           | V <sub>CC</sub> = 3V; \                      | $I_{\rm IN} = 0.2 \rm V  or $                            | $V_{HC}$ ; $I_{OH} = -32 \mu A$  |
|                 | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 | anoliibiisa si                 | if to <b>V</b> elds | $V_{CC} = Min$ $V_{IN} = V_{IH} o$           | r V <sub>IL</sub>  | $\begin{split} I_{OH} &= -300~\mu\text{A} \\ I_{OH} &= -12~\text{mA (Mil)} \\ I_{OH} &= -15~\text{mA (Com)} \end{split}$ |
| VOL             | Maximum Low Level                            |                         | GND                           | 0.2                            |                     | V <sub>CC</sub> = 3V; \                      | $I_{\rm IN}=0.2 {\rm V}$ or                              | $V_{HC}$ ; $I_{OL} = 300 \mu A$  |
|                 | Output Voltage                               |                         | GND<br>0.3<br>0.3             | 0.2<br>0.50<br>0.50            | ٧                   | $V_{CC} = Min$ $V_{IN} = V_{IH} o$           |  | $I_{OL} = 300 \mu A$<br>$I_{OL} = 32 \text{ mA (Mil)}$<br>$I_{OL} = 48 \text{ mA (Com)}$                                 |
| Icc             | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                            | mA                  | $V_{CC} = Max$ $V_{IN} \ge V_{HC}$ $f_I = 0$ |  |  |
| Δlcc            | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                            | mA                  | $V_{CC} = Max$ $V_{IN} = 3.4V$               |  |  |

DC Characteristics for 'FCT Family Devices Typical values are at  $V_{CC}=5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_{A}=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_{A}=-55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC}=V_{CC}-0.2V$  (Continued)

|  | Posemeter.   |   | 74FCT   | Hei                              | 140                    |   | espect to GND (/   | Voltage with Pie  |                                      |
|--|--|---|---|----------------------------------|------------------------|---|--|---|--------------------------------------|
| Symbol   | Parameter  | Min   | Тур Ма  |                                  | its                    |   | Cond   |   |                                      |
| ICCD   | Dynamic Power<br>Supply Current (Note 4)   | 3 Ani dipagnini   | 0.15 0.4  | 0 0                              | MHz                    | V <sub>CC</sub> = I<br>Outputs<br>One Inp<br>50% Du | Open<br>ut Toggling  | 1114 - 0.111  |                                      |
| 175°001  | Total Power Supply<br>Current (Note 6)   | 1.5   | 9(Q)<br>9(C4.5  | W                                | 120 m                  | $V_{CC} = I$ Outputs $\overline{OE} = G$ $LE = V_0$ | Open<br>ND   | V < 0.2V  | 74PC1<br>54PC1<br>Power D<br>DC Outp |
|  |  | 1.8   | 5.0   | ) m                              | outmod                 | f <sub>I</sub> = 10 l<br>One Bit<br>50% Du          | Toggling   | $V_{IN} = 3.4V$ $V_{IN} = GND$  |                                      |
|  | ns shown as Max, use 1<br>Voc = 5.0V ±10%, TA  |   |   | Davic<br>I number                | ylint<br>n bas         | $(Note 5)$ $V_{CC} = 1$ $\overline{OE} = G$         | Max<br>ND  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$  | DC C                                 |
|  | A. 1   |   |   |                                  |                        | LE = V  | OC VS.0 -  | °C, VHC = VGC   | 10 + 126                             |
|  | Conditions   | 5.0   | alin14.   | FOT Max                          | CT7.74<br>Typ          | f <sub>I</sub> = 2.5<br>Eight Bit<br>50% Du         | s Toggling   | $V_{IN} = 3.4V$ $V_{IN} = GND$  | lotleng                              |
| /н   | Input Hysteresis<br>on Clock Only  |   | 200 V   | m'                               | V                      |   |  |   |                                      |
| Note 1: Ma   | aximum test duratioin not to exce  | ed one second   | d, not more than  | one output s                     | horted at              | t one time  | Janes J  | out I mount in the  | U                                    |
|  | is parameter quaranteed but not  | tostad  |   | 8.0                              | nortou d               | t one time.   |  |   |                                      |
| Note 2: Thi<br>Note 3: Pe<br>Note 4: Thi   | is parameter guaranteed but not $r$ TTL driven input ( $V_{\text{IN}} = 3.4V$ ); is parameter is not directly testab   | all other inputs<br>ole, but is deriv   | ed for use in To  | tal Power Su                     | pply calc              | ulations.   |  |   |                                      |
| Note 2: The<br>Note 3: Pe<br>Note 4: The<br>Note 5: Va<br>Note 6: Ic                           | r TTL driven input ( $V_{IN} = 3.4V$ ); is parameter is not directly testablues for these conditions are exa =  QUIESCENT +  INPUTS +  DVIESCENT +  ACC DHNT +  ACC (fc)   | all other inputs<br>ole, but is deriv<br>mples of the lo  | red for use in To   | tal Power Su                     | pply calc              | ulations.   | sted.  |   |                                      |
| Note 2: Thi Note 3: Pe Note 4: Thi Note 5: Va Note 6: Ic Icc Icc DH NT                         | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa =  coulescent +  inputs +  oyie =  cc + A cc D <sub>H</sub> NT +  ccp (fc); = Quiescent Current core = Duty Cycle for TTL Inputs High = Number of Inputs at D <sub>H</sub>   | all other inputs ole, but is deriv mples of the lo NAMIC p/2 + f <sub>l</sub> N <sub>l</sub> )  TTL High Inpu   | red for use in To<br>CC formula. Thes<br>at (V <sub>IN</sub> = 3.4V)  | tal Power Su<br>tel limits are g | pply calc              | ulations.   | sted.  |   |                                      |
| Note 2: Thi Note 3: Pe Note 4: Thi Note 5: Va Note 6: Ic Ic Ic Ic DH NT                        | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa ≡ louiESCENT + linputs + loyi = loc + Δloc DHNT + loco (for the conditions) is equal to the condition of   | all other inputs ble, but is deriv mples of the le NAMIC p/2 + f <sub>l</sub> N <sub>l</sub> ) TTL High Input th  | red for use in To $_{\rm CC}$ formula. These $_{\rm CC}$ in $_{\rm CC}$ $_{\rm CC}$ formula. The $_{\rm CC}$ in $_{\rm CC}$ formula. The $_{\rm CC}$                | tal Power Super limits are g     | pply calc              | ulations.   | sted. Institution of the state  |   |                                      |
| Note 2: Thi Note 3: Pe Note 4: Thi Note 5: Va Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa =  QUIESCENT +  INPUTS +  DYIE =  CC + A CC DHNT +  CCD (fc) = Quiescent Current or a = Duty Cycle for TTL Inputs Hig = Number of Inputs at DH (DE = Dynamic Current Caused by a = Clock Frequency   | all other inputs ole, but is deriv mples of the long NAMIC p/2 + f <sub>1</sub> N <sub>1</sub> )  TTL High Input of the long of the lon | ared for use in To<br>CC formula. These  Aut (V <sub>IN</sub> = 3.4V)  Autition Pair (HLH  of for Non-Registr   | tal Power Super limits are g     | pply calc              | ulations.   | sted. Institution of the state  |   |                                      |
| Note 2: Th Note 3: Pe Note 4: Th Note 5: Va Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I   | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa =  culescent +  inputs +  oxiecolor  | all other inputs ole, but is deriv mples of the Ic NAMIC p/2 + f <sub>1</sub> N <sub>1</sub> )  TTL High Input gh v an Input Tran r Devices (Zero frequencies ar drawing or NS  | red for use in To<br>co formula. These<br>struct (V <sub>IN</sub> = 3.4V)<br>sistion Pair (HLH<br>to for Non-Registruction of the control of the<br>e in megahertz. | or LHL)                          | pply calc              | rulations. ad but not te                            | sted.  STATE Current oftage unent  | Input Voltage Input High Cum Input Low Cum Meyimum TRI-   |                                      |
| Note 2: Th Note 3: Pe Note 4: Th Note 5: Va Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I   | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa =  culescent +  inputs +  oxiecolor  | all other inputs ole, but is deriv mples of the lo NAMIC p/2 + f <sub>1</sub> N <sub>1</sub> )  TTL High Input the derivative of the local control of the lo | red for use in To<br>co formula. These<br>struct (V <sub>IN</sub> = 3.4V)<br>sistion Pair (HLH<br>to for Non-Registruction of the control of the<br>e in megahertz. | or LHL)                          | pply calc              | rulations. ad but not te                            | sted.  STATE Current oftage unent  | Input Voltage Input High Cum Input Low Cum Mayernum TRI- Olamp Diode V Short Circuit C Minimum High               |                                      |
| Note 2: Th Note 3: Pe Note 4: Th Note 5: Va Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I   | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa =  QUIESCENT +  INPUTS +  DYIESCENT +  INPUTS +  DYIESCENT +  INPUTS +  CCC   Coccession   CCC +  CCC | all other inputs ole, but is deriv mples of the Io NAMIC p/2 + f <sub>1</sub> N <sub>1</sub> )  TTL High Input gh v an Input Tran r Devices (Zero frequencies and drawing or NS   | red for use in To<br>co formula. These<br>st (V <sub>IN</sub> = 3.4V)<br>sistion Pair (HLH<br>to for Non-Registe<br>e in megahertz.                                 | or LHL)                          | pply calc              | culations.  ad but not te                           | sted.  Institute of the state o | Input Voltage Input High Cum Input Low Cum Mayernum TRI- Olamp Diode V Short Circuit C Minimum High               |                                      |
| Note 2: Th Note 3: Pe Note 4: Th Note 5: Va Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I   | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa ≡ louiesCENT + linpuTs + loyie = Icc + ΔIcc D <sub>H</sub> NT + Icc) (fct) = Quiescent Current core = Power Supply Current for a = Duty Cycle for TTL Inputs Hight = Number of Inputs at D <sub>H</sub> = Dynamic Current Caused by = Clock Frequency for Register = Input Frequency = Number of Inputs at ficurrents are in milliamps and all it r 54FCT, IccD = 0.40 mA/MHz. For to applicable standard military   | all other inputs ole, but is deriv mples of the Io NAMIC p/2 + f <sub>1</sub> N <sub>1</sub> )  TTL High Input gh v an Input Tran r Devices (Zero frequencies and drawing or NS   | ared for use in To<br>co formula. These<br>art (V <sub>IN</sub> = 3.4V)<br>distition Pair (HLH<br>o for Non-Registr<br>e in megahertz.                              | or LHL) er Devices)              | pply calc<br>guarantee | culations.  ad but not te                           | sted.  tnemuO ETATE  egatio  tnemu tnemu   | Input Voltage Input High Curr Input Low Curr Maximum TRI- Olamp Diode V Short Circuit O Athrimum High             |                                      |
| Note 2: Th Note 3: Pe Note 4: Th Note 5: Va Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I   | r TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testablues for these conditions are exa = louiscent + linputs + lovi = loc + Δloc D <sub>H</sub> NT + loco (for example) = loc + Δloc D <sub>H</sub> NT + loco (for example) = Duty Cycle for TTL Inputs High = Number of Inputs at D <sub>H</sub> = Duty Cycle for TTL Inputs High = Number of Inputs at D <sub>H</sub> = Dynamic Current Caused by example = Clock Frequency for Register = Input Frequency = Number of Inputs at f <sub>1</sub> currents are in milliamps and all to start to applicable standard military  | all other inputs ole, but is deriv mples of the lo NAMIC p/2 + f <sub>1</sub> N <sub>1</sub> )  TTL High Input the properties of the local transfer of th | red for use in To<br>co formula. These<br>out (VIN = 3.4V)<br>distinct Pair (HLH<br>of for Non-Registration Pair (HLH<br>e in megahertz.                            | or LHL) er Devices)              | pply calcularantee     | culations.  ad but not te                           | sted.  fine fine fine fine fine fine fine fin  | Input Voltage Input High Cum Input Low Cum Maximum TRI- Olamp Diode V Short Circuit C Output Voltage Maximum High |                                      |

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                      |   | 54FCT/74FCT                                      | 74FCT  |              | 541  | FCT                      | ma2     |      |
|--------------------------------------|---|--|--|--------------|------|--------------------------|---------|------|
| Symbol                               | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | T <sub>A</sub> , V <sub>CC</sub> = R <sub>L</sub> = 50 C <sub>L</sub> = 50 | 0Ω           | RL = | C = Mil<br>500Ω<br>50 pF | Units   | Fig. |
|                                      |   | Тур 💮  | Min (Note 1)   | Max          | Min  | Max                      | l Cl le | toO  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 5.0  | 1.5  | 8.0          | 1.5  | 8.5                      | ns      | 2-8  |
| t <sub>PZH</sub>                     | Output Enable Time                                    | TETOR 7.0TO AND OF                               | DEM #1.5-qill eq   | 12.0         | 1.5  | 13.5                     | ns      | 2-11 |
| t <sub>PHZ</sub>                     | Output Disable Time                                   | gbe troppe belled<br>firmm, 6.0 belon be         | noO M 1.5 Hud A  | 7.5          | 1.5  | 10.0                     | ns No.  | 2-11 |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>LE to O <sub>n</sub>             | of sec 9.0 quisio                                | ugal #2.0 ong ci   | 13.0         | 2.0  | 15.0                     | ns      | 2-8  |
| tsu                                  | Set Up Time High or Low Dn to LE                      | = 48 mô.formmen                                  | Joh 2.0  | obau bas k   | 2.0  | o MIOTE a                | ns      | 2-10 |
| t <sub>H</sub> -nsi                  | Hold Time High or Low                                 | d Villa ≤ viloummi<br>1.0<br>topoto ver          | 1.5 a MIH  | s for superi | 3.0  | slige a of ne            | ns ,    | 2-10 |
| tw                                   | LE Pulse Width<br>High or Low                         | 5.0  | 6.0  |              | 6.0  |                          | ns      | 2-9  |

## Capacitance T<sub>A</sub> = +25°C, f = 10 MHz

| Symbol               | Parameter (Note)   | Тур | Max | Units | Condition             |
|----------------------|--------------------|-----|-----|-------|-----------------------|
| C <sub>IN</sub> 3/01 | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| COUT                 | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested. C<sub>OUT</sub> for 74FCT only.

> P. El 30 医图如

DEPENDENCE



#### Voc = 5.0V 54FCT/74FCT374 Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'FCT374 is a high-speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all

FACTIM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

■ NSC 54FCT/74FCT374 is pin and functionally equivalent to IDT 54FCT/74FCT374

AC Electrical Characteristics: See Section 2 for Waveforms

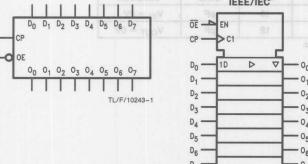
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (commercial) and 32 mA (military)
- CMOS power levels
- ESD immunity ≥ 4kV typ
- Military product compliant to MIL-STD 883 and standard military drawing #5962-87628

Ordering Code: See Section 8

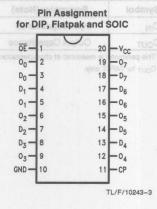
#### **Logic Symbols**

#### **Connection Diagrams**

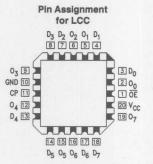
Symbol



| IE    | EE/IEC |                               |
|-------|--------|-------------------------------|
| EN C1 | 12     | 0                             |
| 1D    | D      |                               |
| =     |        | 01                            |
| =     |        | 0 <sub>3</sub>                |
| ==    |        | 0 <sub>5</sub>                |
|       |        | 0 <sub>7</sub><br>TL/F/10243- |



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| CP                             | Clock Pulse Input             |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Outputs             |



TL/F/10243-4

#### Functional Description

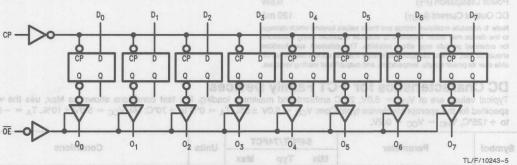
The 'FCT374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{\text{OE}}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{\text{OE}}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{\text{OE}}$  input does not affect the state of the flip-flops.

#### Truth Table its 9 mumixsM stulosdA

| are required,<br>fortor Salas | Inputs | space spacement | Outputs         |
|-------------------------------|--------|-----------------|-----------------|
| Dn                            | CP     | IN ISTER OF ICE | tudint On \sort |
| Н                             | _      | L               | mins H'ollage   |
| was Lusa                      | _      | MRETY SIND O    | Toeque History  |
| X                             | X      | Н               | Z               |

- H = HIGH Voltage Level
- L = LOW Voltage Level X = Immaterial
- X = ImmaterialZ = High Impedance
- = LOW-to-HIGH Transition

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| JIV |                           |  |  |   |  |
|-----|---------------------------|--|--|---|--|
|     |                           |  |  |   | V <sub>1</sub> = V <sub>CC</sub><br>V <sub>2</sub> = 2.7V (Note 2) |
|     |                           |  |  |   |  |
|     | Maximum TRI-STATE Current |  |  |   |  |
|     |                           |  |  |   |  |
|     |                           |  |  | V <sub>OC</sub> = Max (Note 1); V <sub>C</sub>      |  |
|     |                           |  |  | $V_{GC} = 3V; V_{BA} = 0.2V c$                      |  |
|     |                           |  |  |   |  |
|     |                           |  |  |   |  |
|     |                           |  |  | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ |  |
|     |                           |  |  |   |  |
|     |                           |  |  |   |  |

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| with Respect to GND (V <sub>TERM</sub> ) 54FCT 74FCT          | -0.5V to 7.0'<br>-0.5V to 7.0' |
|---|--------------------------------|
| Temperature under Bias (T <sub>BIAS</sub> )<br>74FCT<br>54FCT | -55°C to +125°C to +135°C      |
| Storage Temperature (T <sub>STG</sub> )<br>74FCT<br>54FCT     | -55°C to +125°C                |
| Power Dissipation (P <sub>T</sub> )                           | 0.5\                           |
| DC Output Current (IOUT)                                      | 120 m                          |
|   |                                |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

## Recommended Operating and to an a Conditions

| Supply Voltage (V <sub>CC</sub> )       |                       |
|---|-----------------------|
| 54FCT on eldand Juglio b                | 4.5V to 5.5V          |
| 1974FCT als eff evals liw agoil         | 4.75V to 5.25V        |
| Input Voltage                           | 0V to V <sub>CC</sub> |
| Output Voltage                          | 0V to V <sub>CC</sub> |
| Operating Temperature (T <sub>A</sub> ) |                       |
| or54FCT iterago estate consber          | -55°C to +125°C       |
| 74FCT agoit-gill and to state e         | 0°C to +70°C          |
| Junction Temperature (T <sub>J</sub> )  |                       |
| CDIP                                    | 175°C                 |
| PDIP                                    | 140°C                 |
|   |                       |

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil;  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55$ °C to +125°C,  $V_{HC} = V_{CC} - 0.2V$ .

| Symbol           | Parameter                                    | Parameter 54FCT/74FCT                |                                      | FCT ,                          | Units  | Conditions  |   |  |
|------------------|--|--------------------------------------|--------------------------------------|--------------------------------|--------|---|---|--|
| 3-84507\F        | raidilletei                                  | Min                                  | Тур                                  | Max                            | Offics | Conditions  |   |  |
| V <sub>IH</sub>  | Minimum High Level Input Voltage             | 2.0                                  | na zaoline                           | ac algel to pr                 | V      | lagram is provided only for the u                             | Floass note that this o   |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           |                                      |                                      | 0.8                            | ٧      |   |   |  |
| Ін               | Input High Current                           |                                      |                                      | 5.0<br>5.0                     | μА     | V <sub>CC</sub> = Max   | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |  |
| I <sub>IL</sub>  | Input Low Current                            |                                      |                                      | -5.0<br>-5.0                   | μА     | V <sub>CC</sub> = Max   | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$   |  |
| l <sub>OZ</sub>  | Maximum TRI-STATE Current                    |                                      |                                      | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ     | V <sub>CC</sub> = Max   | $V_{O} = V_{CC}$ $V_{O} = 2.7V \text{ (Note 2)}$ $V_{O} = 0.5V \text{ (Note 2)}$ $V_{O} = \text{GND}$                             |  |
| V <sub>IK</sub>  | Clamp Diode Voltage                          |                                      | -0.7                                 | -1.2                           | ٧      | $V_{CC} = Min; I_N = -18$                                     | mA  |  |
| los              | Short Circuit Current                        | -60                                  | -120                                 |                                | mA     | V <sub>CC</sub> = Max (Note 1); V                             | O = GND   |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage         | 2.8<br>V <sub>HC</sub><br>2.4<br>2.4 | 3.0<br>V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧      | V <sub>CC</sub> = Min   | or $V_{HC}$ ; $I_{OH} = -32 \mu A$<br>$I_{OH} = -300 \mu A$<br>$I_{OH} = -12 \text{ mA (Mil)}$<br>$I_{OH} = -15 \text{ mA (Cor)}$ |  |
| V <sub>OL</sub>  | Maximum Low Level                            |                                      | GND                                  | 0.2                            |        | $V_{CC} = 3V; V_{IN} = 0.2V$                                  | or V <sub>HC</sub> ; I <sub>OL</sub> = 300 μA   |  |
|                  | Output Voltage                               |                                      | GND<br>0.3<br>0.3                    | 0.2<br>0.50<br>0.50            | ٧      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$           | I <sub>OL</sub> = 300 μA<br>I <sub>OL</sub> = 32 mA (Mil)<br>I <sub>OL</sub> = 48 mA (Com)  |  |
| lcc              | Maximum Quiescent<br>Supply Current          |                                      | 0.001                                | 1.5                            | mA     | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2V$ $f_I = 0$ |   |  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                                      | 0.5                                  | 2.0                            | mA     | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)      |   |  |

| Symbol     | Paramete                            | - 10     | 74FCT   | 2 = 1H | Units  | Vcc = 5  | Conditions   |                         |
|------------|-------------------------------------|----------|---------|--------|--------|--|--|-------------------------|
| Symbol     | raramete                            | mits     | Min Typ | Max    | Office | OVT  | Conditions   |                         |
| ICCD       | Dynamic Power<br>Supply Current (I  | Note 4)  | 0.15    | 0.25   | mA/MHz | V <sub>CC</sub> = Max<br>Outputs Open                        | $V_{IN} \ge V_{H}$<br>$V_{IN} \le 0.2$             |                         |
| 11-S       | 14.0 ns                             | 1.5      | 12.5    | 1.5    |        | One Input Toggli<br>50% Duty Cycle                           | CONTRACTOR AND AND AND AND AND AND AND AND AND AND |                         |
| Ic<br>tr-s | Total Power Sup<br>Current (Note 6) |          | 0.8     | 4.0    |        | V <sub>CC</sub> = Max Outputs Open f <sub>CP</sub> = 10 MHz  | $V_{IN} \ge V_{H}$ $V_{IN} \le 0.2$                |                         |
|            | an                                  | 2.5      |         | 2.0    |        | OE = GND   | Set Up Time High or L                              | lgo l                   |
|            | an                                  | 2.5      | 1.8     | 6.0    |        | f <sub>I</sub> = 5 MHz<br>One Bit Toggling<br>50% Duty Cycle | VIN - GI   |                         |
|            | an                                  | 7.0      |         | 7.0    | mA     | (Note 5)<br>V <sub>CC</sub> = Max                            | $V_{IN} \ge V_{H}$ $V_{IN} \le 0.2$                |                         |
|            |                                     |          | 3.0     | 7.8    |        | Outputs Open   | nd poetrareug ett. slime m                         | Note 1: Minimul Capacit |
|            |                                     | ondfilon | ) BriU  | 30     |        | f <sub>I</sub> = 2.5 MHz                                     | V <sub>IN</sub> = 3.4                              | tV damed                |
|            |                                     | V0 = W   | 5.0     | 16.8   |        | Eight Bits Toggli  | ng VINI = GN                                       |                         |
|            |                                     | /0 = THE |         | 1 5    |        | 50% Duty Cycle   | Curput Cape  |                         |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I<sub>CCD</sub> = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I<sub>C</sub>/I<sub>CC</sub> limits.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                  | Mil Voc = 5.0V ± 10%, TA                                  | 54FCT/74FCT                                      | 74FCT  | 54FCT  | ed for the | i ypicai    |
|------------------|---|--|--|--|------------|-------------|
| Symbol           | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | $T_A$ , $V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50 pF$ | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$ | Units      | Fig.<br>No. |
|                  |   | Тур  | Min (Note 1) Max                                       | Min Max  |            |             |
| t <sub>PLH</sub> | Propagation Delay<br>Cp to On                             | o ekigh 6.6                                      | 2.0 10.0   | 2.0 11.0   | ns         | 2-8         |
| t <sub>PZH</sub> | Output Enable Time  | VIDG % 9.0                                       | 1.5 12.5   | 1.5 14.0   | ns         | 2-11        |
| t <sub>PHZ</sub> | Output Disable Time                                       | 6.0 atuque                                       | 1.5 8.0  | 1.5 (8.0)  | ns         | 2-11        |
| tsu              | Set Up Time High or Low Dn to Cp                          | MD = 1.0   | 2.0  | 2.5  | ns         | 2-10        |
| t <sub>H</sub>   | Hold Time High or Low<br>D <sub>n</sub> to C <sub>P</sub> | 0.5 Dury Dury                                    | 2:0 8 8.8  | 2.5  | ns         | 2-10        |
| t <sub>w</sub>   | C <sub>P</sub> Pulse Width<br>High or Low                 | (8 etc 4.0                                       | 7.0  | 7.0  | ns         | 2-9         |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

#### Capacitance TA = +25°C, f = 1.0 MHz

| Symbol           | Parameter (Note 1) | Тур | Max    | Unit | Condition             |
|------------------|--------------------|-----|--------|------|-----------------------|
| CIN GME          | Input Capacitance  | 6   | 10 8.3 | pF   | V <sub>IN</sub> = 0V  |
| C <sub>OUT</sub> | Output Capacitance | 8   | 12     | pF   | V <sub>OUT</sub> = 0V |

Note 1: This parameter is measured at characterization but not tested.

Court for 74FCT only.

Refer to applicable standard military drawing or NSC Table I for test conditions and Ic/Icc limits.



# 54FCT377/74FCT377 Octal D Flip-Flop with Clock Enable

#### **General Description**

The FCT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable  $(\overline{CE})$  is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The  $\overline{\text{CE}}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

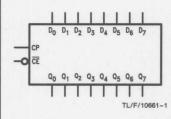
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance

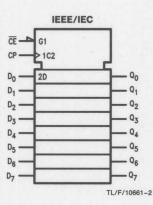
#### **Features**

- NSC 54FCT/74FCT377 is pin and functionally equivalent to IDT 54FCT/74FCT377
- Ideal for addressable register applications
- Clock enables for address and data synchronization applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OI</sub> = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883 and Standard Military Drawing # 5962-87627

Ordering Code: See Section 8

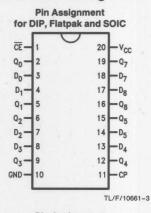
#### **Logic Symbols**

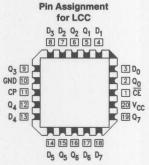




| Pin Names                      | Description               |
|--------------------------------|---------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs               |
| CE                             | Clock Enable (Active LOW) |
| Q <sub>0</sub> -Q <sub>7</sub> | Data Outputs              |
| CP                             | Clock Pulse Input         |

#### **Connection Diagrams**





TL/F/10661-4

**Mode Select-Function Table** 

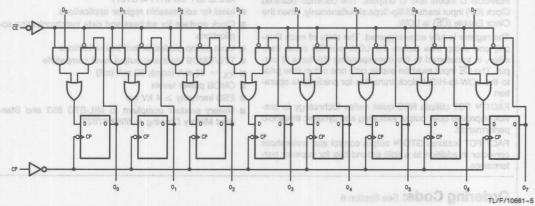
| Operating Mode       |    | Inputs |    | Outputs   |
|----------------------|----|--------|----|-----------|
| Operating mode       | СР | CE     | Dn | Qn        |
| Load '1'             | _  | L      | Н  | Н         |
| Load '0'             | _  | L      | L  | L         |
| Hold (Do Nothing)    | _  | Н      | X  | No Change |
| riola (Do Notrillig) | X  | Н      | X  | No Change |

H = HIGH Voltage Level L = LOW Voltage Level

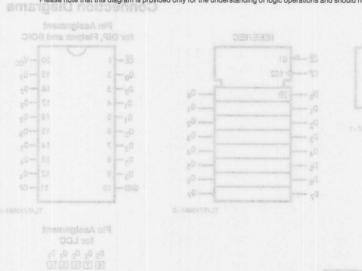
X = Immaterial

= LOW-to-HIGH Clock Transition

#### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



|                           | Do-D7 |
|---------------------------|-------|
| Clock Enable (Active LOW) |       |
|                           |       |
| Clock Pulse Input         |       |

If Military/Aerospace specified devices are required. please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| mry and opcomoduons. |
|----------------------|
| GND                  |
| -0.5V to $+7.0V$     |
| -0.5V to $+7.0$ V    |
| -55°C to +125°C      |
| -65°C to +135°C      |
|                      |
| -55°C to +125°C      |
| -65°C to +150°C      |
| negO etuatio 0.5W    |
| 120 mA               |
|                      |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

#### Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> )<br>54FCT                | 4.5V to 5.5V                           |
|---|--|
| 74FCT   | 4.75V to 5.25V                         |
| Input Voltage   | 0V to V <sub>CC</sub>                  |
| Output Voltage  | 0V to V <sub>CC</sub>                  |
| Operating Temperature (T <sub>A</sub> )<br>54FCT<br>74FCT | -55°C to +125°C<br>-0°C to +70°C       |
| Junction Temperature (T <sub>J</sub> ) CDIP PDIP          | 175°C<br>1712 Inputs HIGH<br>140°C     |
|   | COD Dynamic Power Supply Current (Note |

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55^{\circ}C$ to  $+125^{\circ}$ C,  $V_{HC} = V_{CC} - 0.2$ V.

| Symbol          | Parameter                           | 54FCT/74FCT                     |               | Units       | Conditions                                  |  |  |
|-----------------|-------------------------------------|---------------------------------|---------------|-------------|---|--|--|
| Symbol          | Parameter                           | Min Typ                         | Max           | Office      |   | mattons  |  |
| VIH             | Minimum High Level<br>Input Voltage | 2.0                             |               | V           |   |  |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     | fop = 10 MH<br>50% Duby Cy      | 0.8           | ٧           |   |  |  |
| I <sub>IH</sub> | VInput High Current                 | CE = QND<br>Q = 2.5 MHz         | 5.0<br>5.0    | μА          | V <sub>CC</sub> = Max                       | $V_I = V_{CC}$ $V_I = 2.7V \text{ (Note 2)}$           |  |
| Iլլ             | Input Low Current                   | oT end trigid                   | -5.0<br>V-5.0 | μА          | V <sub>CC</sub> = Max                       | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND |  |
| VIK             | Clamp Diode Voltage                 | -0.7                            | -1.2          | one Vall en | $V_{CC} = Min; I_N = -18 \text{ mA}$        |  |  |
| los             | Short Circuit Current               | -60 -120                        |               | mA          | V <sub>CC</sub> = Max (Note 1);             | V <sub>O</sub> = GND                                   |  |
| V <sub>OH</sub> | Minimum High Level                  | 2.8 3.0                         | ower Supply o | TatoT ni sa | $V_{CC} = 3V; V_{IN} = 0.2V$                | $V$ or $V_{HC}$ ; $I_{OH} = -32 \mu\text{A}$           |  |
|                 | Output Voltage                      | V <sub>HC</sub> V <sub>CC</sub> | dis are guera | V           | V <sub>CC</sub> = Min                       | $I_{OH} = -300 \mu A$                                  |  |
|                 |                                     | 2.4 4.3                         |               | •           | $V_{IN} = V_{IH} \text{ or } V_{IL}$        | $I_{OH} = -12 \text{mA} \text{(Mil)}$                  |  |
|                 |                                     | 2.4 4.3                         |               | (V3.8       | not for a TTL High-Input (V <sub>IM</sub> = | $I_{OH} = -15  \text{mA (Com)}$                        |  |
| VOL             | Maximum Low Level                   | GND                             | 0.2           |             | $V_{CC} = 3V; V_{IN} = 0.2V$                | $I$ or $V_{HC}$ ; $I_{OL} = 300 \mu\text{A}$           |  |
|                 | Output Voltage                      | GND                             | 0.2           | Ragive De   | V <sub>CC</sub> = Min                       | $I_{OL} = 300 \mu\text{A}$                             |  |
|                 |                                     | 0.3                             | 0.5           |             | $V_{IN} = V_{IH} \text{ or } V_{IL}$        | $I_{OL} = 32  \text{mA}  (Mil)$                        |  |
|                 |                                     | 0.3                             | 0.5           | .521011     |   | I <sub>OL</sub> = 48 mA (Com)                          |  |

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to  $+125^{\circ}$ C,  $V_{HC} = V_{CC} - 0.2$ V.

| Symbol                          | Parameter  | 74FCT                     | Units  | Conditions  |   |  |  |
|---------------------------------|--|---------------------------|--|---|---|--|--|
| 30 V 61 V                       | o rarameter  | Min Typ Max               | V0.+7.0V                                       | Va.0-   |   |  |  |
| 201<br>201<br>+ 125°C<br>+ 70°C | Maximum Quiescent<br>Supply Current  | 0.001 1.5                 | mA   | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V \\ &f_I = 0 \end{aligned}$  | 74FCT<br>Temperature Under Bla<br>74FCT<br>24FCT  |  |  |
| ΔI <sub>CC</sub>                | Quiescent Supply Current;  | 0.5 2.0                   | mA<br>Oresi + c                                | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)  | Storage Temperature (1  |  |  |
| ICCD                            | Dynamic Power<br>Supply Current (Note 4)   | 0.25 0.30                 | mA/MHz   | V <sub>CC</sub> = Max<br>Outputs Open<br>$\overline{\text{CE}}$ = GND<br>One Input Toggling<br>50% Duty Cycle   | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V   |  |  |
| lc<br>eulsv er                  | Total Power<br>Supply Current (Note 6)   | 1.5 4.0                   | den dingise<br>soldanay pr<br>antiquity Design | V <sub>CC</sub> = Max Outputs Open f <sub>CP</sub> = 10 MHz 50% Duty Cycle  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$  |  |  |
|                                 |  |                           |  |   |   |  |  |
|                                 | C; Mil: $V_{CC} = 5.0V \pm 10\%$ , $T_A =$ Conditions  |                           | 0 = 5.6V as                                    | CE = GND<br>f <sub>I</sub> = 5 MHz<br>One Bit Toggling  | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND   |  |  |
|                                 | $C_{\rm c}$ MR: $V_{\rm CC} = 5.0V \pm 10\%$ , $T_{\rm A} =$                                       | 1.8 6.0                   | 1± V0.8 = 0                                    | CE = GND<br>f <sub>I</sub> = 5 MHz<br>One Bit Toggling  | $V_{IN} = 3.4V$ $V_{IN} = GND$ $V_{IN} \ge V_{HC}$  |  |  |
|                                 | $C_{\rm c}$ MR: $V_{\rm CC} = 5.0V \pm 10\%$ , $T_{\rm A} =$                                       | 1.8 6.0 estinu            | 0 = 5.6V as                                    | CE = GND  f <sub>I</sub> = 5 MHz  One Bit Toggling 50% Duty Cycle  (Note 5)  V <sub>CC</sub> = Max  Outputs Open f <sub>CP</sub> = 10 MHz   | $\begin{aligned} &V_{IN} = 3.4V \\ &V_{IN} = GND \end{aligned}$ $\begin{aligned} &V_{IN} \geq V_{HC} \\ &V_{IN} \leq 0.2V \end{aligned}$        |  |  |
| O*88—                           | $C_{\rm c}$ MR: $V_{\rm CC} = 5.0V \pm 10\%$ , $T_{\rm A} =$                                       | 1.8 6.0 estau - 3.0 9.0 V | TAPCT  AMWER                                   | CE = GND f <sub>1</sub> = 5 MHz One Bit Toggling 50% Duty Cycle  (Note 5) V <sub>CC</sub> = Max Outputs Open f <sub>CP</sub> = 10 MHz 50% Duty Cycle  CE = GND f <sub>1</sub> = 2.5 MHz | $\begin{aligned} &V_{IN} = 3.4V \\ &V_{IN} = \text{GND} \end{aligned}$ $\begin{aligned} &V_{IN} \geq V_{HC} \\ &V_{IN} \leq 0.2V \end{aligned}$ |  |  |
| 86°C                            | C; Mil: V <sub>CC</sub> = 5.0V ±10%, T <sub>A</sub> = Conditions  V <sub>1</sub> = V <sub>CC</sub> | 1.8 6.0 estau             | TAPOT TAPOT A Amilian O Anii                   | CE = GND  f <sub>1</sub> = 5 MHz  One Bit Toggling 50% Duty Cycle  (Note 5)  V <sub>CC</sub> = Max  Outputs Open f <sub>CP</sub> = 10 MHz  50% Duty Cycle  CE = GND                     | $V_{IN} = 3.4V$ $V_{IN} = GND$ $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$  |  |  |

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6:  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$   $I_{CC} = Quiescent Current$ 

ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs HIGH

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL) f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I<sub>CCD</sub> = 0.4 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I<sub>C</sub>/I<sub>CC</sub> limits.

| Symbol                               | Parameter   | V <sub>CC</sub> = 5.0V  | C   | L = 50 pF  | C <sub>L</sub> = 5 | 0 pF   | STITE | No.  |
|--------------------------------------|---|---|-----|--|--------------------|--------|-------|------|
|                                      |   | Тур   | Min | (Note) Max   | Min                | Max    | igh!  | HELE |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>C <sub>P</sub> to $\overline{O}_{n}$ | 7.0   | 2.0 | 13.0   | 2.0                | 13.0   | ns    | 2-8  |
| t <sub>SU</sub> -sva                 | D   | C 64FCT/74FC1589 to 1DT 0.FC1/74F                             | 2.5 | parator, it com-<br>and provides a<br>t for bit. The ex- | 4.0                |        | ns    | 2-10 |
| tн                                   | HIGH or LOW   | ut olamp diodes to I<br>/CMOS0,frut and r<br>= 48 mA (Com), 8 | 2.0 |  | 2.0                |        | ns    | 2-10 |
| tsu                                  | Set Up Time<br>HIGH or LOW<br>CE to Cp 3 378-JIM of tru   | OS power levels V minim 2.1 ESD im lary Product compli        | 4.0 | toorierebnu bna  |                    |        |       | 2-10 |
| t <sub>H</sub>                       | Hold Time<br>HIGH or LOW<br>CE to Cp                      | 3.0   | 1.5 |  | 2.0                | ole    | ns    | 2-10 |
| t <sub>W</sub>                       | Clock Pulse Width, LOW                                    | 4.0   | 7.0 |  | 7.0                | 400.00 | ns    | 2-9  |

Note: Minimum limits are guaranteed but not tested on propagation delays.

### Capacitance TA = +25°C, f = 1.0 MHz

| Symbol | Parameter          | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| Cour   | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

Cout for 74FCT only.

Pin Assignment

 Pin Names
 Description

 Ao-A7
 Word A inputs

 Bo-B7
 Word B inputs

 TA = 3
 Expansion or Enable input

 OA = 8
 Identity Output



## 54FCT/74FCT521 **8-Bit Identity Comparator**

#### **General Description**

The 'FCT521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input  $\hat{I}_A = B$  also serves as an active LOW enable

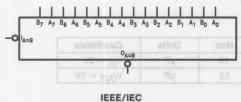
FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

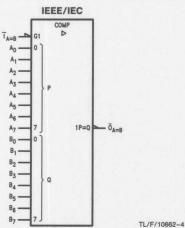
- NSC 54FCT/74FCT521 is pin and functionally equivalent to IDT 54FCT/74FCT521
- Expandable to any word length
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

#### **Logic Symbols**

#### **Connection Diagrams**







|  | 7 |  |
|--|---|--|
|  |   |  |

6-40

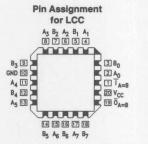
| Pin Names                      | Description               |   |
|--------------------------------|---------------------------|---|
| A <sub>0</sub> -A <sub>7</sub> | Word A Inputs             |   |
| B <sub>0</sub> -B <sub>7</sub> | Word B Inputs             |   |
| $T_A = B$                      | Expansion or Enable Input |   |
| $\overline{O}_A = B$           | Identity Output           |   |
|                                | -                         | _ |

## Pin Assignment



TL/F/10662-2

Symbol



TL/F/10662-3



54FCT/74FCT533

Octal Transparent Latch with TRI-STATE® Outputs

#### **General Description**

The 'FCT533 consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state. FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance. FACT FCT features GTOTM output control and undershoot corrector in addition to a split ground bus for superior performance. The 'FCT533 is the same as the 'FCT373, except that the outputs are inverted.

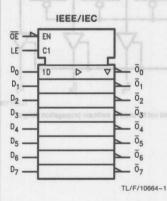
#### **Features**

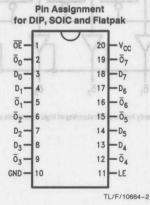
- NSC 54FCT/74FCT533 is pin and functionally equivalent to IDT 54FCT/74FCT533
- TRI-STATE outputs for bus interfacing
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels of the ineragenest ene sexual ent
- ESD immunity 4 kV typ and Jugas Q all emit riose etals
- Military product compliant to MIL-STD 883 and Standard Military Drawing #5962-88651

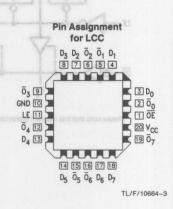
Ordering Code: See Section 8

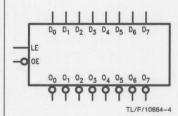
**Logic Symbols** 

**Connection Diagrams** 









| Pin Names                         | Description                      |
|-----------------------------------|----------------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                      |
| LE                                | Latch Enable Input (Active HIGH) |
| ŌĒ                                | Output Enable Input (Active LOW) |
| $\overline{O}_0 - \overline{O}_7$ | Complementary TRI-STATE Outputs  |

Ath TRI-STATE® Outputs

#### **Function Table**

|    | Inputs | DIE | Output |
|----|--------|-----|--------|
| LE | ŌĒ     | D   | ō      |
| Н  | L      | Н   | L      |
| Н  | LES    | L   | THAF   |
| L. | . L    | X   | Ōn     |
| X  | H      | X   | Z      |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Logic(0) or logic(1) must be valid Input Level

 $O_n$  = Previous  $\overline{O}_n$  before high to low transition of latch enable.

'FCT533 is the same as the 'FCT373, except that the out-

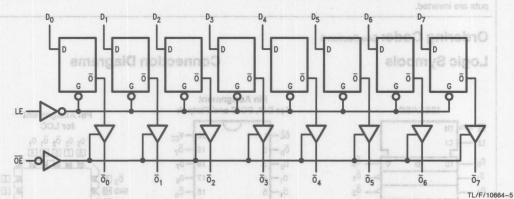
#### Functional Description and STATE AT a

The 'FCT533 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D<sub>n</sub> inputs enters the latches. In this condition the latches are transparent and the latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D in-

IN NSC 54FCT/74FCT533 is pin and functionally equive-

puts a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW the latch contents are presented inverted at the outupts  $\overline{O_7}$ – $\overline{O_0}$ . When  $\overline{OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature Voltage with respect to GND (V<sub>TERM</sub>) 54FCT -0.5V to +7.0V-0.5V to +7.0VTemperature under Bias (T<sub>BIAS</sub>) VS.0 ≥ MV 0HV -55°C to +125°C 74FCT 54FCT -65°C to +135°C Storage Temperature (TSTG) -55°C to +125°C 74FCT (8 e/o//) VA.8 =65°C to +135°C 54FCT 0.5W Power Dissipation (PT) 120 mA

DC Output Current (I<sub>OUT</sub>)

120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

# Conditions Supply Voltage (Vcc)

Junction Temperature (T<sub>J</sub>) 100 yiqque medelud CDIP HeliH atuml JTT 175°C PDIP 140°C

#### **DC Characteristics for FCT Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$   $T_A=-55$ °C to +125°C.

| Symbol          | Parameter pal                       | 54FCT/7                         | 4FCT                           | Units            | 8.1                                      | Conditions   |
|-----------------|-------------------------------------|---------------------------------|--------------------------------|------------------|--|--|
| Symbol          |                                     | Min Typ                         | Max                            | Onits            |  | Conditions   |
| VIH             | Minimum HIGH Level<br>Input Voltage | 2.00 atol/l)<br>xsM = xxV       | Aut                            | ٧                |  |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     | Outputs Oper                    | 0.8                            | V                |  |  |
| lін             | Input High Current                  | LE = Voc<br>1, = 2.5 MHz        | 5.0<br>5.0                     | μА               | V <sub>CC</sub> = Max                    | V <sub>I</sub> = V <sub>CC</sub><br>V <sub>I</sub> = 2.7V (Note 2) |
| l <sub>IL</sub> | Input I ow Current                  | Eight Bits To                   | -5.0<br>-5.0                   | μΑ               | V <sub>CC</sub> = Max                    | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND             |
| loz             | Maximum TRI-STATE<br>Current        | one fine.                       | 10.0<br>10.0<br>-10.0<br>-10.0 | p sno neru<br>μΑ |  | $V_O = 2.7V \text{ (Note 2)}$<br>$V_O = 0.5V \text{ (Note 2)}$     |
| VIK             | Clamp Diode Voltage                 | betreet to =0.7                 | -1.2                           | mil eVari        | V <sub>CC</sub> = Min; I <sub>IN</sub> = | Note 5: Values for these condi Am 81 - a                           |
| los             | Short Circuit Current               | -60 -120                        | )                              | mA               | V <sub>CC</sub> = Max (Not               | e 1); V <sub>O</sub> = GND   |
| V <sub>OH</sub> | Minimum High Level                  | 2.8 3.0                         |                                |                  | V <sub>CC</sub> = 3V; V <sub>IN</sub> =  | = 0.2V or $V_{HC}$ ; $I_{OH} = -32 \mu A$                          |
|                 | Output Voltage                      | V <sub>HC</sub> V <sub>CC</sub> |                                | V                | V <sub>CC</sub> = Min                    | $I_{OH} = -300 \mu\text{A}$  |
|                 |                                     | 2.4 4.3                         |                                |                  | $V_{IN} = V_{IH} \text{ or } V_{IL}$     | $I_{OH} = -12 \text{ mA (Mil)}$                                    |
|                 |                                     | 2.4 4.3                         | (J                             | Line HIRD        | an Japat Transition Pali                 | $I_{OH} = -15  \text{mA}  (\text{Com})$                            |
| VOL             | Maximum Low Level                   | GND                             | 0.2                            | legister Del     | V <sub>CC</sub> = 3V; V <sub>IN</sub> =  | = 0.2V or $V_{HC}$ ; $I_{OL} = 300 \mu A$                          |
|                 | Output Voltage                      | GND                             | 0.2                            | V                |  | $I_{OL} = 300 \mu\text{A}$   |
|                 | Missions and Ic/Ico limits.         | 0.3                             | 0.50                           | astilim inet     | $V_{IN} = V_{IH} \text{ or } V_{IL}$     | I <sub>OL</sub> = 32 mA (Mil)                                      |
|                 |                                     | 0.3                             | 0.50                           |                  |  | I <sub>OL</sub> = 48 mA (Com)                                      |

DC Characteristics for FCT Family Devices and agrilla financia Metabolicada

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$   $T_A=-55$ °C to +125°C. (Continued)

| V85,8 of         | 4.75V                                     | 74FCT            |      | (R)          | with respect to GND (VTER   | Temperature Vollage v                                   |
|------------------|---|------------------|------|--------------|---|---|
| Symbol           | Parameter                                 | Min Typ          | Max  | Units        | /a.o- Cond  | 54FCT ZAFCT   |
| 0"85 # 4         | Maximum Quiescent<br>Supply Current       | 510CH10 0.001    |      | mA +         | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V \\ &f_{I} = 0 \end{aligned}$                          | 74FCT<br>54FCT  |
| ΔI <sub>CC</sub> | Quiescent Supply Current; TTL Inputs HIGH | 0.5              | 2.0  | mA -         | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)  | Storage Lemperatura (<br>74FCT<br>54FCT                 |
| ICCD             | Dynamic Power<br>Supply Current (Note 4)  | 0.25             | 0.45 | mA/MHz       | V <sub>CC</sub> = Max Outputs Open $\overline{\text{OE}} = \text{GND}$ LE = V <sub>CC</sub> One Input Toggling 50% Duty Cycle | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                |
| oulev en         | Total Power<br>Supply Current (Note 6)    | 1.5.1 or lest co | 4.5  |              | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND   | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$                   |
|                  | Conditions                                | 1.8              | 5.0  | ZAFOT<br>Max | LE = V <sub>CC</sub><br>f <sub>I</sub> = 10 MHz  One Bit Toggling 50% Duty Cycle  | V <sub>IN</sub> = 3.4V SI + OI<br>V <sub>IN</sub> = GND |
|                  |   |                  | V    | lin A        | (Note 5)<br>V <sub>CC</sub> = Max   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                |
|                  |   | 3.0              | 8.0  | 8.0          | OE = GND  | IL Maximum L<br>Input Voltag                            |
| ote 2)           | $V_1 = V_{OC}$<br>$V_1 = 2.7V$ (N         | xsM = 30V<br>5.0 | 14.5 | 5.0<br>5.0   | $f_{l} = 2.5 \text{ MHz}$   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND         |
| (ote 2)          | $V_1 = 0.5V (N_2)$ $V_2 = 0.5V (N_3)$     | Voc = Max        | Ац   | 0.3-         | Eight Bits Toggling<br>50% Duty Cycle   | L Input Low C   |
| VH               | Input Hysteresis on LE Only               | 200              |      | mV           | STATE IS  |   |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I<sub>CCD</sub> = 0.40 mA/MHz. Refer to applicable standard military drawing or NSC Table I for test conditions and I<sub>C</sub>/I<sub>CC</sub> limits.

#### AC Electrical Characteristics: See Section 2 for waveforms

| Symbol                               |  | 54FCT/74FCT   | 74               | 74FCT                        |                  | FCT  | noima?                                      |      |
|--------------------------------------|--|---|------------------|------------------------------|------------------|--|---|------|
|                                      | Parameter  | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V         | R <sub>L</sub> = | C = Com<br>= 500Ω<br>= 50 pF | R <sub>L</sub> = | CC = Mil<br>= 500Ω<br>= 50 pF                                | Units                                       | Fig. |
|                                      |  | Typ Min (Note 1) Max Min                                  | Max              | IA OI                        | Octa             |  |   |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay $D_n$ to $\overline{O}_n$        | 6.0   | 1.5              | 10.0                         | 1.5              | 8.5  | ns  | 2-8  |
| t <sub>PLH</sub> of to               | Propagation Delay  LE to O  n                      | 9.0   | 2.0              | 13.0                         | 2.0              | 9.5  | ns<br>ns<br>ang supara                      | 2-8  |
| t <sub>PZH</sub>                     | Output Enable<br>Time                              | pgrif-aph 8.0 vilkog b                                    | 1.5              | is 11.0                      | damentaldia m    | elds 12.5  | c (C an und                                 | 2–11 |
| t <sub>PHZ</sub>                     | Output Disable                                     | 6.0   | 1.5              | 7.0                          | 1.5              | tuatro Islup<br>8.5  | bavotomi<br>pogn <b>s</b> hed               | 2-11 |
| ts                                   | Set Up Time<br>High or Low<br>D <sub>n</sub> to LE | power levels<br>smunity 0.f kV typ<br>product compilent t |                  | uperior per-                 | 2.0              | FOR curpor<br>to a split group<br>34 is the sume<br>averted. | nedibbs n<br>ns <sub>ell</sub><br>supus are | 2–10 |
| tн                                   | HOLD Time<br>High or Low<br>D <sub>n</sub> to LE   | 1.0   | 1.5              |                              | 3.0              | ices sect  | ns  | 2-10 |
| tw                                   | LE Pulse Width<br>High or Low                      | 5.0   | 6.0              |                              | 6.0              | 88   | ns  | 2-9  |

Note 1: Minimum limits are guaranteed but not tested on Propagation Delays

#### Capacitance ( $T_A = +25C$ , f = 1.0 MHz)

| Symbol | Parameter 30       | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| Cin    | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12  | pF    | V <sub>out</sub> = 0V |

**Note:** This parameter is measured at characterization but not tested C<sub>OUT</sub> for 74FCT only.

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# 54FCT/74FCT534 Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'FCT534 is a high-speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{\text{OE}}$ ) are common to all flip-flops. FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance. The 'FCT534 is the same as the 'FCT374 except that the outputs are inverted.

#### **Features**

■ NSC 54/74FCT534 is pin and functionally equivalent to IDT 54/74FCT534

AC Electrical Cinaracteristics: See Section 2 for waveforms

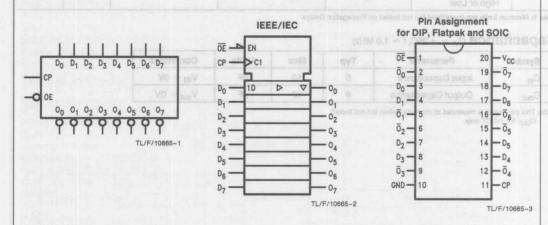
- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD-883

Ordering Code: See Section 8

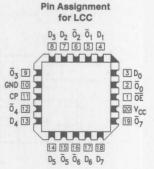
**Logic Symbols** 

#### **Connection Diagrams**

Syn



| Pin Names                         | Description                     |  |  |  |  |
|-----------------------------------|---------------------------------|--|--|--|--|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                     |  |  |  |  |
| CP                                | Clock Pulse Input               |  |  |  |  |
| ŌĒ                                | TRI-STATE Output Enable Input   |  |  |  |  |
| $\overline{O}_0 - \overline{O}_7$ | Complementary TRI-STATE Outputs |  |  |  |  |

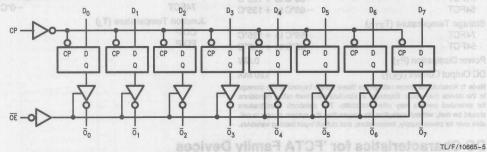


TL/F/10665-4

state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP)

flip-flops.

#### **Logic Diagram**



gulls we Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### **Function Table**

|   |         |                |                     | Acres Office ON a contra of |                          |                          |                                    |     |  |
|---|---------|----------------|---------------------|-----------------------------|--------------------------|--------------------------|------------------------------------|-----|--|
|   | Inputs  |                | Output              | ATO                         |                          |                          |                                    |     |  |
| СР  | OE DED  | D              | OBSINU              | xa3f                        |                          |                          | Paremeter                          |     |  |
| 5   | L<br>L  | H<br>L<br>X    | H<br>O <sub>0</sub> |                             |                          |                          |                                    | HIV |  |
| X   | H       | x              | Z                   | 8,0                         |                          |                          | Maximum Low Level<br>Input Voltage |     |  |
| H = HIGH Voltage L L = LOW Voltage L X = Immaterial = LOW-to-HIGH | evel    |                |                     | 6.0<br>6.0                  |                          |                          |                                    |     |  |
| Z = High Impedanc<br>$\overline{O}_0 = \text{Value stored to}$    | е       | cycle XOM = 00 |                     |                             |                          |                          |                                    |     |  |
| Voc<br>2.7V (Note 2)<br>0.5V (Note 2)<br>GND                      |         | xaM = oc       |                     |                             |                          |                          |                                    |     |  |
|   | - 18 mA |                |                     |                             | -0.7                     |                          |                                    |     |  |
|   |         | co = Max (Not  |                     |                             | -120                     | 09-                      | Short Circuit Gurrent              |     |  |
|   |         |                |                     |                             | 9.0<br>Vcc<br>4.3<br>4.3 | 2.8<br>VHC<br>2.4<br>2.4 |                                    |     |  |
|   |         |                |                     |                             | CHARL                    |                          |                                    |     |  |

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| to GND (V <sub>TERM</sub> )<br>54FCT                    | -0.5V to +7.0V    |
|---|-------------------|
| 74FCT   | -0.5V to $+7.0$ V |
| Temperature Under Bias (T <sub>BIAS</sub> ) 74FCT 54FCT | -55°C to +125°C   |
| Storage Temperature (T <sub>STG</sub> )                 |                   |
| 74FCT   | -55°C to +125°C   |
| 54FCT   | -65°C to +150°C   |
| Power Dissipation (P <sub>T</sub> )                     | 0.5V              |
| DC Output Current (IOUT)                                | 120 m/            |
|   |                   |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

## Recommended Operating molitimus Conditions

| 54FCT   |                                  |
|---|----------------------------------|
| Input Voltage   | OV to V <sub>CC</sub>            |
| Output Voltage  | 0V to V <sub>CC</sub>            |
| Operating Temperature (T <sub>A</sub> )<br>54FCT<br>74FCT | -55°C to +125°C<br>-0°C to +70°C |
| Junction Temperature (T <sub>J</sub> ) CDIP PDIP          | 175°C<br>140°C                   |

#### **DC Characteristics for 'FCTA Family Devices**

Typical values are at  $V_{CC}=5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_{A}=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_{A}=-55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC}=V_{CC}-0.2V$ .

| Symbol           | Parameter                           | 54F                     | CTA/74                        | FCTA                           | Units  | Conditions  |   |  |
|------------------|-------------------------------------|-------------------------|-------------------------------|--------------------------------|--------|---|---|--|
| Symbol           | raiametei                           | Min                     | Тур                           | Max                            | Office | g Col   | nditions  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage | 2.0                     |                               |                                | ٧      | 1 1   |   |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage  |                         |                               | 0.8                            | V 2    | Х   | H X   |  |
| l <sub>IH</sub>  | Input High Current                  |                         |                               | 5.0<br>5.0                     | μΑ     | V <sub>CC</sub> = Max                               | V <sub>I</sub> = V <sub>CC</sub><br>V <sub>I</sub> = 2.7V (Note 2)                                    |  |
| I <sub>I</sub> L | Input Low Current                   |                         |                               | -5.0<br>-5.0                   | μΑ     | V <sub>CC</sub> = Max                               | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND  |  |
| loz              | Maximum TRI-STATE Current           |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μА     | V <sub>CC</sub> = Max                               | $V_{O} = V_{CC}$ $V_{O} = 2.7V \text{ (Note 2)}$ $V_{O} = 0.5V \text{ (Note 2)}$ $V_{O} = \text{GND}$ |  |
| VIK              | Clamp Diode Voltage                 |                         | -0.7                          | -1.2                           | ٧      | $V_{CC} = Min; I_N = -18$                           | mA  |  |
| los              | Short Circuit Current               | -60                     | -120                          | -10                            | mA     | V <sub>CC</sub> = Max (Note 1); V                   | $t_0 = GND$   |  |
| V <sub>OH</sub>  | Minimum High Level                  | 2.8                     | 3.0                           |                                |        | $V_{CC} = 3V; V_{IN} = 0.2V$                        | or $V_{HC}$ ; $I_{OH} = -32 \mu A$  |  |
|                  | Output Voltage                      | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -300 \mu A$<br>$I_{OH} = -12 \text{ mA (Mil)}$<br>$I_{OH} = -15 \text{ mA (Com)}$           |  |
| V <sub>OL</sub>  | Maximum Low Level                   |                         | GND                           | 0.2                            |        | $V_{CC} = 3V; V_{IN} = 0.2V$                        | or $V_{HC}$ ; $I_{OL} = 300 \mu A$  |  |
|                  | Output Voltage                      |                         | GND<br>0.3<br>0.3             | 0.2<br>0.5<br>0.5              | ٧      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 300 \mu\text{A}$ $I_{OL} = 32 \text{mA (Mil)}$ $I_{OL} = 48 \text{mA (Com)}$                |  |

DC Characteristics for 'FCT Family Devices (Continued) Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_{A}=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_{A}=-55$ °C to +125°C, VHC = VCC - 0.2V.

| Symbol     | Parameter                                    | 74FCT   | Units       |           | Cond   | litions   |               |  |
|------------|--|---------|-------------|-----------|--|---|---------------|--|
| yes esta   |  | Min Typ | Min Typ Max |           | Cona   | itions  |               |  |
| lcc<br>8-8 | Maximum Quiescent Supply Current             | 0.001   | 1.5         | mA        | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V \\ &f_I = 0 \end{aligned}$ |   | HJP           |  |
| Δlcc       | Quiescent Supply Current;<br>TTL Inputs HIGH | 0.5     | 2.0         | mA        | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   | Output Enal                                     | PZH           |  |
| ICCD       | Dynamic Power<br>Supply Current (Note 4)     | 0.8     | 0.25        | mA/MHz    | Outputs Open   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        |               |  |
|            | en   |         | 0.8         |           | OE = GND One Input Toggling 50% Duty Cycle   | Set Up Tim<br>Da to CP                          |               |  |
| lc1-S      | Total Power Supply<br>Current (Note 6)       | 1.5     | 4.0         |           | V <sub>CC</sub> = Max<br>Outputs Open<br>f <sub>CP</sub> = 10 MHz<br>$\overline{\text{OE}}$ = GND  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        | 10            |  |
|            |  | 1.8     | 6.0         | n delays. | f <sub>I</sub> = 5 MHz<br>One Bit Toggling<br>50% Duty Cycle                                       | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND | Capac         |  |
|            | conditions<br>Vo = N/V                       |         | - X3        | mA mA     | (Note 5)<br>V <sub>CC</sub> = Max  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        | System<br>CIN |  |
|            | vo = ruo\                                    | 3.0     | 7.8         | r i       | Outputs Open  OE = GND   |   |               |  |
|            |  | 5.0     | 16.8        |           | f <sub>CP</sub> = 10 MHz<br>f <sub>I</sub> = 2.5 MHz<br>Eight Bits Toggling<br>50% Duty Cycle      | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND |               |  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Numbers of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT,  $I_{CCD} = 0.40 \text{ mA/MHz}.$ 

Refer to applicable standard military drawing or NSC Table I for test conditions and I<sub>C</sub>/I<sub>CC</sub> limits.

#### AC Electrical Characteristics: See Section 2 for Waveforms

| O.59 - =         | Mit Voc = 5.0V ± 10%, TA                  | 54FCT/74FCT                                      | 741             | FCT                                | 54F                        | CT                        |       | specific |
|------------------|---|--|-----------------|------------------------------------|----------------------------|---------------------------|-------|----------|
| Symbol Paran     | Parameter                                 | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | N               | / <sub>CC</sub> =<br>//ii<br>50 pF | Com C <sub>L</sub> = 50 pF |                           |       |          |
|                  | XS  | Тур  | Min<br>(Note 1) | Max                                | Min                        | Max<br>receiu0 mi         |       | ool      |
| t <sub>PLH</sub> | Propagation Delay<br>C <sub>P</sub> to On | 0 = 6.5  | 1.5             | 10.0                               |                            | Current                   | ns    | 2-9      |
| t <sub>PZH</sub> | Output Enable<br>Time (8 elo/4) VI        | 0.0 = MA   | 1.5             | 12.5                               | jinenu;                    | ent Supply C<br>outs FIGH |       | 2-11     |
| t <sub>PHZ</sub> | Output Disable Time                       | M = 00 6.0                                       | 1.5             | 8.0                                | (h et                      | ic Power<br>Current (No   | ne    | 2-11     |
| ts               | Set Up Time High or Low<br>Dn to CP       | 10 = 30<br>light en(1.0                          | 2.0             |                                    |                            |                           | ns    | 2-10     |
| t <sub>h</sub>   | Hold Time High or Low<br>Dn to CP         | A = 00 0.5                                       | 1.5             |                                    |                            | ower Supply               | ns ns | 2-10     |
| t <sub>w</sub>   | CP Pulse Width<br>High or Low             | 4.0  | 7.0             | 0.1                                |                            | (d.elc/l) I               | ns    | 2-9      |

Note 1: Maximum test duration not to exceed one se

Note 1: Minimum limits guaranteed but not tested on propagation delays.

#### Capacitance $T_A = +25^{\circ}C$ , $f_I = 1.0 \text{ MHz}$

| Symbol | Parameter          | Тур   | Max    | Units | Conditions            |
|--------|--------------------|-------|--------|-------|-----------------------|
| CIN    | Input Capacitance  | 6     | 10     | pF    | V <sub>IN</sub> = 0V  |
| Cout   | Output Capacitance | 8 000 | 12 8.7 | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested. C<sub>OUT</sub> for 74FCT only.



# 54FCT540 Inverting Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'FCT540 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

The FACT540 is functionally equivalent to the FCT240 while providing broadside pinout.

The FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features undershoot corrector and a split ground bus for superior performance.

#### **Features**

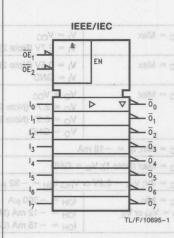
■ NSC 54FCT540 is pin and functionally equivalent to IDT 54FCT540

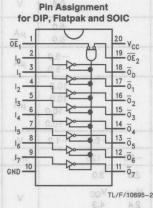
Temperature under Blas (TalAS)

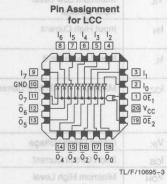
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- CMOS power levels 13 = 55 / 15 to the souley isology.
- 2 kV minimum ESD immunity
- Military product compliant to MIL-STD 883 and Standard Military Drawing #5962-89767

Ordering Code: See Section 8
Logic Symbol

#### Connection Diagrams







#### **Truth Table**

| Pin Names                         | Description                    |
|-----------------------------------|--------------------------------|
| OE <sub>1</sub> , OE <sub>2</sub> | TRI-STATE Output Enable Inputs |
| 10-17                             | Inputs                         |
| $\overline{O}_0 - \overline{O}_7$ | Outputs                        |

| auc             | Output          |    |          |  |
|-----------------|-----------------|----|----------|--|
| OE <sub>1</sub> | OE <sub>2</sub> | In | Outputs  |  |
| E,0 L           | L               | Н  | L        |  |
| Н               | X               | X  | reivet Z |  |
| 100.X           | Н               | X  | Z        |  |
| L               | L               | L  | Н        |  |

- H = HIGH Voltage Level
- L = LOW Voltage Level X = Immaterial
- Z = High Impedance

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage
with Respect to GND (V<sub>TERM</sub>)
54FCT -0.5V to 7.0V

Temperature under Bias (T<sub>BIAS</sub>)
54FCT -65°C to +135°C

Storage Temperature (T<sub>STG</sub>)
54FCT -65°C to +150°C

Power Dissipation (P<sub>T</sub>) 0.5W

DC Output Current (I<sub>OUT</sub>) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

# Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 4.5V to 5.5V

 54FCT
 4.5V to 5.5V

 Input Voltage
 0V to V<sub>CC</sub>

 Output Voltage
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 -55°C to +125°C

 Junction Temperature (T<sub>J</sub>)
 175°C

 CDIP
 140°C

 PDIP
 140°C

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55$ °C to +125°C,  $V_{HC}=V_{CC}-0.2V$ .

| Symbol                                     | Parameter                           | Milliary 1                          | 54FCT                         |                                | Units            | Conditions  |   |  |  |
|--|-------------------------------------|-------------------------------------|-------------------------------|--------------------------------|------------------|---|---|--|--|
| Cymbol                                     | raiameter                           | Min                                 | Тур                           | Max                            | Omto             | 001   | and and an inches   |  |  |
| V <sub>IH</sub>                            | Minimum High Level Input Voltage    | 2.0                                 | noO                           |                                | ٧                | ouer see section 6  | Logic Symb  |  |  |
| V <sub>IL</sub>                            | Maximum Low Level<br>Input Voltage  |                                     | Inome                         | 0.8                            | ٧                | 95.70.70  | 26.70.700   |  |  |
| IIH  | Input High Current                  | 20 Voc                              | CALLED AN                     | 5.0<br>5.0                     | μΑ               | V <sub>CC</sub> = Max   | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |  |  |
| IL 13                                      | Input Low Current                   | 18 062                              | 品                             | -5.0<br>-5.0                   | μА               | V <sub>CC</sub> = Max   | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND  |  |  |
| OZ (15) (15) (15) (15) (15) (15) (15) (15) | Maximum TRI-STATE Current           | 17 01<br>18 02<br>18 03<br>18 03    |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ               | Vcc = Max   | $V_{O} = V_{CC}$ $V_{O} = 2.7V \text{ (Note 2)}$ $V_{O} = 0.5V \text{ (Note 2)}$ $V_{O} = \text{GND}$   |  |  |
| VIK  | Clamp Diode Voltage                 | 13.6                                | -0.7                          | -1.2                           | V                | $V_{CC} = Min; I_N = -18 \text{ mA}$                          |   |  |  |
| los  | Short Circuit Current               | -60                                 | -120                          | 3                              | mA               | V <sub>CC</sub> = Max (Note 1); V <sub>O</sub> = GND          |   |  |  |
| VOH  | Minimum High Level                  | 2.8                                 | 3.0                           |                                | CND -            | $V_{CC} = 3V; V_{IN} = 0.2V$                                  | or $V_{HC}$ ; $I_{OH} = -32 \mu A$  |  |  |
|  | Output Voltage                      | V <sub>HC</sub> 2.4 2.4             | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧                | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$           | $I_{OH} = -300 \mu\text{A}$ $I_{OH} = -12 \text{mA} (\text{Mil})$ $I_{OH} = -15 \text{mA} (\text{Com})$ |  |  |
| VOL  | Maximum Low Level                   |                                     | GND                           | 0.2                            |                  | $V_{CC} = 3V; V_{IN} = 0.2V$                                  | or $V_{HC}$ ; $I_{OL} = 300 \mu A$  |  |  |
| ahuq                                       | Output Voltage                      |                                     | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55            | gni <b>V</b> ida | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$           | $I_{OL} = 300 \mu A$ $I_{OL} = 48 \text{ mA (Mil)}$ $I_{OL} = 64 \text{ mA (Com)}$                      |  |  |
| lcc  | Maximum Quiescent<br>Supply Current |                                     | 0.001                         | 1.5                            | mA               | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2V$ $f_I = 0$ | 1 40-00   |  |  |
| ΔI <sub>CC</sub>                           | Quiescent Supply Current;           | i Veltage U<br>Veltage Lt<br>Meriti | 0.5                           | 2.0                            | mA               | $V_{CC} = Max$ $V_{IN} = 3.4V \text{ (Note 3)}$               |   |  |  |

DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55^{\circ}C$ to +125°C,  $V_{HC} = V_{CC} - 0.2V$ .

| Symbol            | Parameter = 3                            | 54FCT |      | Units | 0.0 = 5.0 Voc = 5.0 | Conditions   |   |       |
|-------------------|--|-------|------|-------|---------------------|--|---|-------|
|                   |  | Min   | Тур  | Max   | Cilita              | 001  | VIIGILIONS                                      |       |
| ICCD<br>8.9       | Dynamic Power<br>Supply Current (Note 4) | .F    | 0.35 | 0.4   | mA/MHz              | V <sub>CC</sub> = Max Outputs Open $\overline{OE}_A = \overline{OE}_B = GND$                       | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$           | TH4   |
| 2-11              | 12.5 ns                                  | 1.5   |      |       |                     | ,, ,   | Output Enab                                     | HZH   |
| Iç <sub>1-S</sub> | Total Power Supply<br>Current (Note 6)   | 1.1   |      | 5.5   |                     | V <sub>CC</sub> = Max Outputs Open   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        |       |
|                   | anolition                                | 0     |      | 6.0   | mA                  | OE <sub>A</sub> = OE <sub>B</sub> = GND  f <sub>I</sub> = 10 MHz  One Bit Toggling  50% Duty Cycle | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND | Capac |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at fi

All currents are milliamps and all frequencies are in megahertz.

### AC Electrical Characteristics: See Section 2 for Waveforms

|                  | 1: Vec = 5.0V ± 10%, TA                            | 54FCT/74FCT  T <sub>A</sub> = +25°C V <sub>CC</sub> = 5.0V |      | 74FCT  |      | 54FCT  |                  |       | apacifia<br>Institution |
|------------------|--|--|------|--|------|--|------------------|-------|-------------------------|
| Symbol           | Parameter  |  |      | T <sub>A</sub> , V <sub>CC</sub> = R <sub>L</sub> = 5 C <sub>L</sub> = 5 | 000Ω | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$ |                  | Units | Fig.                    |
|                  |  | Тур  |      | Min  | Max  | Min  | Max              |       | -                       |
| t <sub>PLH</sub> | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | SQO SW 5.0   | ZHHZ | 0.4 mA   | 0.36 | 1.5  | Curr 2.9 (Note 4 | Youns | 2-8                     |
| t <sub>PZH</sub> | Output Enable Time                                 | 7.0<br>O.7 Duty O  |      |  |      | 1.5  | 12.5             | ns    | 2-11                    |
| t <sub>PHZ</sub> | Output Disable Time                                | ×sM = 6.0  |      | 5.5  |      | 1.5  | 9.5              | ns    | 2-11                    |

#### Capacitance TA = +25°C, f = 1.0 MHz

| Symbol | Parameter (Note)  | Тур | Max   | Units | Conditions    |
|--------|-------------------|-----|-------|-------|---------------|
| CIN    | Input Capacitance | 6   | 8 8 8 | pF    | $V_{IN} = 0V$ |

Note: This parameter is measured at characterization but not tested.



### 54FCT541 Non-Inverting Octal Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'FCT541 is a non-inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

The FCT541 is functionally equivalent to the FCT 241 with the exception of packaging, inputs and outputs are on the opposite side of the package.

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold warm dard military drawing #5962-89766 and secular Isolay T specified for the appropriate device type: Com: Voc = 5.0V ±5%, Mil. Voc = 5.0V ±10%, TA = -55°C (sonamohaque)

FACT FCT features undershoot corrector and split ground bus for superior performance.

#### **Features**

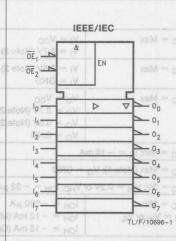
■ NSC 54FCT541 is pin and functionally equivalent to IDT 54FCT541

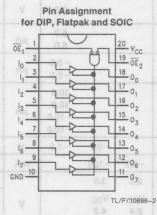
Absolute Maximum Railings (Note 1)

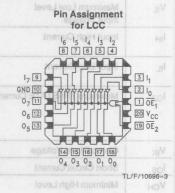
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- IOI = 48 mA
- CMOS power levels
- 2 kV minimum ESD immunity
- Military product compliant to MIL-STD 883 and stan-

Ordering Code: See Section 8 **Logic Symbol** 

#### Connection Diagrams







#### **Truth Table**

| Pin Names                         | Description                    |
|-----------------------------------|--------------------------------|
| OE <sub>1</sub> , OE <sub>2</sub> | TRI-STATE Output Enable Inputs |
| 00-07                             | Outputs                        |

| CINE            | Inputs          | Javali woJ mu<br>Voltage | A SHOW THE REAL PROPERTY OF THE PARTY OF THE |  |  |
|-----------------|-----------------|--------------------------|--|--|--|
| OE <sub>1</sub> | OE <sub>2</sub> | In                       |  |  |  |
| 8.0 L           | L               | Н                        | Н  |  |  |
| H               | X               | X                        | Z  |  |  |
| X               | Н               | M CX escept              | noceM Z ool  |  |  |
| 100.001         | L               | Current                  | Viddos   F   |  |  |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- Z = High Impedance

#### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage
with Respect to GND (V<sub>TERM</sub>)
54FCT -0.5V to 7.0V

Temperature under Bias (T<sub>BIAS</sub>)
54FCT -65°C to +135°C

Storage Temperature (T<sub>STG</sub>)
54FCT -65°C to +150°C

Power Dissipation (P<sub>T</sub>) 0.5W

DC Output Current (I<sub>OUT</sub>) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

# Recommended Operating Conditions

 Supply Voltage (V<sub>CC</sub>)
 4.5V to 5.5V

 54FCT
 4.5V to 5.5V

 Input Voltage
 0V to V<sub>CC</sub>

 Output Voltage
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 -55°C to +125°C

 Junction Temperature (T<sub>J</sub>)
 175°C

 PDIP
 140°C

#### **DC Characteristics for 'FCT Family Devices**

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ , Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55$ °C to +125°C,  $V_{HC} = V_{CC} - 0.2V$ .

| Symbol           | Parameter -                               |  | 54FCT                         |                                | Units             | Conditions  |   |  |
|------------------|---|--|-------------------------------|--------------------------------|-------------------|---|---|--|
| Cymbol           |   | Min                                    | Тур                           | Max                            |                   |   | and malanhad  |  |
| V <sub>IH</sub>  | Minimum High Level Input Voltage          | 2.0                                    | 100                           |                                | ٧                 | Diminos seo sol   | Logic Symbo   |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage           | 2100                                   | Insoming                      | 0.8                            | ٧                 | -   | 884, 70: 20:201   |  |
| I <sub>IH</sub>  | Input High Current                        | 20.                                    |                               | 5.0<br>5.0                     | μΑ                | V <sub>CC</sub> = Max   | $V_I = V_{CC}$ $V_I = 2.7V \text{ (Note 2)}$  |  |
| IL (10)          | Input Low Current                         | 10 012                                 | 12                            | -5.0<br>-5.0                   | μΑ                | V <sub>CC</sub> = Max   | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$   |  |
| loz              | Maximum TRI-STATE Current                 | 18 02<br>18 02<br>18 03                |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ                | V <sub>CC</sub> = Max   | $V_{O} = V_{CC}$ $V_{O} = 2.7V \text{ (Note 2)}$ $V_{O} = 0.5V \text{ (Note 2)}$ $V_{O} = \text{GND}$ |  |
| V <sub>IK</sub>  | Clamp Diode Voltage                       | 13.05                                  | -0.7                          | -1.2                           | ٧                 | $V_{CC} = Min; I_N = -18 \text{ mA}$                                |   |  |
| los              | Short Circuit Current                     | -60                                    | -120                          |                                | mA                | V <sub>CC</sub> = Max (Note 1); V <sub>O</sub> = GND                |   |  |
| V <sub>OH</sub>  | Minimum High Level                        | 2.8 3.0                                |                               |                                | - GN9,            | $V_{CC} = 3V; V_{IN} = 0.2V \text{ or } V_{HC}; I_{OH} = -32 \mu A$ |   |  |
|                  | Output Voltage                            | V <sub>HC</sub> 2.4 2.4                | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧                 | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$                 | $I_{OH} = -300 \mu A$<br>$I_{OH} = -12 \text{ mA (Mil)}$<br>$I_{OH} = -15 \text{ mA (Com)}$           |  |
| VOL              | Maximum Low Level                         |  | GND                           | 0.2                            | -5                | $V_{CC} = 3V; V_{IN} = 0.2$   | $2V \text{ or } V_{HC}; I_{OL} = 300 \mu\text{A}$   |  |
| siuq.            | Output Voltage                            | Ē,                                     | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55            | gril <b>V</b> din | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$                 | $I_{OL} = 300 \mu A$<br>$I_{OL} = 48 \text{ mA (Mil)}$<br>$I_{OL} = 64 \text{ mA (Com)}$              |  |
| lcc s            | Maximum Quiescent Supply Current          | Lengtiny Hi                            | 0.001                         | 1.5                            | mA                | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2V$ $f_1 = 0$       |   |  |
| ΔI <sub>CC</sub> | Quiescent Supply Current; TTL Inputs HIGH | W Veltago L<br>nateriar<br>h Impedanci | 0.5                           | 2.0                            | mA                | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)            |   |  |

DC Characteristics for 'FCT Family Devices (Continued) Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V<sub>CC</sub> = 5.0V ±5%, T<sub>A</sub> = 0°C to +70°C; Mil: V<sub>CC</sub> = 5.0V ±10%, T<sub>A</sub> = -55°C to + 125°C,  $V_{HC} = V_{CC} - 0.2V$ .

| Symbol            | Parameter 3                              | 54FCT |      |      | Units  | 2.8 = 35V Con   | ditions   |                                  |
|-------------------|--|-------|------|------|--------|---|---|----------------------------------|
| Symbol            |  | Min   | Тур  | Max  | Office | Coll  | Conditions  |                                  |
| ICCD<br>8-S       | Dynamic Power<br>Supply Current (Note 4) |       | 0.35 | 0.40 | mA/MHz | V <sub>CC</sub> = Max<br>Outputs Open<br>$\overline{\text{OE}}_{\text{A}} = \overline{\text{OE}}_{\text{B}} = \text{GND}$ | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                              | N1d                              |
|                   | an 12.5 ns                               | .1    |      |      |        | One Input Toggling<br>50% Duty Cycle  | Output Ental  |                                  |
| Iç <sub>1-8</sub> | Total Power Supply<br>Current (Note 6)   |       |      | 5.5  |        | V <sub>CC</sub> = Max<br>Outputs Open<br>$\overline{OE}_A = \overline{OE}_B = GND$  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                              | 219<br>2H3                       |
|                   | ancilitans                               | 0     |      | 6.0  | meM    | f <sub>I</sub> = 10 MHz One Bit Toggling 50% Duty Cycle   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND                       |                                  |
|                   | V0 = N                                   | y I   |      |      | mA     | (Note 5)<br>$V_{CC} = Max$<br>$\overline{OE}_A = \overline{OE}_B = GND$   | $\begin{array}{c} V_{IN} \geq V_{HC} \\ V_{IN} \leq 0.2V \end{array}$ | C <sub>(3)</sub><br>Notes This p |
|                   |  |       |      |      |        | f <sub>I</sub> = 2.5 MHz Eight Bits Toggling 50% Duty Cycle   | V <sub>IN</sub> = 3.4V  |                                  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_{C} = I_{CC} + \Delta I_{CC} D_{H} N_{T} + I_{CCD} (f_{CP}/2 + f_{I} N_{I})$ 

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are milliamps and all frequencies are in megahertz.

# AC Electrical Characteristics: See Section 2 for Waveforms

| : Voc = 5.0V ± 10%, TA = -55°C       |  | 54FCT/74FCT          | 74F              | 74FCT   |     | FCT           | a erit tot be | specifie |  |
|--------------------------------------|--|----------------------|------------------|---|-----|---------------|---------------|----------|--|
| Symbol                               | $ T_{\text{A}} = +25^{\circ}\text{C} $ ool Parameter $ V_{\text{CC}} = 5.0\text{V} $ |                      | R <sub>L</sub> = | $ \begin{array}{cccc} T_{A}, V_{CC} = Com & T_{A}, V_{CC} \\ R_{L} = 500\Omega & R_{L} = 9 \\ C_{L} = 50 \ pF & C_{L} = 9 \end{array} $ |     |               | Units         | Fig.     |  |
|                                      |  | N = V                | Тур              | Min   | Max | Min           | Max           |          |  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub>                                | 5.0 s                | HANAm 05.6       | 0.35  | 1.5 | Our 0.e (Note | ns            | 2-8      |  |
| t <sub>PZL</sub>                     | Output Enable Time   | Trignl and 7.0       |                  |   | 1.5 | 12.5          | ns            | 2-11     |  |
| t <sub>PHZ</sub>                     | Output Disable Time  | xaM =<br>6.0 aug 6.0 | 5.5              |   | 1.5 | 9.5           | ns            | 2-11     |  |

# Capacitance T<sub>A</sub> = +25°C, f = 1.0 MHz

|   | Symbol | Parameter (Note)  | Тур | Max | Units | Conditions    |
|---|--------|-------------------|-----|-----|-------|---------------|
| 1 | CIN    | Input Capacitance | 6   | 8   | pF    | $V_{IN} = 0V$ |

Note: This parameter is measured at characterization but not tested.

# **General Description**

The 'FCT543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

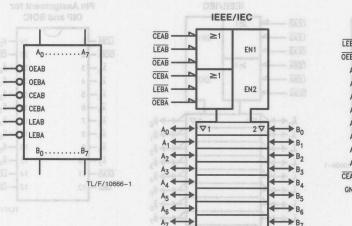
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

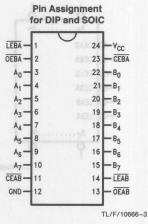
### **Features**

- NSC 54FCT/74FCT543 is pin and functionally equivalent to IDT 54FCT/74FCT543
- Back to back registers for storage
- Separate controls for data flow in each direction
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (com), 48 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

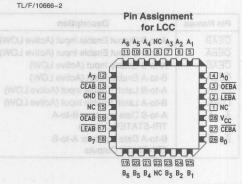
# **Logic Symbols**

# **Connection Diagrams**





| Pin Names                      | Description                             |  |  |  |
|--------------------------------|---|--|--|--|
| OEAB                           | A-to-B Output Enable Input (Active LOW) |  |  |  |
| OEBA                           | B-to-A Output Enable Input (Active LOW) |  |  |  |
| CEAB                           | A-to-B Enable Input (Active LOW)        |  |  |  |
| CEBA                           | B-to-A Enable Input (Active LOW)        |  |  |  |
| LEAB                           | A-to-B Latch Enable Input (Active LOW)  |  |  |  |
| LEBA                           | B-to-A Latch Enable Input (Active LOW)  |  |  |  |
| A <sub>0</sub> -A <sub>7</sub> | A-to-B Data Inputs or                   |  |  |  |
|                                | B-to-A TRI-STATE® Outputs               |  |  |  |
| B <sub>0</sub> -B <sub>7</sub> | B-to-A Data Inputs or                   |  |  |  |
| 1a Z                           | A-to-B TRI-STATE Outputs                |  |  |  |



TL/F/10666-4

6





# 54FCT/74FCT544 Octal Registered Transceiver viscens T benefalos R Isto O

## **General Description**

The 'FCT544 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The 'FCT544 inverts data in both directions.

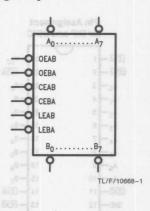
FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold

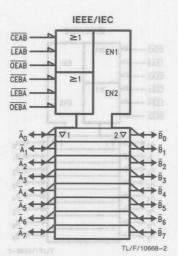
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

### **Features**

- NSC 54FCT/74FCT544 is pin and functionally equivalent to IDT 54FCT/74FCT544
- Back to back registers for storage
- Separate controls for data flow in each direction
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (com), 48 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

# **Logic Symbols**





# **Connection Diagrams**

Pin Assignment for **DIP and SOIC** 



Pin Assignment for LCC

|   | IOI LCC  |  |
|---|--|--|
| Description                               | A <sub>6</sub> A <sub>5</sub> A <sub>4</sub> NC A <sub>3</sub> A <sub>2</sub> A <sub>1</sub> 11 10 9 8 7 6 5         | Pin Nes  |
| A7 12<br>CEAB 13<br>GND 14<br>NC 15       | rgfuO A-ot-8<br>dan3 8-ot-A<br>dan3 A-ot-8<br>fotal A-ot-8<br>sta0 8-ot-A  | 4 A <sub>0</sub> 3 OEBA 2 LEBA 1 NC 28 V <sub>CC</sub> 27 CEBA 26 B <sub>0</sub> |
| ATE® Outputs<br>Inputs or<br>TATE Outputs | 19 20 21 22 23 24 25<br>B <sub>6</sub> B <sub>5</sub> B <sub>4</sub> NC B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> | 8 <sub>0</sub> -8 <sub>7</sub>   |

| B <sub>2</sub> | B <sub>1</sub> |
|----------------|----------------|
|                | TL/F/10668-4   |

| Pin Names                         | Description  |  |  |  |  |
|-----------------------------------|--|--|--|--|--|
| OEAB A                            | A-to-B Output Enable Input (Active LOW)            |  |  |  |  |
| OEBA                              | B-to-A Output Enable Input (Active LOW)            |  |  |  |  |
| CEAB                              | A-to-B Enable Input (Active LOW)                   |  |  |  |  |
| CEBA                              | B-to-A Enable Input (Active LOW)                   |  |  |  |  |
| LEAB                              | A-to-B Latch Enable Input (Active LOW)             |  |  |  |  |
| LEBA                              | B-to-A Latch Enable Input (Active LOW)             |  |  |  |  |
| $\overline{A}_0 - \overline{A}_7$ | A-to-B Data Inputs or B-to-A<br>TRI-STATE® Outputs |  |  |  |  |
| $\overline{B}_0 - \overline{B}_7$ | B-to-A Data Inputs or A-to-B TRI-STATE Outputs     |  |  |  |  |



# 54FCT/74FCT563 Octal Latch with TRI-STATE® Outputs

# **General Description**

The 'FCT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable  $(\overline{OE})$  inputs.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

The 'FCT563 device is functionally identical to the 'FCT573, but with inverted outputs.

### **Features**

- Inputs and outputs on opposite side of package allow easy interface with microprocessors
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels

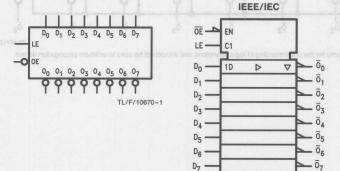
TL/F/10670-2

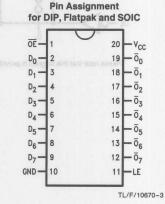
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD-883

Ordering Code: See Section 8

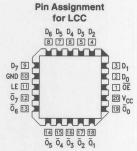
# **Logic Symbols**

# **Connection Diagrams**





| Pin Names                           | Description                   |
|-------------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub>      | Data Inputs                   |
| LE                                  | Latch Enable Input            |
| ŌĒ                                  | TRI-STATE Output Enable Input |
| $\overline{O}_0$ - $\overline{O}_7$ | TRI-STATE Latch Outputs       |



TL/F/10670-4

## **Functional Description**

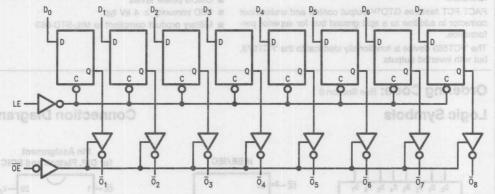
The 'FCT563 contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are in the TRI-STATE mode. When OE is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

### Function Table

|     | Inputs  | B SCORE | Outputs    | Function    |
|-----|---------|---------|------------|-------------|
| ŌE  | LE      | D       | 0          | Tunction    |
| Н   | X       | X       | Z          | High-Z      |
| L   | Н       | COL     | H          | Transparent |
| A T | D. I.H. | H       | a oldban 1 | Transparent |
| L   | L       | X       | NC         | Latched     |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- X = Immaterial
  Z = High Impedance
  NC = No Change NC = No Change

# **Logic Diagram**



TL/F/10670-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTFRM) 54FCT -0.5V to +7.0V-0.5V to +7.0V74FCT Temperature under Bias (TBIAS) -55°C to +125°C 74FCT -65°C to +135°C 54FCT Storage Temperature (TSTG) 74FCT -55°C to +125°C -65°C to +150°C 54FCT Power Dissipation (PT) DC Output Current (IOUT) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

# Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

Supply Voltage (V<sub>CC</sub>) 54FCT 4.5V to 5.5V 74FCT 4.75V to 5.25V Input Voltage OV to Vcc OV to VCC Output Voltage Operating Temperature (TA) -55°C to +125°C 54FCT 74FCT 0°C to +70°C Junction Temperature (TJ) CDIP 175°C PDIP 140°C

### DC Characteristics for 'FCT Family Devices

Typical values are at  $V_{\rm CC} = 5.0$ V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$   $T_A = -55^{\circ}C$ to + 125°C,  $V_{HC} = V_{CC} - 0.2V$ 

| Symbol                            | Parameter                        | SHM 054FCT/7                    | 4FCT                           | Units          | Conditions  |  |
|-----------------------------------|----------------------------------|---------------------------------|--------------------------------|----------------|---|--|
| Symbol                            | Parameter                        | Min Typ                         | Max                            | Onits          | Con   | unions   |
| V <sub>IH</sub>                   | Minimum High Level Input Voltage | 2.0 3 (2014)                    | Are                            | ٧              |   |  |
| VIL                               | Maximum Low Level Input Voltage  | Outputs Open<br>OE = GND        | 0.8                            | 0.8<br>V       | 8   |  |
| lін                               | Input High Current               | LE = Voc                        | 5.0<br>5.0                     | μΑ             | V <sub>CC</sub> = Max   | V <sub>1</sub> = V <sub>CC</sub><br>V <sub>1</sub> = 2.7V (Note 2) |
| I <sub>IL</sub>                   | mpar mon ounone                  | Eight Bits Tog                  | -5.0<br>-5.0                   | μΑ             | V <sub>CC</sub> = Max   | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND             |
| loz                               | Maximum TRI-STATE<br>Current     | emil eno l                      | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ             | beleet ion tud be   | V <sub>O</sub> = 2.7V (Note 2)<br>V <sub>O</sub> = 0.5V (Note 2)   |
| VIK                               | Clamp Diode Voltage              | -0.7                            | -1.2                           | V              | $V_{CC} = Min; I_N = -18 r$   | mA   |
| los                               | Short Circuit Current            | -60 -120                        | )                              | mA             | V <sub>CC</sub> = Max (Note 1); V <sub>C</sub>                              | = GND sample of a stold  |
| V <sub>OH</sub>                   | Minimum High Level               | 2.8 3.0                         |                                |                | $V_{CC} = 3V; V_{IN} = 0.2V$  | or $V_{HC}$ ; $I_{OH} = -32 \mu A$                                 |
|                                   | Output Voltage                   | V <sub>HC</sub> V <sub>CC</sub> |                                | (94,6)         | V <sub>CC</sub> = Min   | $I_{OH} = -300 \mu\text{A}$  |
|                                   |                                  | 2.4 4.3                         | (3%)                           | no HVH nis     | $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OH} = -12 \text{ mA (Mil)}$                                    |
|                                   |                                  | 2.4 4.3                         | (anolve                        | d retrigation  | or Register Devices (Zere for No  | $I_{OH} = -15 \text{mA} \text{(Com)}$                              |
| V <sub>OL</sub> Maximum Low Level |                                  | GND                             | 0.2                            | sherie         | $V_{CC} = 3V; V_{IN} = 0.2V \text{ or } V_{HC}; I_{OL} = 300 \ \mu\text{A}$ |  |
|                                   | Output Voltage                   | GND                             | 0.2                            | V tao V        |   | $I_{OL} = 300 \mu\text{A}$   |
|                                   |                                  | 0.3                             | 0.50                           | 0 1801 103 1 6 | V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>                        | I <sub>OL</sub> = 32 mA (Mil)                                      |
|                                   |                                  | 0.3                             | 0.50                           |                |   | $I_{OL} = 48 \text{ mA (Com)}$                                     |

DC Characteristics for FCT Family Devices (Continued)

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$   $T_A = -55$ °C to +125°C,  $V_{HC} = V_{CC} - 0.2V$ 

| Symbol                  | Parameter                                    | 74F0           | CT       | Units                   | Va.o- Cond   | ditions   |   |
|-------------------------|--|----------------|----------|-------------------------|--|---|---|
| 50V 07 V                | T di dillictoi                               | Min Typ        | Max      | V0.1+ 0                 | V8.0-  | artions   | TAFOT   |
| lcc                     | Maximum Quiescent<br>Supply Current          | 0.00           | 1 1.5    | mA                      | $V_{CC} = Max$ $V_{IN} \ge V_{HC} \le 0.2V$ $f_I = 0$  | zeig tebnu eus<br>i<br>T) stutstagme            | Temperal<br>74FCT<br>54FCT<br>Storage   |
| ΔI <sub>CC</sub>        | Quiescent Supply Current;<br>TTL Inputs HIGH | 0.5            | 2.0      | mA                      | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   |   | 74FCT<br>-54FCT   |
| ICCD                    | Dynamic Power<br>Supply Current (Note 4)     | 0.25           | 5 0.45   | mA/MHz                  | V <sub>CC</sub> = Max<br>Outputs Open<br>$\overline{OE} = GND$<br>LE = V <sub>CC</sub><br>One Input Toggling<br>50% Duty Cycle | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$           | Power Dis<br>DC Output<br>Mate it Abe<br>to the device<br>for extende<br>should be n<br>oble over the |
| lc<br>eulav ar<br>0°63— | Total Power<br>Supply Current (Note 6)       |                | 4.5      | The same of the same of | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND  | $V_{IN} \leq 0.2V$                              |   |
|                         | Conditions                                   | 1.8            | atin 5.0 | TOPACY<br>MAX           | LE = V <sub>CC</sub><br>f <sub>I</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle  | $V_{IN} = 3.4V$ $V_{IN} = GND$                  |   |
|                         |  | 3.0            | 8.0      | 8.0                     | (Note 5)  V <sub>CC</sub> = Max  Outputs Open  OE = GND  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        | 70/   |
| te 2)                   | $V_{i} = V_{00}$<br>$V_{i} = 2.7V$ (No       | M = 50V<br>5.0 | 14.5     | 0.a<br>0.a              | LE = V <sub>CC</sub><br>f <sub>I</sub> = 2.5 MHz   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND | H   |
| ts 2)                   | $x$ $V_1 = 0.5V$ (No $V_2 = GND$             | M = 00V        | Au       | -5.0<br>-5.0            | Eight Bits Toggling<br>50% Duty Cycle  |   | _11   |
| VH                      | Input Hysteresis on LE Only                  | 200            |          | mV                      | STATE  | AT mumbesM                                      | 917   |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

DH = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I<sub>CCD</sub> = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and Ic/Icc limits.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                      |   | 54FCT/74FCT                                     |         | 74FCT                                      | 54FCT  | nimas  |             |
|--------------------------------------|---|---|---------|--|--|--------|-------------|
| Symbol                               | Parameter   | T <sub>A</sub> = 25°C<br>V <sub>CC</sub> = 5.0V | RL      | / <sub>CC</sub> = Com<br>= 500Ω<br>= 50 pF | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$ | Units  | Fig.<br>No. |
|                                      |   | Тур   | Min (   | Note 1) Max                                | Min Max  | 13 (1) | sto C       |
| t <sub>PLH</sub>                     | Propagation Delay $D_n$ to $\overline{O}_n$       | 5.0   | 1.5     | 8.0  | nalisisa   | ns     | 2-8         |
| t <sub>PLH</sub>                     | Propagation Delay<br>LE to On                     | 9.0   | 2.0     | 13.0                                       | in-speed, fow power act<br>Clock (CP) and a but        | ns     | 2-8         |
| t <sub>PZL</sub><br>t <sub>PZH</sub> | Output Enable Time                                | 7.0 To amak                                     | 1.5     | 12.0                                       | The information prese<br>a flip-flops on the LOW-      |        | 2-11        |
| t <sub>PHZ</sub>                     | Output Disable Time                               | THE MESON SOME                                  | = 101.5 | ebivo 7.5                                  | onfoet sense telup 02                                  |        | 2-11        |
| ts                                   | Set Up Tme<br>High or Low<br>D <sub>n</sub> to LE | dyl Val A S ylinum<br>1.0 produced y            | 2.0     |  | GTOTA output control e<br>to a split ground bus to     |        | 2-11        |
| tн                                   | Hold Time<br>High or Low<br>D <sub>n</sub> to LE  | 1.0   | 1.5     | ) the 'ECTS74,                             | is functionally identical to<br>outs.                  | ns led | 2-10        |
| tw                                   | LE Pulse Width<br>High or Low                     | 5.0   | 6.0     |  | tie: See Section 8                                     | ns     | 2-9         |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

# Capacitance $T_A = +25$ °C, f = 1.0 MHz

| Symbol | Parameter          | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | pF    | V <sub>IN</sub> = 0V  |
| Cout   | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

**Note:** This parameter is measured at characterization but not tested. C<sub>OUT</sub> for 74FCT only.

E E E E



# 54FCT/74FCT564 Octal D Flip-Flop with TRI-STATE® Outputs

## **General Description**

The 'FCT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold per-

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior per-

The 'FCT564 device is functionally identical to the 'FCT574, but with inverted outputs.

### **Features**

■ NSC 54FCT/74FCT564 is pin and functionally equivalent to IDT 54FCT/74FCT564

Syn

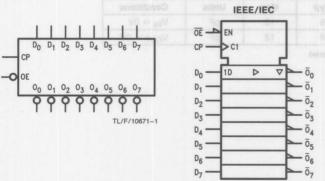
- TRI-STATE outputs for bus-oriented applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military product compliant to MIL-STD 883

Ordering Code: See Section 8

# **Logic Symbols**

# **Connection Diagrams**

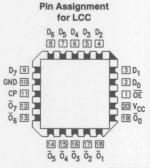
**Pin Assignment** 



| DE -             | EN  |   | -        |   |      |  |
|------------------|-----|---|----------|---|------|--|
| CP —             | >C1 |   | -        |   |      |  |
|                  | 4   |   | 4        |   |      |  |
| 00 —             | 1D  | D | $\nabla$ | − ō <sub>0</sub>  |      |  |
| 01 —             |     |   |          | − ō₁  |      |  |
| 02 -             |     |   |          | − ō <sub>2</sub>  |      |  |
| )3 —             |     |   |          | - ō <sub>3</sub>  |      |  |
| 04 —             |     |   |          | − ō₄  |      |  |
| o <sub>5</sub> — |     |   |          | $-\bar{0}_{2}$ $-\bar{0}_{3}$ $-\bar{0}_{4}$ $-\bar{0}_{5}$ $-\bar{0}_{6}$ $-\bar{0}_{7}$ |      |  |
| o <sub>6</sub> — |     |   |          | − ō <sub>6</sub>  |      |  |
| 7-               |     |   |          | − ō <sub>7</sub>  |      |  |
|                  |     |   | TL       | /F/106  | 71-2 |  |

| GOUTH BROWN        |             |                  |
|--------------------|-------------|------------------|
| 0E-1               | O jugiuo 20 | -V <sub>CC</sub> |
| D <sub>0</sub> - 2 | 19          | $-\bar{o}_0$     |
| D <sub>1</sub> -3  | Vinc18      | -ō1              |
| D <sub>2</sub> - 4 | 17          | $-\bar{o}_2$     |
| D <sub>3</sub> - 5 | 16          | -ō3              |
| D <sub>4</sub> - 6 | 15          | -ō4              |
| $D_5 - 7$          | 14          | -ō <sub>5</sub>  |
| D <sub>6</sub> -8  | 13          | -ō <sub>6</sub>  |
| D <sub>7</sub> — 9 | 12          | - ō <sub>7</sub> |
| ND - 10            | 11          | -CP              |

| Pin Names                         | Description                   |  |  |  |  |  |
|-----------------------------------|-------------------------------|--|--|--|--|--|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                   |  |  |  |  |  |
| CP                                | Clock Pulse Input             |  |  |  |  |  |
| ŌĒ                                | TRI-STATE Output Enable Input |  |  |  |  |  |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Outputs             |  |  |  |  |  |



### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with respect to GND (VTERM) -0.5V to 7.0V 54FCT 74FCT -0.5 to 7.0V Temperature Under Bias (TBIAS) -55°C to +125°C 54FCT -65°C to +135°C Storage Temperature (T<sub>STG</sub>) -55°C to +125°C 74FCT 54FCT -65°C to +150°C

DC Output Current (IOUT) Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Power Dissipation (P<sub>T</sub>)

# Recommended Operating Conditions as well as any man and as a second

Supply Voltage (V<sub>CC</sub>) 4.5V to 5.5V 54FCT 74FCT 4.75V to 5.25V Input Voltage OV to VCC OV to VCC Output Voltage Operating Temperature (TA) -55°C to +125°C 54FCT 74FCT 0°C to +70°C Junction Temperature (T<sub>J</sub>) 175°C PDIP 140°C

# DC Characteristics for 'FCT Family Devices

Typical values are at V<sub>CC</sub> 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}$  5.0V +5%,  $T_A$  = 0°C to +70°; Mil:  $V_{CC}$  = 5.0V ±10%  $T_A$  = 55°C +125°C  $V_{HC}$  = Vcc -0.2V

120 mA

| Symbol          | Parameter                           | SAS E                   | S4FCT/74F                     | СТ                             | Units              | Con  | ditions   |  |
|-----------------|-------------------------------------|-------------------------|-------------------------------|--------------------------------|--------------------|--|---|--|
| Cymbol          | raiameter                           | Min                     | Тур                           | Max                            | Omico              | Conditions                                     |   |  |
| VIH             | Minimum High Level<br>Input Voltage | 2.0                     |                               | 7.8                            | V.s                |  |   |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     | 30<br>907               |                               | 0.8                            | ٧                  |  |   |  |
| IMAS = A        | Input High Current                  | #03<br># #              |                               | 5.0<br>5.0                     | μΑ                 | V <sub>CC</sub> = Max                          | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |  |
| I <sub>IL</sub> | Input Low Current                   | 803                     |                               | -5.0<br>-5.0                   | μА                 | V <sub>CC</sub> = Max                          | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND  |  |
| loz             | Maximum TRI-STATE<br>Current        | Sintact                 | enoliskoles                   | 10.0<br>10.0<br>-10.0<br>-10.0 | μА                 | V <sub>CC</sub> = Max                          | $V_{O} = V_{CC}$ $V_{O} = 2.7V \text{ (Note 2)}$ $V_{O} = 0.5V \text{ (Note 2)}$ $V_{O} = \text{GND}$ |  |
| V <sub>IK</sub> | Clamp Diode Voltage                 |                         | -0.7                          | -1.2                           | ٧                  | $V_{CC} = Min; I_N = -18 r$                    | lote & lo = louissoaut + Am   |  |
| los             | Short Circuit Current               | -60                     | -120                          |                                | mA                 | V <sub>CC</sub> = Max (Note 1); V <sub>C</sub> | O = GND   |  |
| V <sub>OH</sub> | Minimum High Level                  | 2.8                     | 3.0                           |                                | (VA.B              | $V_{CC} = 3V; V_{IN} = 0.2V$                   | or $V_{HC}$ ; $I_{OH} = -32 \mu A$  |  |
|                 | Output Voltage                      | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 | (JHJ                           | V<br>so HJF() sign |  | $I_{OH} = -12  \text{mA}  (Mil)$  |  |
| V <sub>OL</sub> | Maximum Low Level                   | 13.                     | GND                           | 0.2                            | nersign P-ne       | $V_{CC} = 3V; V_{IN} = 0.2V$                   | or V <sub>HC</sub> ; I <sub>OL</sub> = 300 μA   |  |
|                 | Output Voltage                      |                         | GND<br>0.3<br>0.3             | 0.2<br>0.50<br>0.50            | V                  | $V_{IN} = V_{IH} \text{ or } V_{IL}$           | $I_{OH} = 300 \mu A$ $I_{OL} = 32 \text{ mA (Mil)}$ $I_{OL} = 48 \text{ mA (Com)}$                    |  |

DC Characteristics for 'FCT Family Devices (Continued) Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V+5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$   $T_A=-55^{\circ}C$  $+ 125^{\circ}\text{C}; V_{HC} = V_{CC} - 0.2\text{V}$ 

| Symbol Parameter                         |   |                   | 74FCT       |            | Units  | Conditions TO THE   |   |
|--|---|-------------------|-------------|------------|--|---|---|
|  | Parameter   | Min               | Тур         | Max/o      | V of 0.0   |   |   |
| Icc                                      | Maximum Quiescent<br>Supply Current                                 | опаде<br>д Тептро | 0.001       | 1.5°°      | -55°C to +13                                       | $V_{CC} = Max^{T}$ and rebut $V_{IN} \ge V_{HC}$ , $V_{IN} \le 0.2V$ $f_I = 0$  | remperature<br>74FCT<br>54FCT                               |
| ΔI <sub>CC</sub>                         | Quiescent Supply Current;<br>TTL Inputs HIGH                        | Тенциет           | 0.5         | 2.0        | mA)  | $V_{CC} = Max$ $V_{IN} = 3.4V \text{ (Note 3)}$   | Norage Temp<br>74FCT<br>SAFCT                               |
| ICCD                                     | Dynamic Power<br>Supply Current (Note 4)                            |                   | 0.15        | 0.25       | mA/MHz   | V <sub>CC</sub> = Max Outputs Open OE = GND One Input Toggling 50% Duty Cycle   | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V |
| C Total Power<br>Supply Current (Note 6) |   |                   | 1.5         | 4.0        | a ngase masye<br>ishev pobsol hid<br>Kilomas Vi TC | V <sub>CC</sub> = Max Outputs Open OE = GND   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2$                     |
|  |   |                   |             |            |  |   |   |
|  | is shown as Max, use the value 5.0V ±10% T <sub>A</sub> = 55°C +125 |                   |             |            | ent end madn<br>5.0V + 5%, T                       | f <sub>CP</sub> = 10 MHZ<br>f <sub>I</sub> = 5 MHz<br>50% Duty Cycle  |   |
|  |   |                   |             | 100 - 2    | 5.0V +5%, T<br>SAFCT/74FC                          | $f_{CP} = 10 \text{ MHZ}$<br>$f_{I} = 5 \text{ MHz}$  | V <sub>IN</sub> = 3.4\<br>V <sub>IN</sub> = GNI             |
|  | 5.0V ±10% T <sub>A</sub> = 55°C +128                                |                   | 1.8         | 100 - 2    | 5.0V + 5%, T                                       | f <sub>CP</sub> = 10 MHZ<br>f <sub>I</sub> = 5 MHz<br>50% Duty Cycle<br>One Bit Toggling<br>50% Duty Cycle  | V <sub>IN</sub> = GN  |
|  | 5.0V ±10% T <sub>A</sub> = 55°C +128                                |                   | 1.8         | 6.0        | 5.0V +5%, T<br>SAFCT/74FC                          | f <sub>CP</sub> = 10 MHZ<br>f <sub>I</sub> = 5 MHz<br>50% Duty Cycle<br>One Bit Toggling  | V <sub>IN</sub> = GNI                                       |
|  | 5.0V ±10% T <sub>A</sub> = 55°C +128                                |                   | 1.8<br>annu | 6.0        | 5.0V +5%, T<br>SAFCT/74FC                          | f <sub>CP</sub> = 10 MHZ<br>f <sub>I</sub> = 5 MHz<br>50% Duty Cycle<br>One Bit Toggling<br>50% Duty Cycle<br>(Note 5)<br>V <sub>CC</sub> = Max                             | $V_{IN} = GN$ $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$         |
|  | 5.0V ±10% T <sub>A</sub> = 55°C +128                                | © 30V:W           | 1.8         | 6.0<br>7.8 | 5.0V +5%, T<br>SAFCT/74FC                          | f <sub>CP</sub> = 10 MHZ<br>f <sub>I</sub> = 5 MHz<br>50% Duty Cycle<br>One Bit Toggling<br>50% Duty Cycle<br>(Note 5)<br>V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND | $V_{IN} = GN$ $V_{IN} \ge V_{HO}$                           |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC S.1-

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, I<sub>CCD</sub> = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and Ic/Icc limits.

| Symbol Parameter        |  | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V      | -      | = 500Ω<br>= 50 pF   | R <sub>L</sub> = 500Ω<br>C <sub>L</sub> = 50 pF         | Units       | rig.<br>No. |
|-------------------------|--|---|--------|---------------------|---|-------------|-------------|
|                         |  | Тур   | Min (N | ote) Max            | Min Max   | its.I lustr | eto O       |
| t <sub>PLH</sub>        | Propagation Delay<br>CP to $\overline{O}_n$        | 6.6   | 2.0    | 10.0                | noitalio  | ns          | 2-8         |
| t <sub>PZH</sub> of the | Output Enable Time                                 | 9.0   | 1.5    | 12.5                | h-speed ootal latch with b.<br>LE) and buffered commo:  | ns          | 2-11        |
| t <sub>PHZ</sub>        | Output Disable<br>Timed                            | 1 /m   0 6.0 ob cm                                    | 1.5    | 8.0                 | s NSC quiet series techno                               | ns          | 2-11        |
| ts                      | Set-Up Time<br>High or Low<br>D <sub>n</sub> to CP | 8 mA (Com), 82 mA<br>ower lev0.t<br>numity ≥ 4 kV typ | 10.00  |                     | GTOTM output central and<br>to a split ground bus for s | ns          | 2-10        |
| t <sub>H</sub>          | HOLD Time<br>High or Low<br>D <sub>n</sub> to CP   | taly Diagonal # 8065                                  | 2.0    | 373 <u>bu</u> t has | ionally identical to the 'FC'<br>n opposite sides.      | ns          | 2-10        |
| t <sub>W</sub>          | CP Pulse Width<br>High or Low                      | 4.0   | 7.0    | -                   | de: See Section 8                                       | ns          | 2-9         |

Note: Minimum limits are guaranteed but not tested on propagation delays.

# Capacitance (T<sub>A</sub> = +25°C, f = 1.0 MHz)

| Symbol | Parameter          | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

**Note:** This parameter is measured at characterization but not tested. C<sub>OUT</sub> for 74FCT only.

10121 78

00−07 Data Inputs

LE Lotch Enable Input

OE TRI-STATE Output Enable Input

OB-O7 TRI-STATE Latch Outputs



# 54FCT/74FCT573 Octal Latch with TRI-STATE® Outputs

# **General Description**

The 'FCT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

The 'FCT573 is functionally identical to the 'FCT373 but has inputs and outputs on opposite sides.

### **Features**

- NSC 54/74FCT573 is pin and functionally equivalent to IDT 54/74FCT573
- TRI-STATE outputs for bus interfacing

TA = +25°C

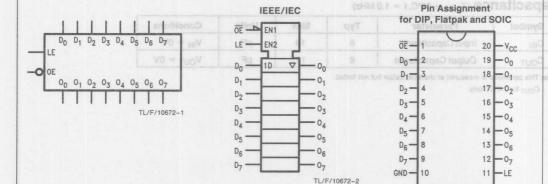
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
   I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- ESD immunity ≥ 4 kV typ
- Military Product compliant to MIL-STD-883 and Standard Military Drawing #5962-88639

Ordering Code: See Section 8

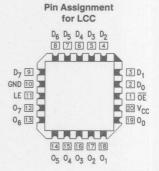
# **Logic Symbols**

# **Connection Diagrams**

Symbol



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| LE                             | Latch Enable Input            |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Latch Outputs       |



TL/F/10672-4

TL/F/10672-3

# Functional Description

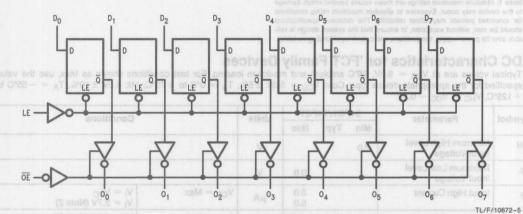
The FCT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_\Pi$  inputs enters the latches. In this condition the latches are transparent, and the latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable  $(\overline{\text{OE}})$  input. When  $\overline{\text{OE}}$  is LOW, the latch contents are presented inverted at the outputs  $\overline{O}_7 - \overline{O}_0$ . When  $\overline{\text{OE}}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

# Truth Table 1167 mumixsM stuloedA

|                | dee specine   | Outputs        |                   |
|----------------|---------------|----------------|-------------------|
| ŌĒ             | eds (LE: Vill | for qualitate  | filce/inorributor |
| L (38          | HUND O        | ith Fleppect I | eminal Holtage v  |
| V0.7 + 01 V2.1 | Н             | L              | Lander            |
| L              | L             | X              | 00                |
| near H         | X             | SHAS X SHAS    | Z                 |

- H = HIGH Voltage
- L = LOW Voltage
- Z = High Impedance
- X = Immaterial  $O_0 = Previous O_0$  before HIGH-to-LOW transition of Latch Enable

## **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| Maximum TRI-STATE<br>Current                 |  | Ац |   |  |
|--|--|----|---|--|
|  |  |    |   |  |
|  |  |    |   |  |
|  |  |    |   |  |
|  |  |    |   |  |
|  |  |    |   |  |
|  |  |    |   |  |
|  |  |    |   |  |
| egsileV tuqhrO                               |  |    |   | $l_{OL} = 800 \mu A$<br>$l_{OL} = 32 mA (Mil)$<br>$l_{OL} = 48 mA (Com)$ |
| Maximum Quiescent<br>Supply Current          |  |    |   |  |
| Quiescent Supply Current:<br>TTL Inputs HIGH |  |    |   |  |
|  |  |    | V <sub>CC</sub> = Max<br>Outputs Open<br>One Input Toggling<br>50% Duty Cycle<br>OT = GND | $V_{\rm H} \leq 0.2 \text{V}$  |

## Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

74FCT — 55°C to + 125°C
Power Dissipation (P<sub>T</sub>) 0.5W

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

DC Ouput Current (IOUT)

# Recommended Operating molecular Conditions

 Supply Voltage (V<sub>CC</sub>)
 4.5V to 5.5V

 54FCT
 4.5V to 5.25V

 74FCT
 4.75V to 5.25V

 Input Voltage
 0V to V<sub>CC</sub>

 Output Voltage
 0V to V<sub>CC</sub>

 Operating Temperature (T<sub>A</sub>)
 −55°C to +125°C

 74FCT
 0°C to +70°C

 Junction Temperature (T<sub>J</sub>)
 175°C

140°C

### **DC Characteristics for 'FCT Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V~\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $5.0V~\pm10\%$ ,  $T_A=-55$ °C to +125°C,  $V_{HC}=V_{CC}-0.2V$ 

120 mA

PDIP

| Symbol           | Parameter                                    | 54              | FCT/74            | FCT                            | Units  |  | Conditions   |  |
|------------------|--|-----------------|-------------------|--------------------------------|--------|--|--|--|
| Syllibol         | Farameter                                    | Min             | Тур               | Max                            | Oilles | Conditions   |  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0             | V                 | 4                              | V      | 内内   | A  |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage              |                 | - ?               | 0.8                            | V      | 91 91  | 1100   |  |
| I <sub>IH</sub>  | Input High Current                           | 0               | 10                | 5.0<br>5.0                     | μА     | V <sub>CC</sub> = Max  | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$  |  |
| IIL              | Input Low Current                            | isu ard In      |                   | -5.0<br>-5.0                   | μΑ     | V <sub>CC</sub> = Max  | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND   |  |
| loz              | Maximum TRI-STATE<br>Current                 |                 |                   | 10.0<br>10.0<br>-10.0<br>-10.0 | μА     | V <sub>CC</sub> = Max  | $V_{O} = V_{CC}$<br>$V_{O} = 2.7V \text{ (Note 2)}$<br>$V_{O} = 0.5V \text{ (Note 2)}$<br>$V_{O} = \text{GND}$ |  |
| V <sub>IK</sub>  | Clamp Doide Voltage                          |                 | -0.7              | -1.2                           | V      | $V_{CC} = Min; I_N = -18 \text{ mA}$   |  |  |
| los              | Short Circuit Current                        | -60             | -120              |                                | mA     | V <sub>CC</sub> = Max (Note 1); V <sub>O</sub> = GND   |  |  |
| V <sub>OH</sub>  | Minimum High Level                           | 2.8             | 3.0               |                                |        | $V_{CC} = 3V; V_{IN} = 0.2V$   | V or $V_{HC}$ ; $I_{OH} = -32 \mu A$   |  |
|                  | Output Voltage                               | V <sub>HC</sub> | Vcc               |                                | V      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OH} = -300 \mu\text{A}$  |  |
|                  |  | 2.4             | 4.3               |                                |        |  | $I_{OH} = -12 \text{ mA (Mil)}$  |  |
|                  |  | 2.4             | 4.3               |                                |        |  | $I_{OH} = -15 \text{ mA (Com)}$  |  |
| VOL              | Maximum Low Level                            |                 | GND               | 0.2                            |        | $V_{CC} = 3V; V_{IN} = 0.2V$   | $V \text{ or } V_{HC}; I_{OL} = 300 \mu A$   |  |
|                  | Output Voltage                               |                 | GND<br>0.3<br>0.3 | 0.2<br>0.50<br>0.50            | ٧      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OL} = 300 \mu A$<br>$I_{OL} = 32 \text{ mA (Mil)}$<br>$I_{OL} = 48 \text{ mA (Com)}$                       |  |
| Icc              | Maximum Quiescent<br>Supply Current          |                 | 0.001             | 1.5                            | mA     | $V_{CC} = Max$<br>$V_{IN} \ge V_{HC}, V_{IN} \le 0.2V$<br>$f_1 = 0$  |  |  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                 | 0.5               | 2.0                            | mA     | $V_{CC} = Max$<br>$V_{IN} = 3.4V \text{ (Note 3)}$   |  |  |
| ICCD             | Dynamic Power<br>Supply Current (Note 4)     |                 | 0.25              | 0.45                           | mA/MHz | V <sub>CC</sub> = Max<br>Outputs Open<br>One Input Toggling<br>50% Duty Cycle<br>$\overline{OE} = GND$<br>LE = V <sub>CC</sub> | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$   |  |

# DC Characteristics for 'FCT Family Devices (Continued)

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V~\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $5.0V~\pm10\%$ ,  $T_A=-55^{\circ}C$  to + 125°C,  $V_{HC} = V_{CC} - 0.2V$ 

| Symbol           | Parameter                              | YOY         | 74FCT |       |   | Con  | ditions   |   |
|------------------|--|-------------|-------|-------|---|--|---|---|
| Symbol Parameter |  | Min Typ Max |       | Units | Note: This paremeter is measured at characterization but not leaded |  |   |   |
| lc               | Total Power<br>Supply Current (Note 6) |             | 1.5   | 4.5   |   | V <sub>CC</sub> = Max Outputs Open OE = GND, LE = V <sub>CC</sub>            | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                              |   |
|                  |  |             | 1.8   | 5.0   |   | m 1  | f <sub>CP</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle        | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND |
|                  |  |             | 3.0   | 8.0   | mA  | (Note 5)  V <sub>CC</sub> = Max Outputs Open  OE = GND, LE = V <sub>CC</sub> | $\begin{array}{c} V_{IN} \geq V_{HC} \\ V_{IN} \leq 0.2V \end{array}$ |   |
|                  |  |             | 5.0   | 14.5  |   | f <sub>CP</sub> = 2.5 MHz<br>Eight Bits Toggling<br>50% Duty Cycle           | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND                       |   |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.

Note 6:  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

DH = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT, ICCD = 0.40 mA/MHz.

Refer to applicable standard military drawing or NSC Table I for test conditions and I<sub>C</sub>/I<sub>CC</sub> limits.

# AC Electrical Characteristics: See Section 2 for Waveforms

|                                      |   | 54/74FCT   | 74               | FCT                    | 541              | FCT                      |       |      |
|--------------------------------------|---|--|------------------|------------------------|------------------|--------------------------|-------|------|
| Symbol                               | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | R <sub>L</sub> = | = Com<br>500Ω<br>50 pF | R <sub>L</sub> = | C = Mil<br>500Ω<br>50 pF | Units | Fig. |
|                                      |   | Тур  | Min (No          | ote) Max               | Min              | Max                      |       |      |
| t <sub>PLH</sub>                     | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 5.0  | 1.5              | 8.0                    | 1.5              | 8.5                      | ns    | 2-8  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>LE to On                         | 9.0  | 2.0              | 13.0                   | 2.0              | 15.0                     | ns    | 2-8  |
| t <sub>PZH</sub>                     | Output Enable Time                                    | 7.0  | 1.5              | 12.0                   | 1.5              | 13.5                     | ns    | 2-11 |
| t <sub>PHZ</sub>                     | Output Disable Time                                   | 6.0  | 1.5              | 7.5                    | 1.5              | 10.0                     | ns    | 2-11 |
| ts                                   | Setup Time High or<br>Low, D <sub>n</sub> to LE       | 1.0  | 2.0              |                        | 2.0              |                          | ns    | 2-10 |
| t <sub>H</sub>                       | Hold Time High or<br>Low, D <sub>n</sub> to LE        | 1.0  | 1.5              |                        | 1.5              |                          | ns    | 2-10 |
| t <sub>W</sub>                       | LE Pulse Width<br>High or Low                         | 5.0  | 6.0              |                        | 6.0              |                          | ns    | 2-9  |

Note: Minimum limits are guaranteed but not tested on propagation delays.

| COUT   | Output Ca | apacitance | 8       | 10     | pF | 7094 | Vol | $_{\rm JT} = 0 V$ | mene9 |  |  |  |
|--|-----------|------------|---------|--------|----|------|-----|-------------------|-------|--|--|--|
| Note: This parameter is measured at characterization but not tested. |           |            | Cantina | 200.00 |    |      |     |                   |       |  |  |  |
| C <sub>OUT</sub> for 74FCT only.                                     |           |            |         |        |    |      |     |                   |       |  |  |  |
|  |           |            |         |        |    |      |     |                   |       |  |  |  |
|  |           |            |         |        |    |      |     |                   |       |  |  |  |
|  |           |            |         |        |    |      |     |                   |       |  |  |  |

Wate it Maximus test duration not to exceed one appoint not make tean one pulput she led at one time.

Bols 2: This paremeter guaranteed but not besut.

Stote 3: Per TTL driven ergot (Veu = 3.4V); all other insuss at Ven or GMD.

Note 4: This parameter is not directly testable, but is nurved for any in Total Power Burpty calculations.

Mote E. Values for these conditions are examples of the fact formula. These lights are guaranteed but not taste

Mote it to = fourteent + transmit = of the stold

to = too + Aloo DaMic + took of = of

top = Oulescant Ourrent

ALCC = Power Supply Current for a TTL High Input (Vig) = 3.1

Dis = Duty Cycle for FTL inputs High

Wr = Number of Inputs at Dis

1000 \* Dynamic Current caused by an input (rationion Pur (nt.))

h = hout Fraguency

the element is reduced at

All currents are in militarros and all frequencies are in magainants

Note 7: For 64PCT, Iorn = 0.40 mAVMHz.

Refer to applicable standard military drawing or MSC Table I for test conditions and fortion limits.

### AC Electrical Characteristics: see seeden 2 for Wavetorns

|  | 742 + + 25°C<br>Voc = 6.0V |  |  |  |
|--|----------------------------|--|--|--|
|  |                            |  |  |  |
|  |                            |  |  |  |
| Propagation Dalay<br>LE to O <sub>n</sub>      |                            |  |  |  |
|  |                            |  |  |  |
|  |                            |  |  |  |
|  |                            |  |  |  |
| Hold Time High or<br>Low, D <sub>n</sub> to LE |                            |  |  |  |
|  |                            |  |  |  |

Note: Minimum limits are quaranteed but not tested on prosecution delays

# 54FCT/74FCT574 Octal D Flip-Flop with TRI-STATE® Outputs

# **General Description**

The 'FCT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

FACT FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

The 'FCT574 is functionally identical to the 'FCT374 except for the pinouts.

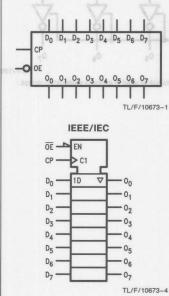
### **Features**

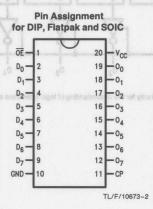
- NSC 54FCT/74FCT574 is pin and functionally equivalent to IDT 54FCT/74FCT574
- Controlled output edge rates and undershoot for improved noise immunity. Internal split ground for improved noise immunity.
- Input clamp diodes to limit bus reflections.
- TTL/CMOS input and output level compatible.
- I<sub>OL</sub> = 48 mA (Com) and 32 mA (Mil)
- CMOS power levels
- ESD immunity ≥ 4kV typ
- Military Product compliant to MIL-STD 883

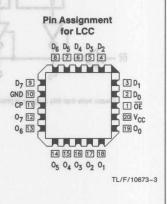
Ordering Code: See Section 8

## **Logic Symbols**

# **Connection Diagrams**







| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| CP                             | Clock Pulse Input             |
| OE                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Outputs             |

# **Functional Description**

The 'FCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

# TFL/CMOS input and output level compatible

### **Function Table**

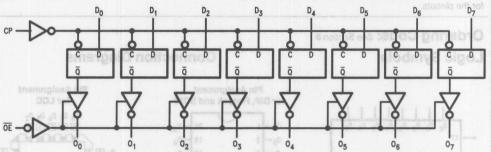
| - 1 | Inputs |   | Internal  | Outputs   | Function          |
|-----|--------|---|-----------|-----------|-------------------|
| ŌĒ  | CP     | D | Q         | ON        | SAFCTA            |
| Н   | Н      | L | NC        | Z         | Hold              |
| Н   | Н      | Н | NC        | Z         | Hold              |
| Н   | _      | L | Laste     | Z         | Load              |
| Н   | 1      | H | Н         | Z         | Load              |
| L   | 5      | L | ed wei be | ods-Joura | Data Available    |
| L   | 5      | H | Н         | Н         | Data Available    |
| L   | Н      | L | NC        | NC        | No Change in Data |
| L   | Н      | Н | NC        | NC        | No Change in Data |

- H = HIGH Voltage Level at 1990 ORM section TOAT
- L = LOW Voltage Level to philipping huntur falue beyondmi
- X = Immaterial
- Z = High Impedance

  = LOW-to-HIGH Transition
- NC = No Change Transition

# **Logic Diagram**

MENGE



TL/F/10673-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

# Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Terminal Voltage with Respect to GNE<br>54FCT<br>74FCT                    | O (V <sub>TERM</sub> )<br>-0.5V to +7.0V<br>-0.5V to +7.0V |
|---|--|
| Temperature under Bias (T <sub>BIAS</sub> )<br>74FCT<br>54FCT             | -55°C to +125°C<br>-65°C to +135°C                         |
| Storage Temperature (T <sub>STG</sub> ) 74FCT 54FCT                       | -55°C to +125°C<br>-65°C to +150°C                         |
| Power Dissipation (P <sub>T</sub> ) DC Output Current (I <sub>OUT</sub> ) | 0.5W<br>120 mA   |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum ratings conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

# Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> )<br>54FCT                | 4.5V to 5.5V                    |
|---|---------------------------------|
| 74FCT   | 4.75V to 5.25V                  |
| Input Voltage   | 0V to V <sub>CC</sub>           |
| Output Voltage  | 0V to V <sub>CC</sub>           |
| Operating Temperature (T <sub>A</sub> )<br>54FCT<br>74FCT | -55°C to +125°C<br>0°C to +70°C |
| CDIP  | ADIA TIT Inputs HDIA            |
| PDIP  | 140°C                           |

DC Characteristics for 'FCT Family Devices Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55$ °C to  $+125^{\circ}$ C,  $V_{HC} = V_{CC} - 0.2V$ 

| Symbol                            | Parameter                           | 5          | 4FCT/74F                      | CT                             | Units                                   | Co   | nditions  |
|-----------------------------------|-------------------------------------|------------|-------------------------------|--------------------------------|---|--|---|
| Cymbol                            | Vote 5)                             | Min        | Тур                           | Max                            | Omico                                   |  | nanono  |
| V <sub>IH</sub> V ≤ 1<br>VS.0 ≥ 1 | Minimum High Level<br>Input Voltage | 2.0        |                               | 7.8                            | 0.0                                     |  |   |
| V <sub>IL</sub>                   | Maximum Low Level Input Voltage     |            |                               | 0.8                            | ٧                                       |  |   |
| I <sub>IH</sub> <sub>AD</sub> =   | Input High Current                  | 5          |                               | 5.0<br>5.0                     | μА                                      | V <sub>CC</sub> = Max  | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| I <sub>IL</sub>                   | Input Low Current                   | .9         | mit and ta bi                 | -5.0<br>-5.0                   | μА                                      | V <sub>CC</sub> = Max  | $V_l = 0.5V \text{ (Note 2)}$<br>$V_l = \text{GND}$   |
| loz                               | Maximum TRI-STATE<br>Current        | insteni io | enchaludisc<br>in fud besini  | 10.0<br>10.0<br>-10.0<br>-10.0 | or GMD.                                 | V <sub>CC</sub> = Max meso us a company of the | $V_{O} = V_{CC}$<br>$V_{O} = 2.7V \text{ (Note 2)}$<br>$V_{O} = 0.5V \text{ (Note 2)}$                  |
| V <sub>IK</sub>                   | Clamp Diode Voltage                 |            | -0.7                          | -1.2                           | V                                       | $V_{CC} = Min; I_N = -18$  | Icc + Culescent CeAm  |
| los                               | Short Circuit Current               | -60        | -120                          |                                | mA                                      | V <sub>CC</sub> = Max (Note 1); \  | O = GND   |
| V <sub>OH</sub>                   | Minimum High Level                  |            | 2.8                           | 3.0                            |   | $V_{CC} = 3V; V_{IN} = 0.2V$   | $'$ or $V_{HC}$ ; $I_{OH} = -32 \mu\text{A}$  |
|                                   | Output Voltage                      |            | V <sub>HC</sub><br>2.4<br>2.4 | V <sub>CC</sub><br>4.3<br>4.3  | Pair (HCH, or<br>on-Fie <b>V</b> star ( | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OH} = -300 \mu\text{A}$ $I_{OH} = -12 \text{mA} (\text{Mil})$ $I_{OH} = -15 \text{mA} (\text{Com})$ |
| V <sub>OL</sub>                   | Maximum Low Level                   |            | GND                           | 0.2                            | shartage                                | $V_{CC} = 3V; V_{IN} = 0.2V$   | $'$ or $V_{HC}$ ; $I_{OL} = 300 \mu\text{A}$  |
|                                   | Output Voltage                      |            | GND<br>0.3<br>0.3             | 0.2<br>0.5<br>0.5              | V see V                                 | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OL} = 300 \mu A$ $I_{OL} = 32 \text{ mA (Mil)}$ $I_{OL} = 48 \text{ mA (Com)}$                      |

DC Characteristics for 'FCT Family Devices Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = {}^{\circ}\text{C}$  to  $+70{}^{\circ}\text{C}$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55{}^{\circ}\text{C}$ to +125°C,  $V_{HC} = V_{CC} - 0.2V$  (Continued)

| Symbol                        | Parameter  | T                                | 74FCT       | Was               | Units                     | Condition   | Terminal Volu                         |  |
|-------------------------------|--|----------------------------------|-------------|-------------------|---------------------------|---|---------------------------------------|--|
| 56V of Vo                     | T didilloto.   | Min                              | Тур         | Max               | or V2.0 —                 | 7AFOT   |                                       |  |
| 20<br>0 + 125°C<br>1to + 70°C | Maximum Quiescent<br>Supply Current                  | Voltage<br>ing Tempi<br>21<br>21 | 0.001       | 1,5 <sub>39</sub> | + 61 mAa -<br>+ 65°C to + | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2V$ $f_I = 0$                 | Feraperature<br>74FOT<br>54FOT        |  |
| ΔI <sub>CC</sub>              | Quiescent Supply Current;<br>TTL Inputs HIGH         | n Tempei                         | 0.5         | 2.0               | + ot mA = -               | $V_{CC} = Max$ $V_{IN} = 3.4V \text{ (Note 3)}$                               | 74FCT<br>54FCT                        |  |
| ICCD                          | Dynamic Power<br>Supply Current (Note 4)             |                                  | 0.15        | 0.25              | mA/MHz                    | V <sub>CC</sub> = Max Outputs Open OE = GND One Input Toggling 50% Duty Cycle | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$ |  |
| lc                            | Total Power Supply Current (Note 6)                  | Ent tool                         | 1.5         | 4.0               |                           | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND                             | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$ |  |
|                               | CQ; Mib V <sub>QQ</sub> = 5.0V ± 10%, T <sub>A</sub> |                                  |             | 8.0V ±59          |                           | $f_{CP} = 10 \text{ MHz}$ $f_{\parallel} = 5.0 \text{ MHz}$ One Bit Toggling  | V <sub>IN</sub> = 3.4\                |  |
|                               | Conditions   |                                  | units Units | 6.0               | SAFFOT/74<br>Am           | 50% Duty Cycle  | V <sub>IN</sub> = GNI                 |  |
|                               | Conditions   |                                  |             | 6.0<br>TON        | mA<br>Typ                 |   |                                       |  |
|                               | Conditions   |                                  |             | TOP               | mA                        | 50% Duty Cycle  (Note 5)  V <sub>CC</sub> = Max  Outputs Open                 |                                       |  |
|                               | Conditions   |                                  |             | FOT<br>Max        | mA<br>qyT nii             | 50% Duty Cycle  (Note 5)  V <sub>CC</sub> = Max                               | V <sub>IN</sub> ≥ V <sub>HC</sub>     |  |

nout Low Gurrant

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_{C} = I_{CC} + \Delta I_{CC} D_{H} N_{T} + I_{CCD} (f_{CP}/2 + f_{I} N_{I})$ 

I<sub>CC</sub> = Quiescent Current 81 - = M mM = acV

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Note 7: For 54FCT,  $I_{CCD} = 0.40 \text{ mA/MHz}$ .

Refer to applicable standard military drawing or NSC Table I for test conditions and  $I_{\rm C}/I_{\rm CC}$  limits.

| <b>AC Electrical</b> | <b>Characteristics:</b> | See Section 2 for Waveforms |
|----------------------|-------------------------|-----------------------------|
|----------------------|-------------------------|-----------------------------|

|  |  | 54FCT/74FCT                                      | 7      | 4FCT                          | 541                             | FCT                         |                  |      |
|--|--|--|--------|-------------------------------|---------------------------------|-----------------------------|------------------|------|
| Symbol   | Parameter  | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$             | RL     | CC = Mil<br>= 500Ω<br>= 50 pF | R <sub>L</sub> =                | = Com<br>500Ω<br>50 pF      | Units            | Fig. |
|  | efuqtuO ®  | Тур  | Min (N | lote) Max                     | Min                             | Max                         | II Trai          | stoC |
| t <sub>PLH</sub> Propagation Delay t <sub>PHL</sub> CP to O <sub>n</sub> |  |  |        | 2.0 10.0                      |                                 | 2.0 11.0                    |                  | 2-8  |
| t <sub>PZL</sub>   | Output Enable Time                               | SAFOTA FOTBAS<br>9.00 a 0.00                     | 1.5    | 12.5                          | 1.5                             | 14.0                        | ns end           | 2-11 |
| t <sub>PHZ</sub>   | Output Disable Time                              | smil be 6.0 bns em                               | 1.5    | 8.0 8.0                       |                                 | 8.0                         | ismins of        | 2-11 |
| t <sub>SU</sub>  | Set-Up Time High or Low Dn to CP                 | MOS input and out 64 mA 0.form), 48 power levels | 2.0    | in (CPAB or                   | 3.5                             |                             | ns<br>exillu TOR | 2-10 |
| <sup>t</sup> H   | Hold Time<br>High or Low<br>D <sub>n</sub> to CP | haliqme tuborq y                                 | 2.0    | t undershoot<br>superior per- | A COLUMN TO SERVICE AND ACCOUNT | etuo MTOTO<br>no filga s of | ns ns            | 2-10 |
| t <sub>W</sub>   | CP Pulse Width<br>High or Low                    | 4.0  | 7.0    |                               | 7.0                             |                             | ns               | 2-9  |

Note: Minimum limits are guaranteed but not tested on propagation delays.

# Capacitance (TA = +25°C, f = 1.0 MHz)

| Symbol | Parameter (Note)   | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured during characterization but not tested. Court for 74FCT only.

> Date Register A Inputs Date Register A Outputs Date Register 8 Inputs

> > Output Enable Input Direction Control Input

s

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# 54FCT/74FCT646 Octal Transceiver/Register with TRI-STATE® Outputs

# **General Description**

The 'FCT646 consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOWto-HIGH transition of the appropriate clock pin (CPAB or

FACTTM FCT utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold

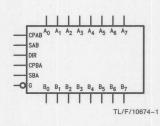
FACT FCT features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

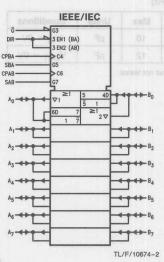
### **Features**

- NSC 54FCT/74FCT646 is pin and functionally equivalent to IDT 54FCT/74FCT646
- Independent registers for A and B buses multiplexed real time and stored time
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD-883

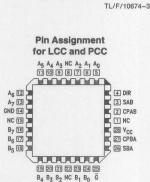
# **Logic Symbols**

# **Connection Diagrams**





|                          |                               | Pin Ass                                  | ignment                                    |
|--------------------------|-------------------------------|--|--|
| IEEE/IEC                 |                               | for DIP, Flat                            | oak and SOIC                               |
| G3<br>3 EN1 (BA)         |                               | CPAB-1                                   | 24 -V <sub>CC</sub>                        |
| 3 EN2 (AB)<br>> C4<br>G5 |                               | SAB — 2<br>DIR — 3                       | 23 — CPBA<br>22 — SBA                      |
| >C6<br>G7                |                               | A <sub>0</sub> 4 5                       | 21 — G<br>20 — B <sub>0</sub>              |
| √1 ≥1 5 4D               | B <sub>0</sub>                | A <sub>2</sub> 6<br>A <sub>3</sub> 7     | 19 — B <sub>1</sub><br>18 — B <sub>2</sub> |
| 6D 7 ≥1<br>1 7 2 ∇       |                               | A <sub>4</sub> - 8<br>A <sub>5</sub> - 9 | 17 —B <sub>3</sub> 16 —B <sub>4</sub>      |
|                          | B <sub>1</sub>                | A <sub>6</sub> —10<br>A <sub>7</sub> —11 | 15 —B <sub>5</sub> 14 —B <sub>6</sub>      |
| ***                      | 4 + 4 + B <sub>3</sub>        | GND — 12                                 | 13 -B <sub>7</sub>                         |
| ***                      | B4                            |  | TL/F/10                                    |
|                          | B <sub>5</sub>                | Pin Ass                                  | ignment                                    |
|                          | B <sub>7</sub> B <sub>7</sub> |  | and PCC                                    |
|                          | ΓL/F/10674-2                  | A <sub>6</sub> 12                        |  |



**Pin Names** Description **Data Register A Inputs**  $A_0 - A_7$ **Data Register A Outputs** B<sub>0</sub>-B<sub>7</sub> Data Register B Inputs Data Register B Outputs CPAB, CPBA Clock Pulse Inputs SAB, SBA Transmit/Receive Inputs G Output Enable Input DIR **Direction Control Input** 

TL/F/10674-4



# Section 7 Contents

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|------|--|
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|      | 54FCT/74FCT241A Octal Buffer/Line Driver with TRI-STATE Outputs  |
|      | 54FCT/74FCT244A Octal Buffer/Line Oriver with TRI-STATE Outputs  |
|      | 54FCT/74FCT245A Octal Buffer/Line Driver with TRI-STATE Outputs  |
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|      | SAFOTY A PROBLEM STATE OF THE S |
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|      |  |
|      | 54FCT/74FCT573A Octal Transparent Latch with TRI-STATE Outputs   |
|      |  |
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|      | 54FCT/74FCT827B 10-9it Buffer/Line Driver with TRI-STATE Outputs   |
|      |  |
|      | SAFCT/74FCT8A1B 10-Bit Transparent Latch with TRI-STATE Outputs  |
|      |  |
|      |  |
|      | S4FCT7/74FCT845A 8-Bit Transparent Latch with TRI-STATE Outputs  |
|      |  |
| 7.90 |  |

# **Section 7 Contents**

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# 54FCT/74FCT138A 1-of-8 Decoder/Demultiplexer

# **General Description**

The 'FCT138A is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'FCT138A devices or a 1-of-32 decoder using four 'FCT138A devices and one inverter.

FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

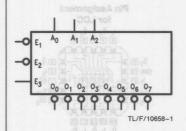
FACT FCTA features undershoot correction and split ground bus for superior performance.

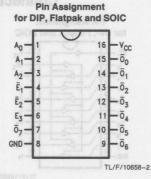
### **Features**

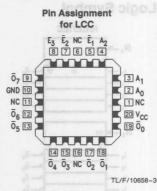
- NSC 54FCT/74FCT138A is pin and functionally equivalent to IDT 54FCT/74FCT138A
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

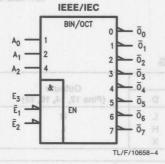
# **Logic Symbol**

# **Connection Diagrams**









| Pin Names                                    | Description    |
|--|----------------|
| A <sub>0</sub> -A <sub>2</sub>               | Address Inputs |
| $A_0-A_2$<br>$\overline{E}_1-\overline{E}_2$ | Enable Inputs  |
| E <sub>3</sub>                               | Enable Input   |
| $\overline{O}_0 - \overline{O}_7$            | Outputs        |

Pln Names Description

OE1, OE2 TRI-STATE Output Enable inputs

10-17 imputs

Oc-O7 Outputs



# 54FCT/74FCT240A Octal Buffer/Line Driver with TRI-STATE® Outputs

# **General Description**

The 'FCT240A is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

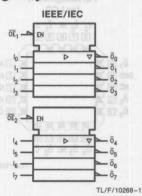
### **Features**

- NSC 54/74FCT240A is pin and functionally equivalent to IDT 54/74FCT240A
- Inverting TRI-STATE outputs drive bus lines or buffer memory address registers

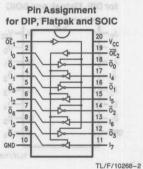
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- I<sub>OL</sub> = 64 mA (commercial) and 48 mA (military)
- Electrostatic discharge protection ≥ 2 kV
- Military product compliant to MIL-STD 883C
- Inherently radiation tolerant

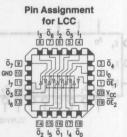
Ordering Code: See Section 8

### Logic Symbol



# Connection Diagrams





TL/F/10268-3

| Pin Names                          | Description                    |
|------------------------------------|--------------------------------|
| $\overline{OE}_1, \overline{OE}_2$ | TRI-STATE Output Enable Inputs |
| 10-17                              | Inputs                         |
| $\overline{O}_0 - \overline{O}_7$  | Outputs                        |

### **Truth Tables**

| Inpu | ts   | Outputs               |
|------|------|-----------------------|
| ŌĒ1  | D o  | (Pins 12, 14, 16, 18) |
| L    | L ao | H H                   |
| L    | H 🔞  | - L                   |
| Н    | X    | Z                     |

| Inpu | ts      | Outputs                                 |
|------|---------|---|
| ŌE2  | D       | (Pins 3, 5, 7, 9)                       |
| L    | nondi   | See Hanney 11/4                         |
| L    | Haugala | A <sub>0</sub> -A <sub>2</sub> J Addres |
| Н    | Xahaqmi | E <sub>1</sub> -E <sub>2</sub> Z Enable |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

# Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTERM) 54FCTA -0.5V to 7.0V 74FCTA -0.5V to 7.0V Temperature under Bias (TBIAS) 74FCTA -55°C to +125°C -65°C to +135°C Storage Temperature (T<sub>STG</sub>)

74FCTA -55°C to +125°C 54FCTA -65°C to +150°C Power Dissipation (PT) 0.5W

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

DC Output Current (IOUT)

# Typical values are at Vcc = **Conditions**

Supply Voltage (V<sub>CC</sub>) 54FCTA 4.5V to 5.5V 74FCTA 4.75V to 5.25V Input Voltage OV to Vcc OV to VCC Output Voltage Operating Temperature (TA) -55°C to +125°C 54FCTA 74FCTA -0°C to +70°C Junction Temperature (T<sub>J</sub>) CDIP 175°C PDIP 140°C

# **DC Characteristics for 'FCTA Family Devices**

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to +125°C, VHC = VCC - 0.2V.

120 mA

| Symbol           | Parameter                                    | 54F                                  | CTA/74                               | FCTA                           | Units              | Cond   | itions  |
|------------------|--|--------------------------------------|--------------------------------------|--------------------------------|--------------------|--|---|
| Symbol           | raidilletei                                  | Min                                  | Тур                                  | Max                            | Office             | er not to exceed our second, and   | Mayon teat rouniyaM st. ptoM  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                                  |                                      |                                | ME 10 001          | where but not tested. ( $V_{\rm DM}=3.4V$ ); all other inputs at 1                                   | Note 2: This parameter guara<br>Note 3: Per TTL driven input  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage              | ations,<br>but not fil               | ipply calcul<br>guaranteed           | 0.8                            | ariT <b>V</b> uana | directly testable, but its derived if<br>sidens are examples of the log to<br>leaster at the masses. | fote 4: This parameter is not<br>fote to Values for these com-<br>date 5: to = franceceus stu-                              |
| IIH              | Input High Current                           |                                      |                                      | 5.0<br>5.0                     | μΑ                 |  | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| I <sub>IL</sub>  | Input Low Current                            |                                      |                                      | -5.0<br>-5.0                   | μΑ                 | V <sub>CC</sub> = Max  | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$   |
| loz              | Maximum TRI-STATE Current                    |                                      |                                      | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ                 |  | $V_{O} = V_{CC}$<br>$V_{O} = 2.7V \text{ (Note 2)}$<br>$V_{O} = 0.5V \text{ (Note 2)}$<br>$V_{O} = \text{GND}$              |
| VIK              | Clamp Diode Voltage                          |                                      | -0.7                                 | -1.2                           | ٧                  | $V_{CC} = Min; I_N = -18 m$  | A   |
| los              | Short Circuit Current                        | -60                                  | -120                                 |                                | mA                 | V <sub>CC</sub> = Max (Note 1); V <sub>O</sub>   | = GND   |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage         | 2.8<br>V <sub>HC</sub><br>2.4<br>2.4 | 3.0<br>V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧                  | 00   | $r V_{HC}$ ; $I_{OH} = -32 \mu A$<br>$I_{OH} = -300 \mu A$<br>$I_{OH} = -12 mA (Mil)$<br>$I_{OH} = -15 mA (Con)$            |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage          |                                      | GND<br>GND<br>0.3<br>0.3             | 0.2<br>0.2<br>0.55<br>0.55     | ٧                  | 00   | $V_{HC}$ ; $I_{OL} = 300 \mu A$<br>$I_{OL} = 300 \mu A$<br>$I_{OL} = 48 \text{ mA (Mil)}$<br>$I_{OL} = 64 \text{ mA (Com)}$ |
| Icc              | Maximum Quiescent<br>Supply Current          |                                      | 0.001                                | 1.5                            | mA                 | $V_{CC} = Max$<br>$V_{IN} \ge V_{HC}, V_{IN} \le 0.2V, f$  | 1 = 0   |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                                      | 0.5                                  | 2.0                            | mA                 | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   |   |

DC Characteristics for 'FCTA Family Devices (Continued) Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55$ °C to +105°C  $V_{CC} = 5.0V \pm 10\%$ ,  $V_{CC} = 5.0V \pm 10\%$ to  $+125^{\circ}$ C,  $V_{HC} = V_{CC} - 0.2$ V.

| Symbol  | Parameter  | 54FC   | TA/74  | 4FCTA  | _ u  | nits   |   | Con  | ditions toage  |  |
|---|--|--|--|--|--|--|---|--|--|--|
| DO V of VO  |  | Min  | Тур  | Max  |  | VO.7 of V  |   | MARKET   | A  |  |
| 0 + 70°C  |  | perature (T  | 0.25   | 04.0   | ) mA   | VO Y of V  | One Inp   | Open (SAGT)  OE <sub>B</sub> = GND  ut Togaling  | A  |  |
| 140°SI  | Total Power Supply<br>Current (Note 6)   |  | 1.5  | 4.5  |  | Am OS t  | f <sub>I</sub> = 10<br>One Bit  | Open<br>OE <sub>B</sub> = GND  | $\begin{aligned} &V_{IN} \geq V_{HC} \\ &V_{IN} \leq 0.2V \end{aligned}$ $\begin{aligned} &V_{IN} = 3.4V \\ &V_{IN} = GND \end{aligned}$               | Power Di<br>DC Outpi<br>Note 1: Abi<br>to the device<br>acception, t |
|   | ons shown as Max, use $V_{\rm CC} = 5.0 V \pm 10\%$ , $T_{\rm A}$  |  |  |  | veQ ş  | littiiii<br>and ma   | (Note 5)<br>$V_{CC} = 0$<br>Outputs<br>$\overline{OE}_A = 0$<br>$f_1 = 2.5$ | Max<br>Open<br><del>OE<sub>B</sub> =</del> GND   | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$  | Typical v<br>specified   |
|   | Conditions   |  | 5.0  | 14.5   | CTA  | TAZZAR   | Eight Bi  | ts Toggling<br>ty Cycle  | $V_{IN} = 3.4V$<br>$V_{IN} = GND$  | ladmy  |
|   | ximum test duration not to excee   | ed one second  | , not m  | ore than o   | one output   | shorted at   | t one time.   |  |  |  |
|   | s parameter guaranteed but not TTL driven input $(V_{IN} = 3.4V)$ ;  |  | s at V <sub>C</sub>  | or GND.  |  |  |   |  | Minimum High L   |  |
| Note 3: Per<br>Note 4: This<br>Note 5: Value  | TTL driven input ( $V_{IN}=3.4V$ ); s parameter is not directly testables for these conditions are exa   | all other inputs<br>ble, but is deriv<br>amples of the lo  | red for i  | use in Tot   | al Power S   |  | culations.  |  |  |  |
| Note 3: Per<br>Note 4: This<br>Note 5: Valu<br>Note 6: I <sub>C</sub> =                   | TTL driven input ( $V_{IN} = 3.4V$ ); s parameter is not directly testable.  | all other inputs<br>ble, but is deriv<br>amples of the Ion<br>(NAMIC)  | red for i  | use in Tot   | al Power S   |  | culations.  | ested.   |  |  |
| Note 3: Per<br>Note 4: This<br>Note 5: Valu<br>Note 6: IC =<br>IC =<br>IC =<br>AIC(<br>DH | TTL driven input (V <sub>IN</sub> = 3.4V); s parameter is not directly testables for these conditions are exa =   QUIESCENT +   INPUTS +   IDY  =   CC + \Delta   CC DHNT +   CCD (fc) =   Quiescent Current   C =   Power Supply Current for a =   Duty Cycle for TTL Inputs Hig  | all other inputs ble, but is deriv amples of the lo (NAMIC p/2 + f NI)   | red for i  | use in Tot   | al Power S<br>e limits are                                       |  | culations.  | isted.   |  |  |
| Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =     | TTL driven input (V <sub>IN</sub> = 3.4V); s parameter is not directly testables for these conditions are exaled a second to the second to | all other inputs ble, but is derivumples of the Ion (NAMIC) by 2 + fi Ni) at TTL High Input gh   | red for the contract of the co   | use in Totula. These   | al Power See limits are  | e guarante   | culations.  | isted. leve  | Input Voltage<br>Maximum Low I<br>Input Voltage<br>Input High Curre  |  |
| Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =     | TTL driven input (V <sub>IN</sub> = 3.4V); s parameter is not directly testables for these conditions are exalled a second to the second t | all other inputs ble, but is deriv imples of the le NAMIC pp/2 + fi Ni) it TTL High Input gh y an Input Tran r Devices (Zero equencies are i   | red for the contract of the co   | use in Totula. These   | al Power See limits are  | e guarante   | culations.  | insted.  Install   | Input Voltage Medinum Lew I Input Voltage Input High Curre Input Low Curre   |  |
| Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =     | TTL driven input (V <sub>IN</sub> = 3.4V); s parameter is not directly testables for these conditions are exalled the state of the seconditions are exalled the state of the seconditions are exalled the state of the second the seco | all other inputs ble, but is deriv imples of the local imples of the local imples of the local imples of the local imples of the local imples input input input imples input i | red for the control of the control o   | use in Totula. These   | al Power See limits are  | e guarante   | culations.  | to the state of th | Input Voltage Medimum Low I Input Voltage Input High Curre Input Low Curre Medimum TRI-5   |  |
| Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =     | TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testables for these conditions are exalled the second to the secon | all other inputs ble, but is derivumples of the long input i | ut (VIN  | use in Totula. These and a second sec | al Power See limits are  | e guarante   | culations.  | tnema 3TATe  | Input Voltage Medinum Low I Input Voltage Input High Curre Input Low Curre Maximum TRI-5 Clamp Diode Vo  |  |
| Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =     | TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testables for these conditions are exale   QuIESCENT +   INPUTS +   IDYIE  | all other inputs ble, but is derivumples of the long manner of the lon | ved for in the control of the contro   | = 3.4V)  Pair (HLH on-Registe  | al Power See limits are  | Property of the control of the contr | culations. ed but not te  | sted. Instance of the stance o | Input Voltage Medimum Low I Input Voltage Input High Curre Input Low Curre Maximum TRI-5 Short Circuit Cu  |  |
| Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =     | TTL driven input (V <sub>IN</sub> = 3.4V); is parameter is not directly testables for these conditions are exalled in the second in the se | all other inputs ble, but is derivumples of the long manner of the long point of the | ved for r<br>coc form<br>that (V <sub>IN</sub><br>that (V <sub>IN</sub> | = 3.4V)  Pair (HLH on-Registe  | al Power \$ e limits are 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8 0.8 | OND<br>CMD<br>CMD<br>CMD<br>CMD<br>CMD<br>CMD<br>CMD   | culations. ed but not te  | sted.  Ins  Ins  Ins  Insert Office of the state of the s | Input Voltage Medimum Lew I Input Voltage Input High Curre Input Low Curre Meximum TRI-5 Short Circuit Cu Cutput Voltage Minimum High I Cutput Voltage |  |

# AC Electrical Characteristics: See Section 2 for Waveforms

|                  |   | 54FCTA/74FCTA                               | 74FCT  | Α   | 54FCT  | A                   |            |             |
|------------------|---|---|--|-----|--|---------------------|------------|-------------|
| Symbol           | Parameter   | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$        | T <sub>A</sub> , V <sub>CC</sub> = R <sub>L</sub> = 50 C <sub>L</sub> = 50 | Ω   | T <sub>A</sub> , V <sub>CC</sub> = R <sub>L</sub> = 50 C <sub>L</sub> = 50 | Ω                   | Units      | Fig.<br>No. |
|                  | stucti  | Тур   | Min (Note 1)   | Max | Min (Note 1)   | Max                 | est la     | 100         |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.5   | 1.5  | 4.8 | 0.00   | enisaar             | ns         | 2-8         |
| t <sub>PZH</sub> | Output Enable Time                                    | TAPETT8.44 le pin                           | 3 08/1.5 of  | 6.2 | ffer and line drive<br>ddress driver, of                                   | an octal by         | ns         | 2-11        |
| t <sub>PHZ</sub> | Output Disable Time                                   | o STATE IST grins<br>leiger as 4.3 y y omar | ni-noi/ # -m<br>s neiflud 1.5  | 5.6 | receiver which   | smitter or density. | nted treat | 2-11        |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

# Capacitance T<sub>A</sub> = +25°C, f = 1.0 MHz

| Symbol | Parameter (Note)   | Тур           | Max | Units | Condition             |
|--------|--------------------|---------------|-----|-------|-----------------------|
| CIN    | Input Capacitance  | riotal 6nemus | 10  | pF    | $V_{IN} = 0V$         |
| Cour   | Output Capacitance | 8             | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

Connection Disgrams

Pin Assignment
for LCC

or LCC



|          | I PARENTI C | energy. |       |    |
|----------|-------------|---------|-------|----|
|          |             |         |       |    |
|          |             |         |       |    |
|          |             |         |       |    |
|          |             |         |       |    |
| g (3     |             |         |       |    |
|          |             |         |       |    |
|          |             | -       |       |    |
|          |             |         |       |    |
|          |             |         |       |    |
|          |             |         | era e | E. |
|          |             |         |       |    |
|          |             |         |       |    |
| 10<br>10 |             |         |       |    |

Ordering Code: See Section 8

lenoHeld RVN

| (Pine 3, 5, 7, 9) |   | OEZ |
|-------------------|---|-----|
|                   |   |     |
|                   | H |     |
|                   |   |     |

Names

OE1, TRI-STATE Output Enable Input
OE2 TRI-STATE Output Enable Input (Active HIGH)
Inputs
Inputs
Ou-O7 Outputs

- HIGH Voltage Lavel - LOW Voltage Lavel - Immeterial



# 54FCT/74FCT241A Octal Buffer/Line Driver with TRI-STATE® Outputs

# **General Description**

The 'FCT241A is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

### **Features**

NSC 54/74FCT241A is pin and functionally equivalent to IDT 54/74FCT241A

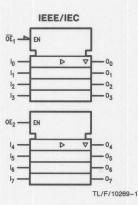
AC Electrical Characteristics: see Section 2 for Waveforms

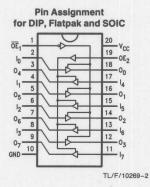
- Non-inverting TRI-STATE outputs drive bus lines or buffer memory address registers
- 'FCT241A has TTL-compatible inputs
- Military product compliant to MIL-STD-883C
- Inherently radiation tolerant
- I<sub>OL</sub> = 64 mA (Comm) and 48 mA (Mil)
- TTL input and output level compatible
- High current latch up

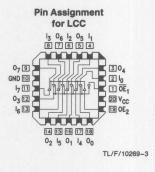
Ordering Code: See Section 8

**Logic Symbol** 

# **Connection Diagrams**







Symbol

| Pin<br>Names                   | Description                                 |
|--------------------------------|---|
| OE <sub>1</sub> ,              | TRI-STATE Output Enable Input               |
| OE <sub>2</sub>                | TRI-STATE Output Enable Input (Active HIGH) |
| I <sub>0</sub> -I <sub>7</sub> | Inputs                                      |
| O <sub>0</sub> -O <sub>7</sub> | Outputs                                     |

### **Truth Tables**

| Inputs            |                      | Outputs |  |  |
|-------------------|----------------------|---------|--|--|
| OE <sub>1</sub> D | (Pins 12, 14, 16, 18 |         |  |  |
| L                 | L                    | L       |  |  |
| L                 | Н                    | Н       |  |  |
| Н                 | X                    | Z       |  |  |

| Inpu              | ts | Outputs           |  |  |
|-------------------|----|-------------------|--|--|
| OE <sub>2</sub> D |    | (Pins 3, 5, 7, 9) |  |  |
| Н                 | L  | L                 |  |  |
| Н                 | Н  | Н                 |  |  |
| L                 | X  | Z                 |  |  |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

# Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTERM) 74FCTA -0.5V to 7.0V 54FCTA -0.5V to 7.0V

Temperature under Bias (T<sub>BIAS</sub>) -55°C to +125°C 74FCTA VS.O Z MV -65°C to +135°C 54FCTA Storage Temperature (T<sub>STG</sub>)

-55°C to +125°C 74FCTA -65°C to +150°C 54FCTA xst// = 00V 0.5W Power Dissipation (PT) negO stugitiO 120 mA

DC Output Current (IOUT)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM FCT circuits outside databook specifications.

# Conditions es va = 50V is era saulay lacigyT

Supply Voltage (V<sub>CC</sub>) 54FCTA 4.5V to 5.5V 74FCTA 4.75V to 5.25V Input Voltage OV to Vcc Output Voltage OV to VCC Dynamic Power Operating Temperature (TA) -55°C to +125°C 54FCTA 74FCTA -0°C to +70°C Junction Temperature (T,J) CDIP 175°C PDIP 140°C

**DC Characteristics for 'FCTA Family Devices** 

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to  $+125^{\circ}$ C,  $V_{HC} = V_{CC} - 0.2V$ 

| Symbol          | Parameter Parameter                          | 54F                     | CTA/74                        | FCTA                           | Units   | Conditions  |   |  |
|-----------------|--|-------------------------|-------------------------------|--------------------------------|---------|---|---|--|
| Symbol          | Slov0 y                                      | Min                     | Тур                           | Max                            | Office  |   |   |  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage          | 2.0                     | V                             | m                              | V       | 20  | H Input Hysteresis on Clock Only  |  |
| V <sub>IL</sub> | Maximum Low Level<br>Input Voltage           | no ilme.                | o la hebbel                   | 0.8                            | V       | Fin , brinder and bearse of<br>befrei fon fud<br>V a valent stock for SV at f | Rote 1; Maximum (est duration not )<br>Note 2; This parameter guaranteed<br>Maria 3; Par 171, drivan lenst (V <sub>m.</sub> m |  |
| IIH             | Input High Current                           |                         | pply caloui<br>poarunteed     |                                | μА      | of got set to ealthware the   | $V_1 = V_{CC}$<br>$V_1 = 2.7V \text{ (Note 2)}$   |  |
| I <sub>IL</sub> | Input Low Current                            |                         |                               | -5.0<br>-5.0                   | μΑ      | V <sub>CC</sub> = Max   | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$   |  |
| loz             | Maximum TRI-STATE Current                    |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ      | 345   | $V_{O} = V_{CC}$<br>$V_{O} = 2.7V \text{ (Note 2)}$<br>$V_{O} = 0.5V \text{ (Note 2)}$<br>$V_{O} = GND$                       |  |
| VIK             | Clamp Diode Voltage                          |                         | -0.7                          | -1.2                           | an Vage | V <sub>CC</sub> = Min; I <sub>N</sub> = -                                     | 18 mA   |  |
| los             | Short Circuit Current                        | -60                     | -120                          |                                | mA      | V <sub>CC</sub> = Max (Note 1   | ); V <sub>O</sub> = GND   |  |
| VOH             | Minimum High Level                           | 2.8 3.0                 |                               |                                |         | $V_{CC} = 3V$ ; $V_{IN} = 0.2V$ or $V_{HC}$ ; $I_{OH} = -32 \mu A$            |   |  |
|                 | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧       | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$                           | $I_{OH} = -300 \mu A$<br>$I_{OH} = -12 \text{ mA (Mil)}$<br>$I_{OH} = -15 \text{ mA (Com)}$                                   |  |
| VoL             | Maximum Low Level                            |                         | GND                           | 0.2                            |         | $V_{CC} = 3V; V_{IN} = 0.$  | .2V or $V_{HC}$ ; $I_{OL} = 300  \mu A$   |  |
|                 | Output Voltage                               |                         | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55            | ٧       | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$                           | $I_{OL} = 300 \mu A$<br>$I_{OL} = 48 \text{ mA (Mil)}$<br>$I_{OL} = 64 \text{ mA (Com)}$                                      |  |
| loc             | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                            | mA      | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0$ $f_I = 0$                    | .2V   |  |
| Δlcc            | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                            | mA      | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)                      |   |  |

# DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V<sub>CC</sub> = 5.0V ±5%, T<sub>A</sub> = 0°C to +70°C; Mil: V<sub>CC</sub> = 5.0V ±10%, T<sub>A</sub> = -55°C to +125°C, VHC = VCC - 0.2V

| Symbol          | Parameter                                | 54FC                  | TA/74 | FCTA | Units                                  | Conditions ATORAT   |   |                          |  |
|-----------------|--|-----------------------|-------|------|--|---|---|--------------------------|--|
| 35000101        | raidilletei                              | Min                   | Тур   | Max  | to 7.0V                                | SAFCTA SHOUTDHOOD -U.SV   |   |                          |  |
| 0751 + 0707 + 0 | Dynamic Power<br>Supply Current (Note 4) | nperatura<br>peratura | 0.25  | 0.40 | mA/MHz                                 | V <sub>CC</sub> = Max Outputs Open $\overline{OE}_A = \overline{OE}_B = GND$ One Input Toggling 50% Duty Cycle            | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$                       |                          |  |
| C               | Total Power Supply<br>Current (Note 6)   |                       | 1.5   | 4.5  | W8.0<br>120 mA                         | V <sub>CC</sub> = Max<br>Outputs Open<br>$\overline{\text{OE}}_{\text{A}} = \overline{\text{OE}}_{\text{B}} = \text{GND}$ | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V |                          |  |
|                 |  |                       | 1.8   | 5.0  | mA                                     | f <sub>I</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND             | los<br>loss<br>med<br>em |  |
|                 |  |                       |       | 8.0  | aCl ylima<br>umixem bris<br>ra± vo.a = | (Note 5)  V <sub>CC</sub> = Max  Outputs Open $\overline{OE}_A = \overline{OE}_B = GND$                                   | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V |                          |  |
|                 | Conditions                               |                       | 5.0   | 14.5 | TAZZECTA                               | f <sub>I</sub> = 2.5 MHz<br>Eight Bits Toggling<br>50% Duty Cycle   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND             |                          |  |
| V <sub>H</sub>  | Input Hysteresis<br>on Clock Only        |                       | 200   | ν .  | mV                                     | 0.S leve.   | Minimum High I  | HIV                      |  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6:  $I_{C} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   $I_{C} = I_{CC} + \Delta I_{CC} D_{H} N_{T} + I_{CCD} (f_{CP}/2 + f_{I} N_{I})$   $I_{CC} = Quiescent Current$ 

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL) f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at fi

All currents are in milliamps and all frequencies are in megahertz.

# AC Electrical Characteristics: See Section 2 for Waveforms

| Symbol Parameter                     |   | 54FCTA/74FCTA                                    | 74FCT  | A            | 54FCT  | Units       | Fig.<br>No. |      |
|--------------------------------------|---|--|--|--------------|--|-------------|-------------|------|
|                                      | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | T <sub>A</sub> , V <sub>CC</sub> = R <sub>L</sub> = 50 C <sub>L</sub> = 50 | Ω            | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$ |             |             |      |
|                                      | atuoti O Typ AT                                       | Min (Note 1)                                     | Max  | Min (Note 1) | Max  |             |             |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.0  | 1.5  | 4.8          | noi  | inisane     | ns          | 2-8  |
| t <sub>PZH</sub>                     | Output Enable Time                                    | ALTARCT O.A Is pin                               | 1.5 of t   | 6.2          | ifter and line drive                                   | an octal bu | ns          | 2-10 |
| t <sub>PHZ</sub>                     | Output Disable Time                                   | 3.0  | 1.5 bev  | 5.6          | eiver which provide                                    | smitter/rec | nent betm   | 2-10 |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

# Capacitance ( $T_A = +25^{\circ}C$ , f = 1.0 MHz)

| Symbol | Parameter (Note)   | Тур          | Max | Units | Conditions            |
|--------|--------------------|--------------|-----|-------|-----------------------|
| CIN    | Input Capacitance  | o lo 6 ord v | 10  | pF    | V <sub>IN</sub> = 0V  |
| Cout   | Output Capacitance | 8            | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.



# 54FCT/74FCT244A Octal Buffer/Line Driver with TRI-STATE® Outputs

# **General Description**

The 'FCT244A is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

### **Features**

■ NSC 54/74FCT244A is pin and functionally equivalent to IDT 54/74FCT244A

AC Electrical Characteristics: See Section 2 for Waveforms

- TRI-STATE outputs drive lines or buffer memory address registers
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- I<sub>OL</sub> = 64 mA (commercial) and 48 mA (military)
- Electrostatic discharge protection ≥ 2 kV

**Connection Diagrams** 

- Military product compliant to MIL-STD 883C
- Inherently radiation tolerant

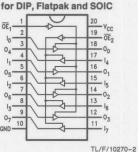
Ordering Code: See Section 8

# **Logic Symbol**

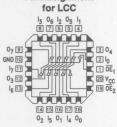
10-17 00-07

# IEEE/IEC OE, --01 02 -05 06 07

# **Pin Assignment**



# **Pin Assignment**



TL/F/10270-3

too my 8

### **Pin Names** Description OE1, OE2 TRI-STATE Output Enable Inputs

Inputs

Outputs

TL/F/10270-1

# **Truth Tables**

| Inputs            |                      | Outputs |  |
|-------------------|----------------------|---------|--|
| OE <sub>1</sub> D | (Pins 12, 14, 16, 18 |         |  |
| L                 | L                    | L       |  |
| L                 | Н                    | Н       |  |
| Н                 | X                    | Z       |  |

| Inpu            | its | Outputs           |
|-----------------|-----|-------------------|
| ŌE <sub>2</sub> | D   | (Pins 3, 5, 7, 9) |
| L               | L   | L                 |
| L               | Н   | Н                 |
| Н               | X   | Z                 |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

# Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V<sub>TERM</sub>)
54FCTA -0.5V to 7.0V
74FCTA -0.5V to 7.0V

DC Output Current (IOUT)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

# Recommended Operating Science Conditions

Supply Voltage (V<sub>CC</sub>) 4.5V to 5.5V 54FCTA 74FCTA 4.75V to 5.25V OV to VCC Input Voltage OV to VCC Output Voltage Operating Temperature (TA) -55°C to +125°C 54FCTA 74FCTA -0°C to +70°C Junction Temperature (T<sub>J</sub>) 175°C CDIP PDIP 140°C

# **DC Characteristics for 'FCTA Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55$ °C to +125°C,  $V_{HC}=V_{CC}-0.2V$ 

120 mA

| Symbol           | OMA Parameter policoot                       | 54F                     | CTA/74                        | FCTA                           | Units       | 18  | Conditions   |                      |
|------------------|--|-------------------------|-------------------------------|--------------------------------|-------------|---|--|----------------------|
| Symbol           | eloyOx                                       | Min                     | Тур                           | Max                            | Oilito      | 7.0   | Conditions   |                      |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                     |                               | (en                            | ٧           | 200   | Input Hysteresis<br>on Clock Only  | H                    |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           | ne time.                | o in behor                    | 0.8                            | V           | od one second, not<br>helied.   | te 1: Maximum test duration not to excel<br>to 2: This parameter guarmined but not   |                      |
| I <sub>IH</sub>  | Input High Current                           | .engili                 | oply carcul                   | 5.0<br>5.0                     | μΑ          | V <sub>CC</sub> = Max   | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$  | lold<br>lold<br>told |
| I <sub>IL</sub>  | Input Low Current                            |                         |                               | -5.0<br>-5.0                   | μΑ          | V <sub>CC</sub> = Max   | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$  | fold                 |
| loz              | Maximum TRI-STATE Current                    |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μA<br>H. μΑ |   | $ \begin{aligned} &V_{l} = V_{CC} \\ &V_{l} = 2.7V \text{ (Note 2)} \\ &V_{l} = 0.5V \text{ (Note 2)} \\ &V_{l} = \text{GND} \end{aligned} $ |                      |
| VIK              | Clamp Diode Voltage                          |                         | -0.7                          | -1.2                           | ٧           | V <sub>CC</sub> = Min; I <sub>N</sub>                                     | $_{\rm I} = -18$ mA of to reduce $^{\rm IM}$   |                      |
| los              | Short Circuit Current                        | -60                     | -120                          |                                | mA          | V <sub>CC</sub> = Max (N  | Note 1); V <sub>O</sub> = GND  |                      |
| V <sub>OH</sub>  | Minimum High Level                           | ım High Level 2.8 3.0   |                               |                                |             | $V_{CC} = 3V; V_{IN} = 0.2V \text{ or } V_{HC}; I_{OH} = -32 \mu\text{A}$ |  |                      |
|                  | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | V           | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IH}$                       | $I_{OH}=-300~\mu A$ $I_{OH}=-12~mA$ (Mil) $I_{OH}=-15~mA$ (Co  |                      |
| VOL              | Maximum Low Level                            |                         | GND                           | 0.2                            |             | $V_{CC} = 3V; V_{II}$   | $_{V} = 0.2V \text{ or } V_{HC}; I_{OL} = 300 \ \mu A$   |                      |
|                  | Output Voltage                               |                         | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55            | V           | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IN}$                       | $I_{OL}=300~\mu A$ $I_{OL}=48~mA~(Mil)$ $I_{OL}=64~mA~(Com)$   | )                    |
| lcc              | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                            | mA          | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{I}$ $f_{I} = 0$                     | N ≤ 0.2V   |                      |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                            | mA          | $V_{CC} = Max$ $V_{IN} = 3.4V (N)$  | lote 3)  |                      |

| Symbol Parameter  | 54FC   | CTA/7  | 4FCTA  | Units   | Va.0-   | (MRSTV) CMO of forces of this egallov i  |  |  |           |
|---|--|--|--|---|---|--|--|--|-----------|
| 20 A 51 A 5   |  | Min Typ Max  |  |   | 10 7.0V   |  |  |  |           |
| OF07 + 6  | Dynamic Power<br>Supply Current (Note 4)   | perature<br>erature  | 0.25   | 0,40  | mA/MHz  | $V_{CC} = M_{C}$ Outputs $C$ $\overline{OE}_{A} = \overline{O}$ One Input 50% Duty   | pen<br>E <sub>B</sub> = GND<br>Toggling  | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V  |           |
| lc o  | Total Power Supply<br>Current (Note 6)   |  | 1.5  | 4.5   | 0.5W<br>120 mA                                      | $V_{CC} = M_0$ Outputs $C$ $\overline{OE}_A = \overline{O}$  |  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$   | Power D   |
|   |  | 1.8  | 5.0  | mA  | f <sub>I</sub> = 10 M<br>One Bit To<br>50% Duty     | oggling  | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND  | to the device<br>exception,<br>lemperatur<br>mend open   |           |
|   | ons shown as Max, use t<br>: V <sub>CC</sub> = 5.0V ± 10%, T <sub>A</sub> =  |  |  |   | arrilly Der   | $\begin{array}{c} \text{(Note 5)} \\ \text{V}_{\text{CC}} = \text{Ma} \\ \text{Outputs C} \\ \hline \overline{\text{OE}}_{\text{A}} = \overline{\text{O}} \end{array}$ |  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$   |           |
|   | Conditions   |  | 5.0  | 14.5  | AVTAFCTA<br>lyp Max                                 | f <sub>I</sub> = 2.5 M<br>Eight Bits<br>50% Duty   | Toggling   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND  |           |
| VH  | Input Hysteresis   |  | 200  | V   | mV  | 20   | Level  | Minimum High   | H         |
|   | on Clock Only  | one secon  |  | ore than on   |   | t one time   | Inces 1  | Input Voltage  | -         |
| Note 1: Max<br>Note 2: This<br>Note 3: Per  | on Clock Only  ximum test duration not to exceed s parameter guaranteed but not te  TTL driven input (V <sub>IN</sub> = 3.4V); al s parameter is not directly testable   | sted.<br>I other inpu  | d, not me  | or GND.   | e output shorted a                                  |  |  | Input Voltage<br>Input Voltage<br>Input High Curr  |           |
| Note 1: Max<br>Note 2: This<br>Note 3: Per<br>Note 4: This<br>Note 5: Valu<br>Note 6: IC =<br>IC =                              | ximum test duration not to exceed s parameter guaranteed but not te TTL driven input ( $V_{\rm IN}=3.4V$ ); al s parameter is not directly testable uses for these conditions are exam = $I_{\rm OUIESCENT}+I_{\rm INPUTS}+I_{\rm DYN}$ , = $I_{\rm CC}+I_{\rm ICC}$ ( $I_{\rm CC}$ ) ( $I_{$ | ested. I other inpute, but is deriples of the  | d, not me  | or GND.<br>use in Total   | e output shorted a                                  | culations.   | ine<br>ed.   | Maximum Low<br>Input Volkage   |           |
| Note 1: Max<br>Note 2: This<br>Note 3: Per<br>Note 4: This<br>Note 5: Vali<br>Note 6: Ic =<br>Ic =<br>Icc =<br>Alc(<br>DH<br>NT | ximum test duration not to exceed a parameter guaranteed but not te TTL driven input (V <sub>IN</sub> = 3.4V); al s parameter is not directly testable uses for these conditions are exam = IouIESCENT + INPUTS + IDYN/= ICC + AICC DHNT + ICCD (TCP/= Quiescent Current C= Power Supply Current for a T= Duty Cycle for TTL Inputs High Number of Inputs at DH= Number of Inputs at DH= Clock Frequency for Register C= Clock Frequency for Register C= Clock Frequency for Register C= TTL Inputs High Puts AID (TTL Inputs High Puts AID) = Dynamic Current Caused by a C= Clock Frequency for Register C= Clock Frequency for Register C= TTL Inputs High Puts AID (TTL Inputs High Puts AID) = Dynamic Current Caused by a Clock Frequency for Register C= TTL Inputs High Puts AID (TTL Inputs High Puts AID) = TTL Inputs High Puts AID (TTL Inputs High Puts AID) = TTL Inputs High Puts AID (TTL Inputs High Puts AID) = TTL Inputs High Puts AID (TTL Inputs High Puts AID (TTL Inputs High Puts AID) = TTL Inputs High Puts AID (TTL Inputs High Puts AID (TTL Inputs High Puts AID) = TTL Inputs High Puts AID (TTL Inputs High Puts AID (TTL Inputs High Puts AID (TTL Inputs High Puts AID) = TTL Inputs High Puts AID (TTL Inpu   | sted. I other input b, but is deri ples of the AMIC 2 + f <sub>1</sub> N <sub>1</sub> ) TL High Input an Input Tra   | d, not mets at V <sub>CC</sub> ived for ulc <sub>CC</sub> form   | c or GND. use in Total ula. These = 3.4V)                           | Power Supply cal                                    | culations.   | ed.  | Maximum Low<br>Input Voltage<br>Input High Curr  | ) 22<br>1 |
| Note 1: Max Note 2: This Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =                  | ximum test duration not to exceed s parameter guaranteed but not te TTL driven input (V <sub>IN</sub> = 3.4V); al s parameter is not directly testable uses for these conditions are exam =  I <sub>QUIESCENT</sub> +  I <sub>INPUTS</sub> +  I <sub>DYN</sub> =  I <sub>CC</sub> + Δ  <sub>ICC</sub> D <sub>H</sub> N <sub>T</sub> +  I <sub>CCD</sub> (f <sub>CP</sub> / = Quiescent Current C = Power Supply Current for a T = Duty Cycle for TTL Inputs High = Number of Inputs at D <sub>H</sub> = Dynamic Current Caused by a = Clock Frequency for Register II Input Frequency = Number of Inputs at f <sub>I</sub>   | sted. I other input be builded by the second | d, not me ts at V <sub>CC</sub> ived for the l <sub>CC</sub> form out (V <sub>IN</sub> separation Pro for No   | c or GND. use in Total ula. These = 3.4V) Pair (HLH or              | Power Supply cal                                    | culations.   | ont sort STATE Current   | Maximum Low<br>Input Vollage<br>Input High Curr<br>Input Low Curry   |           |
| Note 1: Max Note 2: This Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =                  | ximum test duration not to exceed s parameter guaranteed but not te TTL driven input (V <sub>IN</sub> = 3.4V); al s parameter is not directly testable uses for these conditions are exam =   IquiESCENT +   InprUTS +   IDYNJ =   ICC + AICC DHNT +   ICC   (CEV) = Quiescent Current   C = Power Supply Current for a T = Duty Cycle for TTL Inputs High = Number of Inputs at DH   D = Dynamic Current Caused by a = Clock Frequency for Register II.   | sted. I other input, a, but is deriples of the AMIC '2 + f <sub>1</sub> N <sub>1</sub> ) TL High Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon Input Transon   | d, not motived for ulco form   | c or GND. use in Total ula. These = 3.4V) Pair (HLH or              | Power Supply cal<br>limits are guarante             | culations.<br>ed but not test  | ed. ins STATE Current  | Meximum Low<br>Input Voltage<br>Input High Curr<br>Input Low Curre<br>Meximum TRI-5  |           |
| Note 1: Max Note 2: This Note 3: Per Note 4: This Note 5: Vali Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =                  | ximum test duration not to exceed s parameter guaranteed but not te TTL driven input (V <sub>IN</sub> = 3.4V); al s parameter is not directly testable uses for these conditions are exam =   I <sub>QUIESCENT</sub> +   I <sub>INPUTS</sub> +   I <sub>CD</sub> (f <sub>CP</sub> /=   I <sub>CC</sub> + Δ  <sub>ICC</sub> D <sub>H</sub> N <sub>T</sub> +   I <sub>CC</sub> (f <sub>CP</sub> /=   Quiescent Current C = Power Supply Current for a T = Duty Cycle for TTL Inputs High = Number of Inputs at D <sub>H</sub>   D = Dynamic Current Caused by a = Clock Frequency for Register D   Input Frequency = Number of Inputs at f <sub>I</sub> currents are in milliamps and all frequency are in milliamps and all frequency as a constant of the conditions are in milliamps and all frequency as a constant of the conditions are in milliamps and all frequency as a constant of the conditions are in milliamps and all frequency as a condition of the conditions are in milliamps and all frequency as a condition of the conditions are in milliamps and all frequency as a condition of the conditions are exampled to the conditions are exampled t   | sted. I other inpu by but is deriples of the MMIC 2 + f <sub>1</sub> N <sub>1</sub> ) TL High Inpu an Input Tra pevices (Zei   | ts at V <sub>CC</sub> ived for tl <sub>CC</sub> form  out (V <sub>IN</sub> :   | or GND. use in Total ula. These  = 3.4V)  air (HLH or n-Register    | Power Supply cal limits are guarante                | culations. ed but not test   | ent instruction of the period  | Maximum Low<br>Input Voltage<br>Input High Cum<br>Input Low Cum<br>Maximum TRI-S<br>Clamp Diode V                                      |           |
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| Note 1: Max Note 2: This Note 3: Per Note 4: This Note 5: Valid Note 6: IC = IC = IC = IC = IC = IC = IC = IC =                 | ximum test duration not to exceed a parameter guaranteed but not te TTL driven input (V <sub>IN</sub> = 3.4V); al s parameter is not directly testable uses for these conditions are exame   Iquilescent + IInputs + IDYNJ = I <sub>CC</sub> + AI <sub>CC</sub> D <sub>H</sub> N <sub>T</sub> + I <sub>CCD</sub> (f <sub>CP</sub> /= Quiescent Current C = Power Supply Current for a T = Duty Cycle for TTL Inputs High = Number of Inputs at D <sub>H</sub> D = Dynamic Current Caused by a Clock Frequency   Number of Inputs at f <sub>I</sub> currents are in milliamps and all frequency   Number of Inputs at f <sub>I</sub> currents are in milliamps and all frequency  | sted. I other inpu  by but is deriples of the  stance  continued to the co | ts at V <sub>CC</sub> form  out (V <sub>IN</sub> :  unsition Fro for No  | c or GND. use in Total ula. These  = 3.4V) Pair (HLH or on-Register | Power Supply cal                                    | culations.  ed but not test  | ed.  Institute Consent  against them.  Institute Consent  against them.  | Maximum Low Input Voltage Input High Curr Input Low Curr Maximum TRI-S Short Circuit Cu Ninimum High Output Voltage                    |           |
| Note 1: Max Note 2: This Note 3: Per Note 4: This Note 5: Valid Note 6: IC = IC = IC = IC = IC = IC = IC = IC =                 | ximum test duration not to exceed a parameter guaranteed but not te TTL driven input (V <sub>IN</sub> = 3.4V); al s parameter is not directly testable uses for these conditions are exame =   Iquilescent +   Inputs +   IpyNe   Icc + A cc Dh NT +   Icc) (fcp/ = Quiescent Current c = Power Supply Current for a T = Duty Cycle for TTL Inputs High = Number of Inputs at Dh = Dynamic Current Caused by a = Clock Frequency for Register Description   Input Frequency   Number of Inputs at figurernts are in milliamps and all frequency   Input Frequenc   | sted. I other inpu a, but is deri ples of the AMIC 2 + f <sub>1</sub> N <sub>1</sub> ) TL High Inp TL High Input Tra Devices (Zei  | ts at V <sub>CC</sub> ived for a l <sub>CC</sub> form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> substitute of the local form out (V <sub>IN</sub> s | c or GND. use in Total ula. These  = 3.4V) Pair (HLH or on-Register | Power Supply cal limits are guarante  LHL) Devices) | culations. ed but not test   | STATE Current oftage unant Level   | Maximum Low Input Voltage Input High Curr Input Low Curr Maximum TRI-S Short Circuit Cu Output Voltage Maximum High Output Voltage     |           |

### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |   | 54FCTA/74FCTA                                    | 74FCTA   | 54FCTA  | read S |      |
|------------------|---|--|--|---|--------|------|
| Symbol           | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | $T_A$ , $V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50 pF$ | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$      | Units  | Fig. |
|                  |   | Тур  | Min (Note 1) Max                                       | Min (Note 1) Max  | IA Ic  | mo   |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 3.1  | 1.5 4.8  | -STATE® Inp   | ns     | 2-8  |
| t <sub>PZH</sub> | Output Enable Time                                    | 3.8  | 1.5 6.2  | escription  | ns     | 2-11 |
| t <sub>PHZ</sub> | Output Disable Time                                   | AVARCES EN                                       | TGI of 1.5 -ho-au 5.6                                  | contains eight non-invertion<br>STATE outputs and is Intent | ns     | 2-11 |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

### Capacitance ( $T_A = +25$ °C, f = 1.0 MHz)

| Symbol | Parameter (Note)   | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

Connection Diagrams

TRACKER

Ordering Code: See Section 8

ports to A ports. The Out

Logic Symbols

75 — 63 75 — 63 75 — 63 (m)

f-ITSONTLIT

Pln
Names

Description

Output Enable Input

T/R

Transmit/Receive Input
Ao-Ar

Side A Inputs or TRISTATE Outputs

Fruth Table

|                     | FINT |  |  |
|---------------------|------|--|--|
| Bus B Data to Bus A | 1    |  |  |
|                     |      |  |  |
|                     | X    |  |  |



### 54FCT/74FCT245A **Octal Bidirectional Transceiver** with TRI-STATE® Inputs/Outputs

### **General Description**

The 'FCT245A contains eight non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. The Transmit/Receive (T/R) input determines the direction of data flow through 'he bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a HIGH Z condi-

### **Features**

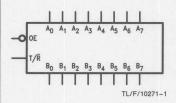
■ NSC 54/74FCT245A is pin and functionally equivalent to IDT 54/74FCT245A

Symbol

- Non-inverting buffers
- Bidirectional data path
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up immunity
- I<sub>OL</sub> = 64 mA (commercial) and 48 mA (military)
- Electrostatic discharge protection ≥ 2 kV
- Military product compliant to MIL-STD 883C
- Inherently radiation tolerant

Ordering Code: See Section 8

### **Logic Symbols**



| Pin<br>Names                   | Description                            |
|--------------------------------|--|
| ŌĒ                             | Output Enable Input                    |
| T/R                            | Transmit/Receive Input                 |
| A <sub>0</sub> -A <sub>7</sub> | Side A Inputs or TRI-<br>STATE Outputs |
| B <sub>0</sub> -B <sub>7</sub> | Side B Inputs or TRI-<br>STATE Outputs |

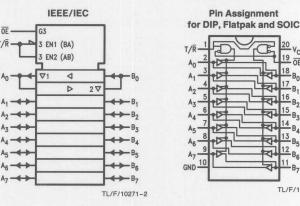
### **Truth Table**

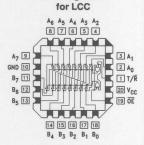
| Inputs |     | Outputs             |
|--------|-----|---------------------|
| ŌĒ     | T/R | Outputs             |
| L      | L   | Bus B Data to Bus A |
| L      | Н   | Bus A Data to Bus B |
| Н      | X   | HIGH-Z State        |

H = HIGH Voltage Level L = LOW Voltage Level

X = Immaterial

### **Connection Diagrams**





**Pin Assignment** 

TL/F/10271-4

19 OE

TL/F/10271-3

140°C

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTERM) -0.5V to 7.0V 54FCTA 74FCTA -0.5V to 7.0V Temperature under Bias (TBIAS) V3.0 > 11 V -55°C to +125°C 74FCTA 54FCTA -65°C to +135°C Storage Temperature (TSTG) -55°C to +125°C 74FCTA 54FCTA Power Dissipation (PT)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM FCT circuits outside databook specifications.

DC Output Current (IOUT)

# Recommended Operating Conditions

Supply Voltage (Vcc) 54FCTA 4.5V to 5.5V 74FCTA 4.75V to 5.25V Input Voltage OV to Vcc OV to Vcc Output Voltage Operating Temperature (TA) -55°C to +125°C 54FCTA 74FCTA 0°C to +70°C Junction Temperature (T<sub>J</sub>) CDIP 175°C

### **DC Characteristics for 'FCTA Family Devices**

Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55$ °C to +125°C,  $V_{HC} = V_{CC} - 0.2V$ .

120 mA

PDIP

| Symbol                     | Parameter                               | 54FC                        | 54FCTA/74FCTA                 |                     |             | Conditions  |   |
|----------------------------|---|-----------------------------|-------------------------------|---------------------|-------------|---|---|
| Symbol                     | and smy                                 | Min                         | Тур                           | Max                 | Units       | Conditions  |   |
| V <sub>IH</sub>            | Minimum High Level Input Voltage        | 2.0                         | VC<br>Ov                      |                     | 0.8 V       | 3.0   |   |
| VIL                        | Maximum Low Level Input Voltage         | R = 06 =<br>= 2.5 MHz       |                               | 0.8                 | V           |   |   |
| Ін                         | Input High Current<br>(except I/O Pins) | oht Bills Top<br>% Duty Cyc |                               | 5.0<br>5.0          | μΑ          | V <sub>CC</sub> = Max                               | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| Ін                         | Input High Current<br>(I/O Pins Only)   |                             |                               | Vm 15<br>15         | μΑ          | V <sub>CC</sub> = Max                               | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| I <sub>I</sub> L           | Input Low Current<br>(except I/O Pins)  | .800                        | e eno-se t                    | -5.0<br>-5.0        | μΑ          | V <sub>CC</sub> = Max                               | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND  |
| I <sub>IL</sub>            | Input Low Current<br>(I/O Pins Only)    | es.<br>not teated.          | notistuntes<br>fad besm       |                     | μА          | V <sub>CC</sub> = Max                               | $V_l = 0.5V \text{ (Note 2)}$<br>$V_l = \text{GND}$   |
| VIK                        | Clamp Diode Voltage                     |                             | -0.7                          | -1.2                | V           | $V_{CC} = Min; I_N = -1$                            | 18 mA   |
| los                        | Short Circuit Current                   | -60                         | -120                          |                     | mA          | V <sub>CC</sub> = Max (Note 1);                     | $V_0 = GND$   |
| V <sub>OH</sub>            | Minimum High Level                      | 2.8                         | 3.0                           |                     |             | $V_{CC} = 3V; V_{IN} = 0.2$                         | 2V or $V_{HC}$ ; $I_{OH} = -32 \mu A$   |
|                            | Output Voltage                          | V <sub>HC</sub> 2.4 2.4     | V <sub>CC</sub><br>4.3<br>4.3 | HL)<br>evices)      | TieseV      | $V_{IN} = V_{IH} \text{ or } V_{IL}$                | $I_{OH} = -300 \mu\text{A}$<br>$I_{OH} = -12 \text{mA} (\text{Mil})$<br>$I_{OH} = -15 \text{mA} (\text{Com})$ |
| V <sub>OL</sub> Maximum Lo | Maximum Low Level                       |                             | GND                           | 0.2                 | 123 193 (6) | $V_{CC} = 3V; V_{IN} = 0.2$                         | $2V \text{ or } V_{HC}; I_{OL} = 300 \ \mu\text{A}$   |
|                            | Output Voltage                          |                             | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55 | ٧           | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 300 \mu\text{A}$ $I_{OL} = 48 \text{mA (Mil)}$ $I_{OL} = 64 \text{mA (Com)}$                        |

### DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to  $+125^{\circ}$ C. VHC = VCC -0.2V.

| Symbol                  | Parameter                                    | 54FCT/74FCT |      | СТ   | Units                | Conditions   |   |  |  |
|-------------------------|--|-------------|------|------|----------------------|--|---|--|--|
| and of V                |  | Min Typ Max |      | Max  | VOTOLV               | SAFOTA SHORIDAN -0.1   |   |  |  |
| lcc<br>O'esr+           | Maximum Quiescent<br>Supply Current          | ut Voltage  |      | 1.5  | mA                   | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2V$ $f_I = 0$  |   |  |  |
| Δl <sub>CC</sub>        | Quiescent Supply Current;<br>TTL Inputs HIGH | emperature  | 0.5  | 2.0  | mA                   | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   | Storage Temperature (<br>74FCTA<br>54FCTA       |  |  |
| ICCD                    | Dynamic Power<br>Supply Current (Note 4)     | 0           | ).25 | 0.40 | mA/MHz               | V <sub>CC</sub> = Max<br>Outputs Open<br>T/R̄ = GND or V <sub>CC</sub><br>OE = GND<br>One Input Toggling<br>50% Duty Cycle | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        |  |  |
| lc<br>eulev en<br>0°83- | Total Power Supply<br>Current (Note 6)       | neo test re | 1.5  | 4.5  | 2 viims <sup>2</sup> | V <sub>CC</sub> = Max<br>Outputs Open<br>T/R = OE = GND  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        |  |  |
|                         | Conditions                                   |             | 1.8  | 5.0  | mA                   | f <sub>I</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle  | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND |  |  |
|                         |  |             | 3.0  | 8.0  | XXX                  | Outputs Open   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        |  |  |
|                         |  |             |      |      | 8.0                  | $T/\overline{R} = \overline{OE} = GND$<br>$f_1 = 2.5 \text{ MHz}$  | V <sub>IN</sub> = 3.4V                          |  |  |
| (C ptr                  |  | seM = pav   | 5.0  | 14.5 | 5,0                  | Eight Bits Toggling<br>50% Duty Cycle  | V <sub>IN</sub> = GND                           |  |  |
| VH                      | Input Hysteresis<br>on Clock Only            | aM = 00 V2  | 200  | Aus  | ≅ mV                 |  | H Input High C                                  |  |  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

IC = ICC + ΔICC D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub> (f<sub>CP</sub>/2 + f<sub>I</sub> N<sub>I</sub>)
I<sub>CC</sub> = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V) D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

### AC Electrical Characteristics: See Section 2 for Waveforms

|                                      |   | 54FCTA/74FCTA   | 74FCTA   | 54FCTA  | PER STATE | CAR.        |
|--------------------------------------|---|---|--|---|-----------|-------------|
| Symbol                               | Parameter                                 | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V          | $T_A$ , $V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50 pF$ | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$        | Units     | Fig.<br>No. |
|                                      |   | Тур   | Min (Note 2) Max                                       | Min (Note 2) Max  | Clie      | 100         |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>A to B, B to A       | 3.3   | 1.5 4.6  | an Natara   | ns        | 2-8         |
| t <sub>PZH</sub>                     | Output Enable Time OE to A or B           | AFOT/8.8 TOTAL  | 1.5 6.2  | nas eight edge-riggered t-tyd                                 | A ns      | 2-8         |
| t <sub>PHZ</sub>                     | Output Disable Time OE to A or B          | totolim 804.5 rat rettuc<br>stanta nomino be              | 1.5 - 5.0  | and Master Roset (MR) input le<br>Rops simultaneously.        | ns        | 2-11        |
| t <sub>PZH</sub>                     | Output Enable Time T/R to A or B (Note 1) | em auononomyas ,be<br>imil et 4.8<br>samp dioese et limit | 1.5 6.2  | ily edge-triggered. The state of<br>ins before the LOW-to-HBH | ns        | 2-11        |
| t <sub>PHZ</sub>                     | Output Enable Time T/R to A or B (Note 1) | m \$6 .(r4.5) Am 64                                       | 1.5 5.0  | i i i i i i i i i i i i i i i i i i i                         | ns        | 2-11        |

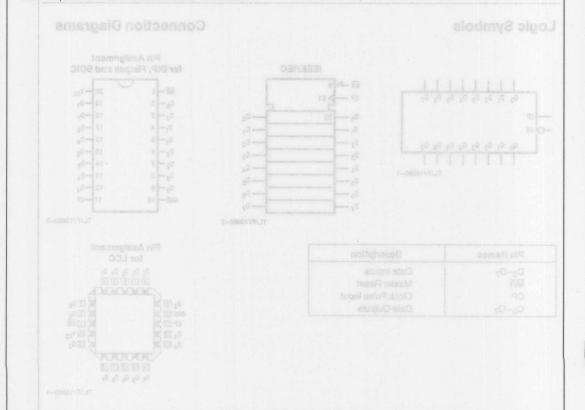
Note 1: This parameter is guaranteed but not tested.

Note 2: Minimum limits guaranteed but not tested on propagation delays.

### Capacitance TA = +25°C, f = 1.0 MHz

| Symbol           | Parameter (Note)   | Тур | Max | Units | Conditions            |
|------------------|--------------------|-----|-----|-------|-----------------------|
| CIN              | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| C <sub>OUT</sub> | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.





### ADVANCE INFORMATION

Symbol

### 54FCT/74FCT273A Octal D Flip-Flop

### **General Description**

The 'FCT273A has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buff-ered Clock (CP) and Master Reset (MR) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{\text{MR}}$  input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

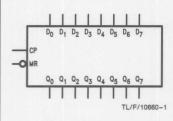
FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

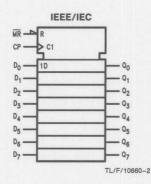
FACT FCTA features NSC correction and split ground bus for superior performance.

### **Features**

- NSC 54FCT/74FCT273A is pin and functionally equivalent to IDT 54FCT/74FCT273A
- Ideal buffer for MOS microprocessor or memory
- Buffered common clock
- Buffered, asynchronous master reset
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

### **Logic Symbols**

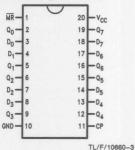


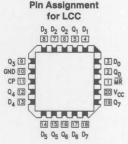


| Pin Names                      | Description       |
|--------------------------------|-------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs       |
| MR                             | Master Reset      |
| CP                             | Clock Pulse Input |
| Q <sub>0</sub> -Q <sub>7</sub> | Data Outputs      |

### **Connection Diagrams**

Pin Assignment for DIP, Flatpak and SOIC





TL/F/10660-4



# 54FCT/74FCT373A Octal Transparent Latch with TRI-STATE® Outputs

### **General Description**

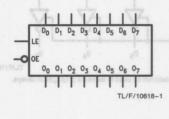
The 'FCT373A consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable  $(\overline{OE})$  is LOW. When  $\overline{OE}$  is HIGH, the bus output is in the high impedance state.

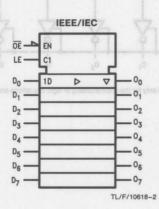
### **Features**

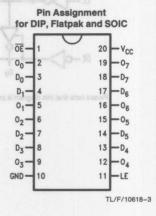
- NSC 54/74FCT373A pin and functionally equivalent to IDT 54/74FCT373A
- Eight latches in a single package
- TRI-STATE outputs for bus interfacing
- TTL input and output level compatible
- High current latch up immunity
- IOI = 48 mA (commercial) and 32 mA (military)
- Military product compliant to MIL-STD 883

Ordering Code: See Section 8
Logic Symbols

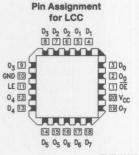
### **Connection Diagrams**







| Pin Names                      | Description             |  |  |
|--------------------------------|-------------------------|--|--|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs             |  |  |
| LE                             | Latch Enable Input      |  |  |
| ŌĒ                             | Output Enable Input     |  |  |
| 00-07                          | TRI-STATE Latch Outputs |  |  |



TL/F/10618-4

### **Functional Description**

The 'FCT373A contains eight D-type latches with TRI-STATE outputs. When the Latch Enable (LE) input is HIGH, data on the  $D_n$  inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE outputs are controlled by the Output Enable  $(\overline{OE})$  input. When  $\overline{OE}$  is LOW, the standard outputs are in the 2-state mode. When  $\overline{OE}$  is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Elight latches in a single package

W TRI-STATE outputs for bus interfacing

### Truth Table

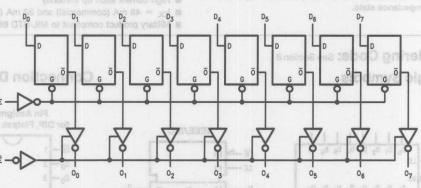
|    | Inputs   | hannalma   | Outputs  |
|----|----------|------------|----------|
| LE | ŌĒ       | Dn         | On       |
| X  | ACHOT    | X          | Z        |
| Н  | Moles.   | Par 26 2 1 | 1 - 1150 |
| H  | s. incre | SECHET     | CHCLGI   |
| L  | L        | X          | 00       |

H = HIGH Voltage Level

X = Immaterial

O<sub>0</sub> = Previous O<sub>0</sub> before HIGH to Low transition of Latch Enable

# Logic Diagram co level tuctuo bas tuqal JTT 18



TL/F/10618-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Pin Assignme
Description

Dala inputs
Laten Enable Input

Output Enable Input

TRI-STATE Laten Outputs

Output State Country

Output

| Terminal Voltage with Re   |  | 1701                          | 74FCTA  | 4.75                            | / to 5.25V  |
|--|--|-------------------------------|---|---------------------------------|---|
| 54FCTA<br>74FCTA   | -0.5V to   | 0 + 7.0V<br>0 + 7.0V          | Input Voltage   |                                 | OV to V <sub>CC</sub>   |
| Temperature under Bias ( 74FCTA 54FCTA Storage Temperature (T <sub>S</sub> 74FCTA 54FCTA | (T <sub>BIAS</sub> ) -55°C to  | + 125°C<br>+ 135°C<br>+ 125°C | Output Voltage Operating Temperature 54FCTA 74FCTA Junction Temperature ( CDIP PDIP | (T <sub>A</sub> ) -55°C to -0°C | 0V to V <sub>CC</sub><br>0 + 125°C<br>to + 70°C<br>175°C<br>140°C |
| to the device may occur. The dat   | ngs are those values beyond which<br>tabook specifications should be meter design is reliable over its pov | et, without                   | 1.5 4.5   |                                 | ol  |

temperature, and output/input loading variables. National does not recommend operation of FACT FCTA circuits outside databook specifications.

DC Characteristics for 'FCTA Family Devices

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type; Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to  $\pm70$ °C; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55$ °C to  $\pm125$ °C,  $V_{HC}=V_{CC}=0.2V$ 

| Symbol           | Parameter                                    | 54FCTA/74FCTA           |                               |                                | Units                   | Conditions   |  |  |
|------------------|--|-------------------------|-------------------------------|--------------------------------|-------------------------|--|--|--|
| Cymbol .         | $VAx = V_{BV} = 3.4V$                        | Min Typ Max             |                               |                                | Conditions              |  |  |  |
| V <sub>IH</sub>  | Minimum High Level                           | 2.0                     |                               | 8                              | V 14                    | .8   |  |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           |                         | Vn                            | 0.8                            | v °                     | INC.   | V <sub>H</sub> Input Hyst<br>on Clock (  |  |
| I <sub>IH</sub>  | Input High Current                           | ,one pane,              | angina at                     | 5.0<br>5.0                     | μΑ                      |  | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$  |  |
| I <sub>IL</sub>  | Input Low Current                            |                         | Jupply calcu<br>gueranteed    |                                | μΑ                      | V <sub>CC</sub> = Max (datas) vice lb conditions are examples of the lbc till  |  |  |
| l <sub>OZ</sub>  | Maximum TRI-STATE Current                    |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μ <b>Α</b><br>(VA.0 — M | Arrent  Aurent for a TTL High Input (V   | $V_{l} = V_{CC}$<br>$V_{l} = 2.7V \text{ (Note 2)}$<br>$V_{l} = 0.5V \text{ (Note 2)}$<br>$V_{l} = \text{GND}$ |  |
| V <sub>IK</sub>  | Clamp Diode Voltage                          |                         | -0.7                          | -1.2                           | V                       | V <sub>CC</sub> = Min; I <sub>N</sub> = -18 mA   |  |  |
| los              | Short Circuit Current                        | -60                     | -120                          | or crucy<br>ar Davions)        | mA                      | V <sub>CC</sub> = Max (Note 1); V <sub>O</sub> =   | GND  |  |
| VoH              | Minimum High Level                           | 2.8                     | 3.0                           |                                |                         | $V_{CC} = 3V; V_{IN} = 0.2V \text{ or } V_{IN} $ | $I_{HC}$ ; $I_{OH} = -32 \mu\text{A}$  |  |
|                  | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | .she <b>V</b> gon       | $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OH} = -300 \mu\text{A}$<br>$I_{OH} = -12 \text{mA} (\text{Mil})$<br>$I_{OH} = -15 \text{mA} (\text{Com})$  |  |
| VOL              | Maximum Low Level                            |                         | GND                           | 0.2                            |                         | $V_{CC} = 3V; V_{IN} = 0.2V \text{ or } V_{IN} $ | $I_{HC}$ ; $I_{OL} = 300  \mu A$   |  |
|                  | Output Voltage                               |                         | GND<br>0.3<br>0.3             | 0.2<br>0.50<br>0.50            | ٧                       | $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OL} = 300 \mu A$<br>$I_{OL} = 32 \text{ mA (Mil)}$<br>$I_{OL} = 48 \text{ mA (Com)}$                       |  |
| Icc              | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                            | mA                      | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V \\ &f_{I} = 0 \end{aligned}$   |  |  |
| Δl <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                            | mA                      | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   |  |  |

DC Characteristics for 'FCTA Family Devices (Continued) Typical values are at  $V_{CC}=5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_{A}=0^{\circ}C$  to  $\pm70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_{A}=-55^{\circ}C$  to  $\pm125^{\circ}C$ ,  $V_{HC}=V_{CC}-0.2V$ 

| Symbol Parameter   |   | 54FCT  | 54FCTA/74FCTA  |  |  | (MRHY) CIND of Property distributions                           |  |   |   |
|--|---|--|--|--|--|---|--|---|---|
|  |   | Min  | Min Typ Max  |  | nits   | IVE.0— Conditions AT  |  |   | 54FC  |
| 175°C  | Dynamic Power<br>Supply Current (Note   |  | 0.25   | ).45 mA  | O'8S) +<br>O'8S) +<br>O'MHz  |   | Open<br>ND   | Temperature (1  |   |
| Total Power Supply<br>Current (Note 6)   |   |  | 1.5  |  | V.B.V.<br>Am OST<br>denset<br>des without<br>were supply,<br>det recom-  | V <sub>CC</sub> = I<br>Outputs<br>OE = G<br>LE = V <sub>0</sub> | Open<br>iND<br>cc  | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V   | Power DC Out Work to the de exception (exception) |
|  |   |  |  | 5.0  | mA   | ma - de lasta -m-   | MHz<br>Toggling<br>ity Cycle   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND   |   |
| fibre shown as Max, use the value if $V_{\rm CG} = 5.0 \rm V \pm 10\%$ , $T_{\rm A} = -58^{\circ} \rm C$           |   |  | 3.0  | 8.0  | аль саты<br>V0,6 = (   | (Note 5)  V <sub>CC</sub> = Max  OE = GND                       |  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$  |   |
|  | Conditions  |  |  | Make   | TAITAP   | $LE = V_0$<br>$f_1 = 2.5$                                       | 101015   | V <sub>IN</sub> = 3.4V  | ladengl   |
|  |   |  | 5.0  | 14.5   | 3.5  | The second second   | ts Toggling  | V <sub>IN</sub> = GND   | HI)   |
| VH   | Input Hysteresis  | CONTRACTOR OF THE PARTY OF THE  |  |  |  |   |  |   |   |
|  | on Clock Only   |  | 200  | 8.0  | mV   |   | Level  | Maximum Low<br>Input Voltage  | 11  |
| Note 1: Ma:<br>Note 2: This  |   | ceed one second,<br>not tested.  | not more th  | an one output  |  | one time.   |  | Input Voltage<br>Input High Cur   |   |
| Note 1: Max<br>Note 2: This<br>Note 3: Per<br>Note 4: This<br>Note 5: Val  | on Clock Only  ximum test duration not to ex s parameter guaranteed but n  TTL driven input (V <sub>IN</sub> = 3.4) s parameter is not directly tes ues for these conditions are e  | ceed one second,<br>not tested.<br>V); all other inputs<br>stable, but is derive<br>examples of the IC   | not more th<br>at V <sub>CC</sub> or G<br>d for use in   | an one output iND. Total Power \$  | t shorted at   | eulations.  | fner   | Innut Voltage   | Н   |
| Note 1: Max<br>Note 2: This<br>Note 3: Per<br>Note 4: This<br>Note 5: Val<br>Note 6: IC =<br>IC =<br>ICC           | on Clock Only  ximum test duration not to ex s parameter guaranteed but n  TTL driven input (V <sub>IN</sub> = 3.4) s parameter is not directly tes   | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the I <sub>Cl</sub> DYNAMIC  (f <sub>CP</sub> /2 + f <sub>I</sub> N <sub>I</sub> )  or a TTL High Input   | not more that V <sub>CC</sub> or G   | an one output  | t shorted at   | eulations.  | fner   | Input Vollage<br>Input High Cur<br>Input Low Cun  | Н   |
| Note 1: Ma: Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: IC = ICC AIC DH NT                           | on Clock Only  ximum test duration not to ex s parameter guaranteed but in  TTL driven input (V <sub>IN</sub> = 3.4) s parameter is not directly tes ues for these conditions are e    QUIESCENT + INPUTS + I   CC + AICC D <sub>I</sub> N <sub>T</sub> + ICCD =   Quiescent Current   C = Power Supply Current fo   Duty Cycle for TTL Inputs   Number of Inputs at D <sub>I</sub>   | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the I <sub>Ct</sub> IDYNAMIC (f <sub>CP</sub> /2 + f <sub>1</sub> N <sub>1</sub> )  or a TTL High Input  High   | not more that V <sub>CC</sub> or G d for use in the formula. T   | in one output  | t shorted at   | eulations.  | tnen the sted.   | Input Vollage<br>Input High Cur<br>Input Low Cun  | 20<br>Hi  |
| Note 1: Ma: Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic = Ic = Icc Alc DH NT                      | on Clock Only  ximum test duration not to exist a parameter guaranteed but in TTL driven input (V <sub>IN</sub> = 3.4) is parameter is not directly test uses for these conditions are elected to the second the second to the                                | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the local distribution of the local d | not more that V <sub>CC</sub> or G d for use in g formula. T $(V_{IN} = 3.4)$  | ian one output iND. Total Power s hese limits are  | shorted at   | eulations.  | iner  sted.  There  STATE  egatlo\   | Input Vollege<br>Input Low Cun<br>Input Low Cun<br>Maximum TRI  | IL OZ OZ  |
| Note 1: Ma: Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic = Icc = Alc DH NT Icct fcp Au fi =        | on Clock Only  ximum test duration not to exist a parameter guaranteed but in TTL driven input (V <sub>IN</sub> = 3.4) is parameter is not directly test uses for these conditions are earliestern to the second                                | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the I <sub>Cl</sub> DYNAMIC (f <sub>CP</sub> /2 + f <sub>1</sub> N <sub>1</sub> )  or a TTL High Input High  d by an Input Trans  ster Devices (Zero  | not more that $V_{CC}$ or $G$ of $G$ of $G$ of $G$ or $G$ of $G$ or $G$  | ian one output iND. Total Power s hese limits are  | shorted at   | culations.<br>ed but not te                                     | tnent tnent to the part to the | Input Vollege Input High Cur Input Low Cun Maximum TRI Clamp Diode V  | IH OZ OZ /IK                                      |
| Note 1: Ma: Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic : Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic = | on Clock Only  ximum test duration not to exist a parameter guaranteed but in TTL driven input (V <sub>IN</sub> = 3.4) is parameter is not directly test uses for these conditions are elected to the second tions are elected to the second tions are the second to the second tions and the second tions are the second tions ar                                | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the I <sub>Cl</sub> DYNAMIC  (f <sub>CP</sub> /2 + f <sub>1</sub> N <sub>1</sub> )  or a TTL High Input  High  d by an Input Trans  ster Devices (Zero  | not more that $V_{CC}$ or $G$ of $G$ of $G$ of $G$ or $G$ of $G$ of $G$ or $G$ of $G$ or $G$ of $G$ or $G$ of $G$ or $G$ of $G$ or $G$ of $G$ or $G$ of $G$ or $G$  | inn one output inno. Total Power's hese limits are   | supply calc  | bulations.  d but not te  | sted. STATE Carrent Voltage  | Input Voltage Input Fligh Cur Input Low Cur Maximum TRI Cramp Diode V   | IH OZ OZ /IK                                      |
| Note 1: Ma: Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I     | on Clock Only  ximum test duration not to exist parameter guaranteed but in TTL driven input (V <sub>IN</sub> = 3.4) is parameter is not directly test uses for these conditions are elected for the second times and the second times are the second times and the second times are the second times and the second times are the second times and the second times are the second times and the second times are the second times are the second times are the second times and the second times are the second time                                | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the I <sub>Cl</sub> DYNAMIC  (f <sub>CP</sub> /2 + f <sub>I</sub> N <sub>I</sub> )  or a TTL High Input High  d by an Input Trans  ster Devices (Zero   | not more that $V_{CC}$ or $G$ of $G$ of $G$ of $G$ or use in $G$ formula. The $G$ of $G$ of $G$ of $G$ of $G$ or $G$ of $G$ of $G$ of $G$ or   | inn one output inno.  Total Power s hese limits are  V)  July or LHL) July or LHL July or LH July or LH July or LH | Supply calce a guarantee   | bulations.  ad but not te                                       | sted. STATE Gurrant Acitage Jurent Lavel   | Input Vollege Input High Cur Input Low Cun Maximum TRI Clamp Diode N Short Circuit C Output Voltage             | IH OZ OZ /IK                                      |
| Note 1: Ma: Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic Ic I     | on Clock Only  ximum test duration not to exist parameter guaranteed but in TTL driven input (V <sub>IN</sub> = 3.4) is parameter is not directly test uses for these conditions are elected for these conditions are elected for the conditions are elected for t                                | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the I <sub>Cl</sub> IDYNAMIC  (f <sub>CP</sub> /2 + f <sub>1</sub> N <sub>1</sub> )  or a TTL High Input High  Id by an Input Trans ster Devices (Zero  | not more that V <sub>CC</sub> or G d for use in formula. T (V <sub>IN</sub> = 3.4 (V <sub>IN</sub> = 1.4 (V <sub>IN</sub> = | inn one output inno. Total Power's hese limits are   | Supply calcolors and a supply calcolors are guaranteed at the supply calcolors and supply calcolors are guaranteed at the supply calcol | bulations.  d but not te  | sted. STATE Gurrant Authorities Lavel  | Input Vollage Input High Cur Input Low Cun Maximum TRI Clamp Diode V Short Circuit C Output Voltage Maximum Low | III. OZ OZ AIK                                    |
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| Note 1: Max Note 2: This Note 3: Per Note 4: This Note 5: Val Note 6: Ic = Ic = Ic = Ic = Ic = Ic = Ic = Ic =      | on Clock Only  ximum test duration not to ex s parameter guaranteed but n  TTL driven input (V <sub>IN</sub> = 3.4) s parameter is not directly tes ues for these conditions are e louiscent + linputs + l cc + Alcc D <sub>H</sub> N <sub>T</sub> + lccD  Quiescent Current C = Power Supply Current fo Duty Cycle for TTL Inputs Number of Inputs at D <sub>H</sub> D = Dynamic Current Caused C = Clock Frequency for Regist Input Frequency Number of Inputs at fi currents are in milliamps and incurrents are in milliamps and in the second of | ceed one second, not tested.  V); all other inputs stable, but is derive examples of the local distribution of the local d | at V <sub>CC</sub> or G d for use in formula. T (V <sub>IN</sub> = 3.4   | inn one output inno. Total Power s hese limits and V)  ILH or LHL) gister Devices  | Supply calco   | bulations.  d but not te  | sted. STATE Gurrant fourth turners for the seal fourth the sea | Input Vollage Input High Cur Input Low Cun Maximum TRI Clamp Diode V Short Circuit C Output Voltage Maximum Low | /ц. пт. пт. пт. пт. пт. пт. пт. пт. пт. пт        |

### AC Electrical Characteristics: See Section 2 for Waveforms

|                  |   | 54FCTA/74FCTA                                    | 74FCT/  | 4   | 54FCTA   | ne2 i   | Fig. |
|------------------|---|--|---|-----|--|---------|------|
| Symbol           | Parameter   | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | T <sub>A</sub> , V <sub>CC</sub> = R <sub>L</sub> = 500 C <sub>L</sub> = 50 | ΩΩ  | $T_A$ , $V_{CC} = MII$ $R_L = 500\Omega$ $C_L = 50 pF$ | Units   |      |
|                  |   | Тур 💮  | Min (Note 1)  | Max | Min (Note 1) Max                                       | Ols     | 100  |
| t <sub>PLH</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 4.0  | 1.5   | 5.2 | noitoiroan   | ns      | 2-8  |
| t <sub>PZL</sub> | Output Enable Time                                    | 5.5 AAT 5.5                                      | 1.5 -qill eq<br>il ot 1.5 to li   | 6.5 | a high-speed, low-power oarate D-type inputs for e     | ns      | 2-11 |
| t <sub>PHZ</sub> | Output Disable Time                                   | A STATE CO. LINE TO DE                           | itud is -itud i<br>isti s1.5 ils ota  |     | outs for bus-oriented appliand Ordput Enable (OE) ar   | ATE OUT | 2-11 |
| t <sub>PLH</sub> | Propagation Delay<br>LE to On                         | 20M0 17.0 a stugni                               | 2.0   | 8.5 |  | ns      | 2-8  |
| tsu              | Set Up Time High or Low<br>D <sub>n</sub> to LE       | = 48 m. 1.0 mercis                               | 2.0   |     |  | ns      | 2-10 |
| tн               | Hold Time High or Low Dn to LE                        | neith reliaber vilner<br>1.0                     | 1.5   |     |  | ns      | 2-10 |
| t <sub>w</sub>   | LE Pulse Width<br>High or Low                         | 4.0  | 5.0   |     | Code: Sea Section 6                                    | ns      | 2-9  |

### Capacitance TA = +25°C, f = 1.0 MHz

| Symbol | Parameter (Note 1) | Тур | Max | Units      | Conditions            |
|--------|--------------------|-----|-----|------------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | 10 < pF 90 | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12  | pF         | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

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30 [1] DV III I

### 54FCT/74FCT374A Octal D Flip-Flop with TRI-STATE® Outputs

### **General Description**

The 'FCT374A is a high-speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops.

### **Features**

- NSC 54/74FCT374A is pin and functionally equivalent to IDT 54/74FCT374A
- Buffered positive edge triggered clock
- TRI-STATE outputs for bus-oriented applications
- TTL input and output level compatible
- TTL inputs accept CMOS levels
  - High current latch up immunity
  - I<sub>OL</sub> = 48 mA (commercial) and 32 mA (military)
  - Electrostatic discharge protection ≥ 2 kV
  - Inherently radiation tolerant

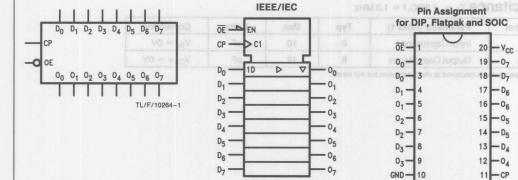
TL/F/10264-2

Ordering Code: See Section 8

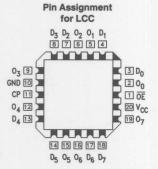
### **Logic Symbols**

### **Connection Diagrams**

loolmy8



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| CP                             | Clock Pulse Input             |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Outputs             |



TL/F/10264-4

-CP

TL/F/10264-3

### **Functional Description**

The 'FCT374A consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{\text{OE}}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{\text{OE}}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{\text{OE}}$  input does not affect the state of the flip-flops.

### Truth Table 154 mumixeM etuloed A

| pertuper en | Inputs |           |                    |  |  |  |
|-------------|--------|-----------|--------------------|--|--|--|
| Dn          | CP     | ŌĒ        | ofuditi On \ealito |  |  |  |
| Н           | _      | L         | Termina Holtage    |  |  |  |
| Luca Luca n | _      | NEBLA GNE | or roads of min    |  |  |  |
| X           | X      | Н         | Z                  |  |  |  |

H = HIGH Voltage Level

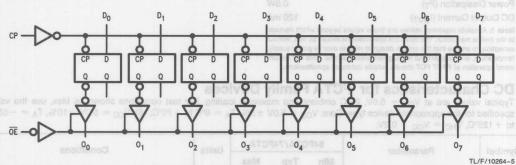
L = LOW Voltage Level

X = Immaterial

Z = High Impedance

✓ = LOW-to-HIGH Transition

### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

# V<sub>II</sub> Maximum Law Level Input Voltage 0.8 V Igh Input High Current 5.0 μA V<sub>GC</sub> = Max V<sub>II</sub> = V<sub>GC</sub> Igh Input Low Current -5.0 μA V<sub>GC</sub> = Max V<sub>II</sub> = GND Igh Maximum TRI-STATE Current 10.0 μA V<sub>GC</sub> = Max V<sub>G</sub> = V<sub>G</sub> V<sub>G</sub> V<sub>II</sub> Clamp Diode Veltage -0.7 -1.2 V V<sub>GC</sub> = Min; I<sub>M</sub> = -18 mA V<sub>II</sub> Clamp Diode Veltage -0.7 -1.2 V V<sub>GC</sub> = Min; I<sub>M</sub> = -18 mA V<sub>II</sub> Clamp Diode Veltage -0.7 -1.2 V V<sub>GC</sub> = Min; I<sub>M</sub> = -18 mA V<sub>I</sub> Clamp Diode Veltage -0.7 -1.2 V V<sub>GC</sub> = Min; I<sub>M</sub> = -18 mA V<sub>I</sub> Clamp Circuit Current -6.0 -1.2 V V<sub>GC</sub> = Min; I<sub>M</sub> = -18 mA V<sub>I</sub> Clump Circuit Current -2.8 3.0 V<sub>GC</sub> = Min; I<sub>M</sub> = -10 mA V<sub>I</sub> Clump Veltage V<sub>I</sub> V<sub>G</sub> = Min; I<sub>M</sub> = -12 mA I<sub>M</sub>= -12 mA V<sub>I</sub> V<sub>I</sub> V<sub>I</sub> V<sub>I</sub> <t

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Terminal Voltage with Respect to GND (V <sub>TERM</sub> ) 54FCTA 74FCTA | -0.5V to 7.0V<br>-0.5V to 7.0V     |
|---|------------------------------------|
| Temperature under Bias (T <sub>BIAS</sub> )<br>74FCTA<br>54FCTA         | -55°C to +125°C<br>-65°C to +135°C |
| Storage Temperature (T <sub>STG</sub> )<br>74FCTA<br>54FCTA             | -55°C to +125°C<br>-65°C to +150°C |
| Power Dissipation (P <sub>T</sub> )                                     | 0.5W                               |
| DC Output Current (IOLIT)   | 120 mA                             |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

# Recommended Operating

| Supply Voltage (V <sub>CC</sub> )       |                       |
|---|-----------------------|
| 54FCTA SIN BIOMET MIGHLO IN             |                       |
| 74FCTA and over liw agoli               | 4.75V to 5.25V        |
| Input Voltage                           | 0V to V <sub>CC</sub> |
| Output Voltage                          | 0V to V <sub>CC</sub> |
| Operating Temperature (T <sub>A</sub> ) |                       |
| 54FCTA                                  | -55°C to +125°C       |
| 74FCTA off-quit ent to etata er         |                       |
| Junction Temperature (T,I)              |                       |
| CDIP                                    | 175°C                 |
| PDIP                                    | 140°C                 |
|   |                       |

### DC Characteristics for 'FCTA Family Devices

Typical values are at  $V_{CC}=5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC}=V_{CC}-0.2V$ .

| Symbol           | Parameter                                    | 54F                     | CTA/74                        | FCTA                           | Units | Conditions  |  |  |
|------------------|--|-------------------------|-------------------------------|--------------------------------|-------|---|--|--|
| R-PRINCIPA       |  | Min                     | Тур                           | Max                            |       |   |  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                     | as enclusies                  | ne digol to gr                 | V     | tram is provided only for the   | Please note that tile dia  |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           |                         |                               | 0.8                            | ٧     |   |  |  |
| lін              | Input High Current                           |                         |                               | 5.0<br>5.0                     | μΑ    | V <sub>CC</sub> = Max   | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$  |  |
| I <sub>IL</sub>  | Input Low Current                            |                         |                               | -5.0<br>-5.0                   | μΑ    | V <sub>CC</sub> = Max   | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$  |  |
| loz              | Maximum TRI-STATE Current                    |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ    | V <sub>CC</sub> = Max   | $\begin{aligned} &V_{O} = V_{CC} \\ &V_{O} = 2.7V \text{ (Note 2)} \\ &V_{O} = 0.5V \text{ (Note 2)} \\ &V_{O} = \text{GND} \end{aligned}$ |  |
| VIK              | Clamp Diode Voltage                          |                         | -0.7                          | -1.2                           | ٧     | $V_{CC} = Min; I_N = -18 \text{ mA}$  |  |  |
| los              | Short Circuit Current                        | -60                     | -120                          |                                | mA    | V <sub>CC</sub> = Max (Note 1);   | $V_O = GND$  |  |
| V <sub>OH</sub>  | Minimum High Level                           | 2.8                     | 3.0                           |                                |       | $V_{CC} = 3V; V_{IN} = 0.2$   | V or $V_{HC}$ ; $I_{OH} = -32 \mu\text{A}$   |  |
|                  | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧     | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OH} = -300 \mu A$<br>$I_{OH} = -12 \text{ mA (Mil)}$<br>$I_{OH} = -15 \text{ mA (Con)}$  |  |
| V <sub>OL</sub>  | Maximum Low Level                            |                         | GND                           | 0.2                            |       | $V_{CC} = 3V; V_{IN} = 0.2$   | V or $V_{HC}$ ; $I_{OL} = 300 \mu A$   |  |
|                  | Output Voltage                               |                         | GND<br>0.3<br>0.3             | 0.2<br>0.50<br>0.50            | ٧     | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OL} = 300 \ \mu A$<br>$I_{OL} = 32 \ mA \ (Mil)$<br>$I_{OL} = 48 \ mA \ (Com)$   |  |
| loc              | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                            | mA    | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2 \\ &f_I = 0 \end{aligned}$ | V  |  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                            | mA    | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)  |  |  |

### DC Characteristics for 'FCTA Family Devices (Continued)

Typical values are at  $V_{CC}=5.0V$ ,  $25^{\circ}C$  ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_{A}=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_{A}=-55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{HC}=V_{CC}-0.2V$ .

| Symbol         | Parameter                                | 54FCTA/74FCTA |      | Units | d = goV Cone | Conditions  |  |            |
|----------------|--|---------------|------|-------|--------------|---|--|------------|
| Symbol         |  | Min           | Тур  | Max   | relia        | avī.  | antionio                                 |            |
| ICCD<br>8-S    | Dynamic Power<br>Supply Current (Note 4) |               | 0.15 | 0.25  | mA/MHz       | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND                       | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$ |            |
|                | n  |               |      | 1.5   |              | One Input Toggling 50% Duty Cycle                                       | Output Enable                            |            |
| Ic S           | Total Power Supply<br>Current (Note 6)   |               | 8,8  | 1.5   |              | V <sub>CC</sub> = Max Outputs Open                                      | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$ | PHZ<br>PL2 |
|                | Odirent (Note 0)                         |               | 1.5  | 4.0   |              | f <sub>CP</sub> = 10 MHz  | Set Up Time It                           |            |
|                | 0  |               | 2.0  | 6.0   |              | f <sub>I</sub> = 5.0 MHz<br>One Bit Toggling                            | $V_{IN} = 3.4V$ $V_{IN} = GND$           | H          |
|                |  |               |      | 6.0   | mA           | 50% Duty Cycle  | Cp Rutsa Wildth                          | W          |
|                |  |               | 3.75 | 7.8   |              | (Note 5)  V <sub>CC</sub> = Max  Outputs Open  f <sub>CP</sub> = 10 MHz | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$ | Note to Mi |
|                | notifien                                 | 3             |      | 1 10  |              | OE = GND<br>f <sub>I</sub> = 2.5 MHz                                    |  |            |
|                | V0 = N                                   | V             | 6.0  | 16.8  |              | Eight Bits Toggling   | $V_{IN} = 3.4V$<br>$V_{IN} = GND$        |            |
|                | V0 = 700                                 | y I           | 70   | 1 3   |              | 50% Duty Cycle  |  | Cou        |
| V <sub>H</sub> | Input Hysteresis on Clock Only           |               | 200  |       | mV           | liei han fud molleshetoaninto ta bor                                    | paremeter la measur                      | Note: This |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (VIN = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

|                                      | Conditions   | v <sub>CC</sub> = 5.0v            | sileU  | CL =       | 50 pF | C <sub>L</sub> = 50 pF               | h     | NO.  |
|--------------------------------------|--|-----------------------------------|--------|------------|-------|--------------------------------------|-------|------|
|                                      |  | Тур                               | Mi     | n (Note 1) | Max   | Min (Note 1) Max                     |       |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay  | 00 alug 4.5                       | HMI Am | 2.0        | 6.5   | namic Power<br>coly Current (Note 4) | 7     | 2-8  |
| t <sub>PZH</sub>                     | Output Enable Time                                       | T tugni e5.5                      |        | 1.5        | 6.5   |                                      | ns    | 2-11 |
| t <sub>PHZ</sub>                     | Output Disable Time                                      | xsM = 4.0                         |        | 1.5        | 5.5   | al Power Supply                      | oT ns | 2-11 |
| tsu                                  | Set Up Time High or Low D <sub>n</sub> to C <sub>P</sub> | MOT = 1.0<br>QMD = 30             |        | 2.0        | 1.5   | (0.000)7.10                          | ns    | 2-10 |
| t <sub>H</sub>                       | Hold Time High or Low D <sub>n</sub> to C <sub>P</sub>   | 1-1M 0.3 = 1<br>0.5<br>0.5 BR Tog |        | 1.5        | 0.8   |                                      | ns    | 2-10 |
| t <sub>w</sub>                       | C <sub>P</sub> Pulse Width<br>High or Low                | 0.4 Diay 0                        | Am     | 5.0        |       |                                      | ns    | 2-9  |

Input Hysteresis

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

# Capacitance T<sub>A</sub> = +25°C, f = 1.0 MHz

| Symbol  | Parameter (Note)   | Тур    | Max     | Unit | Condition             |
|---------|--------------------|--------|---------|------|-----------------------|
| CIN QUE | Input Capacitance  | Heid 6 | 10 8.81 | pF   | $V_{IN} = 0V$         |
| Cout    | Output Capacitance | 8      | 12      | pF   | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

### UTI UIUIIA/ITI UIUIIA

### Octal D Flip-Flop with Clock Enable and Williams 118-8

### **General Description**

The FCT377A has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (CE) is LOW.

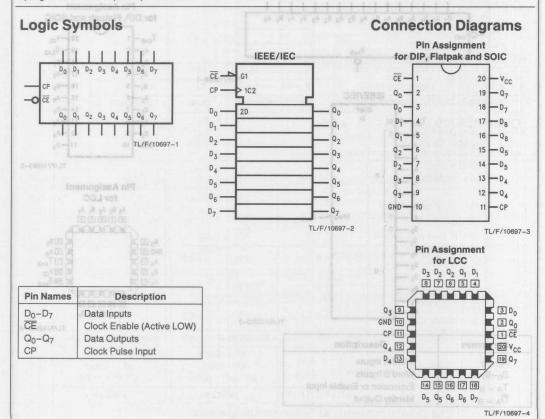
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The  $\overline{\text{CE}}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot corrector in addition to a split ground bus for superior performance.

### **Features**

- NSC 54FCT/74FCT377A is pin and functionally equivalent to IDT 54FCT/74FCT377A
- Ideal for addressable register applications
- Clock enables for address and data synchronization applications
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (com), 32 mA (mil)
- CMOS power levels
- ESD immunity ≥ 4 kV.
- Military product compliant to MIL-STD 883





### **ADVANCE INFORMATION**

# 54FCT/74FCT521A 8-Bit Identity Comparator and page 19 and

### **General Description**

The 'FCT521A is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. The expansion input  $\overline{I}_{A} = {}_{B}$  also serves as an active LOW enable input.

FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

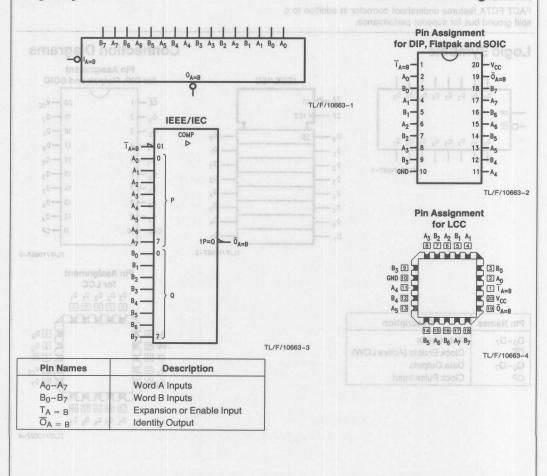
FACT FCTA features undershoot correction and split ground bus for superior performance.

### **Features**

- NSC 54FCT/74FCT521A is pin and functionally equivalent to IDT 54FCT/74FCT521A
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels 3. and a gold and guite and high
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

### **Logic Symbols**

### **Connection Diagrams**





# 54FCT/74FCT533A Octal Transparent Latch with TRI-STATE® Outputs

### **General Description**

The 'FCT533A consists of eight latches with TRI-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the bus output is in the high impedance state. The 'FCT533A is the same as the 'FCT373A, except that the outputs are inverted.

FACT FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

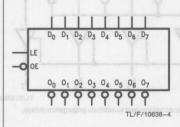
### **Features**

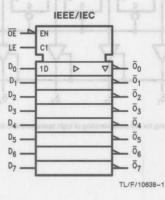
- NSC 54FCT/74FCT533A is pin and functionally equivalent to IDT 54FCT/74FCT533A
- TRI-STATE outputs for bus interfacing
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible STATS
- IOI = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD 883
- Inherently radiation tolerant

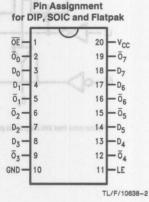
Ordering Code: See Section 8

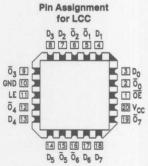
**Logic Symbols** 

Connection Diagrams









TL/F/10638-3

| Pin Names  | Description   |
|--|---|
| $\begin{array}{c} D_0 - D_7 \\ LE \\ \overline{OE} \\ \overline{O}_0 - \overline{O}_7 \end{array}$ | Data Inputs Latch Enable Input (Active HIGH) Output Enable Input (Active LOW) Complementary TRI-STATE Outputs |

### **Function Table**

|       | Inputs   |       |                  |  |  |  |  |
|-------|----------|-------|------------------|--|--|--|--|
| LE    | ŌĒ       | D     | ō                |  |  |  |  |
| Н     | Low      | Н     | 100 S. O. S. S   |  |  |  |  |
| Н     | 1000     | JCL W | H                |  |  |  |  |
| chair | o I Live | X     | $\overline{O}_0$ |  |  |  |  |
| X     | Н        | X     | Z                |  |  |  |  |

H = HIGH Voltage Level L = LOW Voltage Level

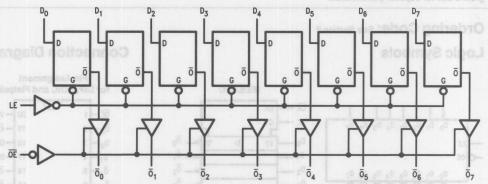
X = Logic(0) or logic(1) must be valid Input Level

### Functional Description

The 'FCT533A contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent and the latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on

the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (OE) input. When OE is LOW the latch contents are presented inverted at the outupts  $\overline{O}_7 - \overline{O}_0$ . When OE is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches. Smarryb one paidotive fuglue tolup bavorqmi

### **Logic Diagram**



TL/F/10638-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Office/ Distributors for availab  | mity and specimounons.  |
|---|---|
| Temperature Voltage with respe-<br>54FCTA<br>74FCTA                       | ect to GND (V <sub>TERM</sub> )<br>-0.5V to +7.0V<br>-0.5V to +7.0V |
| Temperature under Bias (T <sub>BIAS</sub> )<br>74FCTA<br>54FCTA           | 0 x 5 x 5 x 5 x 5 x 5 x 5 x 5 x 5 x 5 x                             |
| Storage Temperature (T <sub>STG</sub> )<br>74FCTA<br>54FCTA               | -55°C to +125°C<br>-65°C to +135°C                                  |
| Power Dissipation (P <sub>T</sub> ) DC Output Current (I <sub>OUT</sub> ) | 0.5W  |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT FCT circuits outside databook specifications.

### Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> )<br>54FCTA | 4.5V to 5.5V  |
|---|---|
| 74FCTA                                      | 4.75V to 5.25V  |
| Input Voltage                               | 0V to V <sub>CC</sub>                                 |
| Output Voltage                              | InecceluD mumixely OV to Vcc                          |
| Operating Temperature<br>54FCTA<br>74FCTA   | -55°C to +125°C<br>0°C to +70°C                       |
| Junction Temperature<br>CDIP<br>PDIP        | (T <sub>J</sub> ) HOH studed JTT 175°C<br>140°C 140°C |
|   |   |

DC Characteristics for FCTA Family Devices
Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0$ °C to +70°C; Mil:  $V_{CC} = 5.0V \pm 10\%$   $T_A = -55$ °C

|                 | China - Nia                         | 54FCTA/74                       | FCTA                           | 8 5,0  |  |  |
|-----------------|-------------------------------------|---------------------------------|--------------------------------|--|--|--|
| Symbol          | Parameter                           | Min Typ                         | Max                            | Max V  0.8 V  5.0 μA V <sub>CC</sub> = Max V <sub>I</sub> = V <sub>CC</sub> V <sub>I</sub> = 2.7V (Note 2 V <sub>I</sub> = GND  0.0 μA V <sub>CC</sub> = Max V <sub>I</sub> = 0.5V (Note 2 V <sub>I</sub> = GND  0.0 0.0 μA V <sub>CC</sub> = Max V <sub>I</sub> = GND  10.0 μA V <sub>CC</sub> = Max V <sub>I</sub> = 0.5V (Note 2 V <sub>I</sub> = GND  10.0 μA V <sub>I</sub> = GND  10.0 μA V <sub>I</sub> = GND | onditions  |  |
| V <sub>IH</sub> | Minimum HIGH Level<br>Input Voltage | 2.0                             | Action 1                       | V  | 9  |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     | Outputs Ope                     | 0.8                            | ٧  |  |  |
| IIH             | Input High Current                  | f) = 2.6 MHz                    | 5.0<br>5.0                     | μА   | V <sub>CC</sub> = Max  | $V_I = V_{CC}$ $V_I = 2.7V \text{ (Note 2)}$           |
| l <sub>IL</sub> | Input Low Current                   | CO 96 Duty C)                   | -5.0<br>-5.0                   | μА   | V <sub>CC</sub> = Max  | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND |
| loz             | Maximum TRI-STATE<br>Current        | d one bms.                      | 10.0<br>10.0<br>-10.0<br>-10.0 | GND  | ion not beat al.  2.4V); all other inputs at V <sub>GC</sub> c | V <sub>O</sub> = 2.7V (Note 2)                         |
| VIK             | Clamp Diode Voltage                 | -0.7                            | -1.2                           | V  | $V_{CC} = Min; I_{IN} = -18$                                   | MA Consultation for these consultations                |
| los             | Short Circuit Current               | -60 -120                        |                                | mA   | V <sub>CC</sub> = Max (Note 1); V                              | O = GND  |
| V <sub>OH</sub> | Minimum High Level                  | 2.8 3.0                         |                                |  | $V_{CC} = 3V; V_{IN} = 0.2V$                                   | or $V_{HC}$ ; $I_{OH} = -32 \mu\text{A}$               |
|                 | Output Voltage                      | V <sub>HC</sub> V <sub>CC</sub> |                                | V  | V <sub>CC</sub> = Min  | $I_{OH} = -300 \mu\text{A}$                            |
|                 |                                     | 2.4 4.3                         |                                |  | $V_{IN} = V_{IH} \text{ or } V_{IL}$                           | $I_{OH} = -12 \text{ mA (Mil)}$                        |
|                 |                                     | 2.4 4.3                         | (2)                            | -(J to HUH)  | used by an input Transition Pair                               | $I_{OH} = -15  \text{mA (Com)}$                        |
| VOL             | Maximum Low Level                   | GND                             | 0.2                            |  | $V_{CC} = 3V; V_{IN} = 0.2V$                                   | or $V_{HC}$ ; $I_{OL} = 300 \mu A$                     |
|                 | Output Voltage                      | GND                             | 0.2                            | ٧  | V <sub>CC</sub> = Min  | $I_{OL} = 300 \mu\text{A}$                             |
|                 |                                     | 0.3                             | 0.50                           | - 1200   | $V_{IN} = V_{IH} \text{ or } V_{IL}$                           | I <sub>OL</sub> = 32 mA (Mil)                          |
|                 |                                     | 0.3                             | 0.50                           |  |  | I <sub>OL</sub> = 48 mA (Com)                          |

DC Characteristics for FCTA Family Devices

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$   $T_A=-55$ °C to +125°C. (Continued)

| Symbol           | Parameter                                    | 54FCTA/                    | 74FC1 | ГА   | Units   | Condi   | tions   |                         |  |
|------------------|--|----------------------------|-------|------|---|---|---|-------------------------|--|
| apV of V         | Parameter                                    | Min Ty                     | p N   | /lax | VAC & TAOM  | 0.0-  |   | 54FOTA<br>Z4SCTA        |  |
| lcc V of V       | Maximum Quiescent<br>Supply Current          | 0.0                        | 01    | 1.5  | 0°mA+ of  | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2V \\ &f_I = 0 \end{aligned}$              |   | Temper<br>74FC<br>54FC  |  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH | 0.                         | 5 4   | 2.0  | o mA - o  | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)  | AT<br>AT  | Storage<br>74FC<br>sasc |  |
| ICCD             | Dynamic Power<br>Supply Current (Note 4)     | 0.2                        | 25 0  | ).45 | mA/MHz  | V <sub>CC</sub> = Max Outputs Open $\overline{OE}$ = GND LE = V <sub>CC</sub> One Input Toggling 50% Duty Cycle | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V   |                         |  |
| oulsv er         | Total Power<br>Supply Current (Note 6)       | 1                          |       |      | Vilms in the local depth of the | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                      | DC C                    |  |
|                  | Conditions                                   | 1.7                        |       | 5.0  | ATORAVI   | LE = V <sub>CC</sub><br>f <sub>I</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle                           | $V_{IN} = 3.4V$ $V_{IN} = GND$                                |                         |  |
|                  |  | 3.                         | 0 8   | 8.0  | IIIA  | (Note 5)  V <sub>CC</sub> = Max  Outputs Open   | $V_{\text{IN}} \ge V_{\text{HC}}$<br>$V_{\text{IN}} \le 0.2V$ | HI,                     |  |
|                  |  |                            |       |      | 8:0   | OE = GND  | d mumbteM   | 11/                     |  |
| ote 2)           | $v_i = v_{QC}$<br>$v_j = 2.7V (N$            | ıM = <sub>00</sub> V<br>5. | ) Au  | 4.5  | 5.0   | LE = V <sub>CC</sub><br>f <sub>I</sub> = 2.5 MHz  | $V_{IN} = 3.4V$<br>$V_{IN} = GND$                             |                         |  |
| (\$ 610          |  | V <sub>GG</sub> = Ma       |       |      | -5.0  | Eight Bits Toggling<br>50% Duty Cycle   |   |                         |  |
| VH               | Input Hysteresis on Clock Only               | 20                         | 0     |      | mV  |   |   |                         |  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

IC = ICC + AICC DHNT + ICCD (fcp/2 + fi Ni)

Icc = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

DH = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

ICCD = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>|</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

### AC Electrical Characteristics: See Section 2 for Waveforms

|                        |  | 54FCTA/74FCTA   | 74               | FCTA                         | 54FCTA   | mima?      |      |
|------------------------|--|---|------------------|------------------------------|--|------------|------|
| Symbol                 | Parameter  | $T_A = +25^{\circ}C$ $V_{CC} = +5.0V$                                     | R <sub>L</sub> : | c = Com<br>= 500Ω<br>= 50 pF | $T_A$ , $V_{CC} = MiI$ $R_L = 500\Omega$ $C_L = 50 pF$                                 | Units      | Fig. |
|                        |  | Тур   | Min              | Max                          | Min Max  | IF O I     | Octa |
| t <sub>PLH</sub>       | Propagation Delay $D_n$ to $\overline{O}_n$      | 4.0   | 1.5              | 5.2                          | noitain  | ns         | 2-8  |
| t <sub>PLH</sub> treat | Propagation Delay                                | SALTAFOTESAA is pin   | 2.0              | 8.5                          | gh-speed, low-power oc<br>ta D-type Inputs for eac                                     | ns at AAER | 2-8  |
| t <sub>PZH</sub>       | Output Enable<br>Time                            | bodin squ-s beleggin<br>oggid-egb 5,5/dleog bet<br>o level tughe bos fude | 1.5              | 16 of 6.5                    | for bus-onemed applications (SE) are a start (SE) are a start is the same as the first | ns O)      | 2-11 |
| t <sub>PHZ</sub>       | Output Disable Time                              | nguts accent CMOS ler<br>Qurrent later up                                 | 1.5              | 5.5                          | are inverted.  | ns ns      | 2-11 |
| ts                     | Set Up Time<br>High or Low<br>Dn to LE           | 48 mA (Com), 32 mA<br>y producto.pmpliant to                              | 2.0              |                              |  | ns         | 2-10 |
| t <sub>H</sub>         | HOLD Time<br>High or Low<br>D <sub>n</sub> to LE | onnoO <sup>1.0</sup>  | 1.5              |                              | 10: See Section 8  | ns         | 2-10 |
| tw                     | LE Pulse Width<br>High or Low                    | 4.0   | 5.0              | 1931                         |  | ns         | 2-9  |

Minimum limits are guaranteed but not tested on Propagation Delays

### Capacitance (TA = +25C, f = 1.0 MHz)

| Symbol | Parameter          | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| Cin    | Input Capacitance  | 6   | 10  | pF    | V <sub>IN</sub> = 0V  |
| Cout 5 | Output Capacitance | 8   | 12  | pF    | V <sub>out</sub> = 0V |

Note: This parameter is measured at characterization but not tested

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### 54FCT/74FCT534A Octal D Flip-Flop with TRI-STATE® Outputs

### **General Description**

The 'FCT534A is a high-speed, low-power octal D-type flipflop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops. The 'FCT534A is the same as the 'FCT374A except that the outputs are inverted.

### **Features**

■ NSC 54/74FCT534A is pin and functionally equivalent to IDT 54/74FCT534A

AC Electrical Characteristics: see section 2 for Waveforms

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TTL input and output level compatible
- TTL inputs accept CMOS levels
- High current latch up
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- Military product compliant to MIL-STD-883

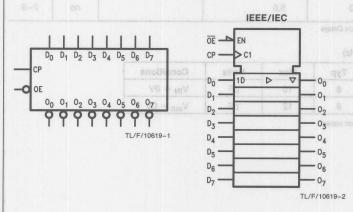
Ordering Code: See Section 8

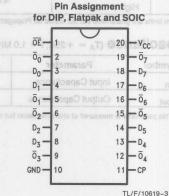
**Logic Symbols** 

### **Connection Diagrams**

DateL

Paramater





| Pin Names                         | Description                     |
|-----------------------------------|---------------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                     |
| CP                                | Clock Pulse Input               |
| ŌĒ                                | TRI-STATE Output Enable Input   |
| $\overline{O}_0 - \overline{O}_7$ | Complementary TRI-STATE Outputs |

## 3 D<sub>0</sub> 2 Ō<sub>0</sub> 1 ŌE 20 V<sub>CC</sub>

O<sub>3</sub> 9 GND 10 CP 11 O<sub>4</sub> 12 D<sub>4</sub> 13 19 07 14 15 16 17 18 D5 05 06 D6 D7

Pin Assignment for LCC

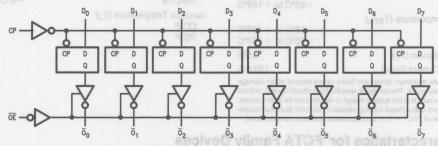
TL/F/10619-4

### Functional Description

The 'FCT534A consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP)

transition. With the Output Enable  $(\overline{OE})$  LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

### **Logic Diagram**



TL/F/10619-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### **Function Table**

|  |                                     |  |                   |       |                  |  | inction lable | run      |   |
|--|-------------------------------------|--|-------------------|-------|------------------|--|---------------|----------|---|
|  |                                     |  |                   | ATO   | tput             | Ou   | Core          | Inputs   |   |
|  |                                     |  |                   | nelli | ō                | D  | D             | OE       | СР  |
|  | Minimum High Level<br>Input Voltage |  |                   |       | L <sub>V</sub>   | L  |               | L<br>L   | 5   |
|  |                                     |  |                   | 8.0   | Σ <sub>0</sub> γ | X X  |               | L<br>H   | L<br>X  |
|  |                                     |  |                   |       | Au               |  |               | ge Level | H = HIGH Volta<br>L = LOW Voltag<br>X = Immaterial              |
|  |                                     |  |                   |       |                  |  |               |          | Z = LOW-to-H<br>$Z = High Impedia \overline{O}_0 = Value store$ |
|  |                                     |  |                   |       | Au               |  |               |          |   |
|  |                                     |  |                   |       |                  |  |               |          |   |
|  |                                     |  |                   |       |                  |  |               |          |   |
|  | Minimum High Level                  |  |                   |       |                  |  |               |          |   |
|  |                                     |  | Voc<br>4.9<br>4.8 |       | ٧                |  |               |          |   |
|  |                                     |  |                   |       |                  |  |               |          |   |
|  |                                     |  |                   |       |                  | $V_{CC} = Min$ $V_{IN} = V_{HH} \text{ or } V$ |               |          |   |
|  |                                     |  |                   |       |                  |  |               |          |   |

### **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTERM)

-0.5V to +7.0V54FCTA 74FCTA -0.5V to +7.0V

Temperature Under Bias (TBIAS) 74FCTA

54FCTA -65°C to +135°C Storage Temperature (TSTG)

74FCTA

-65°C to +150°C 54FCTA Power Dissipation (PT) 0.5W DC Output Current (IOUT)

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM FCT circuits outside databook specifications.

### Recommended Operating **Conditions**

Supply Voltage (V<sub>CC</sub>)

4.5V to 5.5V 54FCTA 74FCTA 4.75V to 5.25V Input Voltage OV to VCC

OV to VCC

Output Voltage

Operating Temperature (TA) 54FCTA -55°C to +125°C 74FCTA -0°C to +70°C

Junction Temperature (T<sub>J</sub>)

175°C CDIP PDIP 140°C

**DC Characteristics for 'FCTA Family Devices** 

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to +125°C. Vuc = Vcc - 0.2V.

-55°C to +125°C

-55°C to +125°C

120 mA

| Symbol          | Parameter                           | 54F                     | CTA/74I                       | FCTA                           | Units | uO.                                 |  | Conditions                              |   |
|-----------------|-------------------------------------|-------------------------|-------------------------------|--------------------------------|-------|-------------------------------------|--|---|---|
| Symbol          |                                     | Min                     | Тур                           | Max                            |       |                                     | d  | 30                                      | 90  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage | 2.0                     |                               |                                | V     |                                     | В  | 1                                       |   |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     |                         |                               | 0.8                            | V 3   |                                     | X  | H                                       | ×   |
| Іін             | Input High Current                  |                         |                               | 5.0<br>5.0                     | μА    | V <sub>CC</sub> =                   | = Max  | $V_{I} = V_{I}$ $V_{I} = V_{I}$         | V <sub>CC</sub><br>2.7V (Note 2)              |
| I <sub>IL</sub> | Input Low Current                   |                         |                               | -5.0<br>-5.0                   | μА    | V <sub>CC</sub> =                   | $V_{CC} = Max$ $V_I = 0.5V \text{ (Note 2)}$ $V_I = GND$ |   |   |
| loz             | Maximum TRI-STATE Current           |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ    | V <sub>CC</sub> =                   | = Max  |   | 2.7V (Note 2)<br>0.5V (Note 2)                |
| VIK             | Clamp Diode Voltage                 |                         | -0.7                          | -1.2                           | ٧     | V <sub>CC</sub> =                   | Min; I <sub>N</sub> = -                                  | 18 mA                                   |   |
| los             | Short Circuit Current               | -60                     | -120                          |                                | mA    | V <sub>CC</sub> =                   | Max (Note 1  | ); V <sub>O</sub> = GNE                 | )   |
| V <sub>OH</sub> | Minimum High Level                  | 2.8                     | 3.0                           |                                |       | V <sub>CC</sub> =                   | = 3V; V <sub>IN</sub> = 0                                | .2V or V <sub>HC</sub> ; I <sub>(</sub> | DH = -32 μA                                   |
|                 | Output Voltage                      | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧     | V <sub>CC</sub> = V <sub>IN</sub> = | = Min<br>V <sub>IH</sub> or V <sub>IL</sub>              | I <sub>OH</sub> =                       | = -300 μA<br>= -12 mA (Mil)<br>= -15 mA (Com) |
| V <sub>OL</sub> | Maximum Low Level                   |                         | GND                           | 0.2                            |       | V <sub>CC</sub> =                   | = 3V; V <sub>IN</sub> = 0                                | .2V or V <sub>HC</sub> ; I <sub>0</sub> | $DL = 300 \mu A$                              |
|                 | Output Voltage                      |                         | GND<br>0.3<br>0.3             | 0.2<br>0.5<br>0.5              | ٧     | V <sub>CC</sub> = V <sub>IN</sub> = | = Min<br>V <sub>IH</sub> or V <sub>IL</sub>              | I <sub>OL</sub> =                       | 300 μA<br>32 mA (Mil)<br>48 mA (Com)          |
| V <sub>H</sub>  | Input Hysteresis on<br>Clock Only   |                         | 200                           |                                | mV    |                                     |  |   |   |

DC Characteristics for 'FCTA Family Devices (Continued) Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55^{\circ}C$ to +125°C,  $V_{HC} = V_{CC} - 0.2V$ .

| Symbol     | Parameter |                                      | 54FCTA/74F  | FCTA       | Units  | - oov  | Conditions                                | Bymbol             |
|------------|-----------|--------------------------------------|-------------|------------|--------|--|---|--------------------|
| Symbol     |           | Parameter 30                         | Min Typ     | Max        | Offics |  | Conditions                                |                    |
| lcc<br>e-s |           | mum Quiescent                        | 0.001       | 1.5<br>8.1 | mA     | $V_{CC} = Max$ $V_{IN} \ge V_{HC}$ , $f_I = 0$                                       | V <sub>IN</sub> ≤ 0.2V                    | PLH                |
| ΔICC       |           | scent Supply Current;<br>Inputs HIGH | a.e 0.5     | 2.0        | mA a   | $V_{CC} = Max$<br>$V_{IN} = 3.4V$  |   | PZH                |
| ICCD       |           | mic Power<br>ly Current (Note 4)     | a.a<br>0.15 | 0.40       | mA/MHz | V <sub>CC</sub> = Max<br>Outputs Ope<br>$\overline{\text{OE}}$ = GND<br>One Input To | en V <sub>IN</sub> ≤ 0.2V                 | 8<br>PHC<br>ZHZ    |
| lc -       | 1         | Power Supply                         |             | 1.5        | 0      | $V_{CC} = Max$   | ycle V <sub>IN</sub> ≥ V <sub>HC</sub>    | d                  |
|            | Curre     | ent (Note 6)                         | 1.5         | 4.0        | 0      | Outputs Ope<br>f <sub>CP</sub> = 10 Mi<br>OE = GND                                   |   | 19                 |
|            |           |                                      | 1.8         | 6.0        |        | fl = 5 MHz<br>One Bit Tog<br>50% Duty C  |   | Capa               |
|            |           | Conditions                           | (Jnlite     | XE         | mA     | (Note 5)   | V <sub>IN</sub> ≥ V <sub>HC</sub>         | miya               |
|            |           | $V0 = y_0V$                          |             | 0          |        | V <sub>CC</sub> = Max  | V <sub>IN</sub> ≤ 0.2V                    |                    |
|            |           | V0 = TuoV                            | 3,0         | 7.8        |        | Outputs Ope<br>$\overline{OE} = GND$<br>$f_{CP} = 10 MH$                             | semants is the sure at characte           | Cour<br>Note: This |
|            |           |                                      | 5.0         | 16.8       |        | f <sub>I</sub> = 2.5 MHz<br>Eight Bits To<br>50% Duty C                              | oggling $V_{IN} = 3.4V$<br>$V_{IN} = GND$ |                    |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Numbers of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

| Symbol           | Parameter                                 | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = 5.0V | arm:            | cc =<br>Mil<br>50 pF | Com<br>C <sub>L</sub> = 50 pF      | Units | Fig. |
|------------------|---|--|-----------------|----------------------|------------------------------------|-------|------|
|                  | 25  | M = OOVTyp                                       | Min<br>(Note 1) | Max                  | Min Max<br>(Note 1)                | eixaM | col  |
| t <sub>PLH</sub> | Propagation Delay<br>C <sub>P</sub> to On | 0 = 14.5   | 1.5             | 6.5                  | y Current                          | ns    | 2-9  |
| t <sub>PZH</sub> | Output Enable<br>Time                     | N.E = MV 5.5 Am                                  | 1.5             | 6.5                  | cent Supply Current:<br>spots HIGH | The   | 2-11 |
| t <sub>PHZ</sub> | Output Disable<br>Time                    | M = 00V<br>DebuginO 4.0                          | 1.5             | 5.5                  | nic Power<br>y Current (Note 4)    | ns    | 2-11 |
| ts               | Set Up Time High or Low<br>Dn to CP       | regni snO1.0                                     | 2.0             |                      |                                    | ns    | 2-10 |
| t <sub>h</sub>   | Hold Time High or Low<br>Dn to CP         | M = 00V 1.0                                      | 1.5             |                      | Power Supply                       | ns    | 2-10 |
| t <sub>w</sub>   | CP Pulse Width<br>High or Low             | 01 = 90 4.0                                      | 5.0             |                      | (9-019A) III                       | ns    | 2-9  |

Note 1: Minimum limits guaranteed but not tested on propagation delays.

### Capacitance $T_A = +25^{\circ}C$ , $f_I = 1.0 \text{ MHz}$

| Symbol           | Parameter          | Тур      | Max    | Units | Conditions            |
|------------------|--------------------|----------|--------|-------|-----------------------|
| CIN VS.0         | Input Capacitance  | 6        | 10     | pF    | V <sub>IN</sub> = 0V  |
| C <sub>OUT</sub> | Output Capacitance | 8 Output | 12 8 7 | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

# 54FCT/74FCT543A Octal Registered Transceiver

### **General Description**

The FCT543A octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow.

FACT™ FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

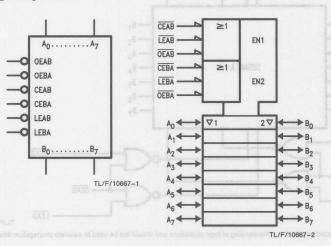
FACT FCTA features undershoot correction and split ground bus for superior performance.

### **Features**

- NSC 54FCT/74FCT543A is pin and functionally equivalent to IDT 54FCT/74FCT543A
- Speed controls for data flow in each direction
- Back to back latched transceiver
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (com), 48 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product complaint to MIL-STD 883

### Ordering Code: See Section 8

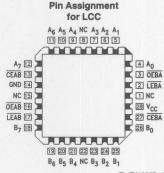
### **Logic Symbols**



### **Connection Diagrams**



| Pin Names                      | Description                             |  |  |  |  |  |  |
|--------------------------------|---|--|--|--|--|--|--|
| OEAB                           | A-to-B Output Enable Input (Active LOW) |  |  |  |  |  |  |
| OEBA                           | B-to-A Output Enable Input (Active LOW) |  |  |  |  |  |  |
| CEAB                           | A-to-B Enable Input (Active LOW)        |  |  |  |  |  |  |
| CEBA                           | B-to-A Enable Input (Active LOW)        |  |  |  |  |  |  |
| LEAB                           | A-to-B Latch Enable Input (Active LOW)  |  |  |  |  |  |  |
| LEBA                           | B-to-A Latch Enable Input (Active LOW)  |  |  |  |  |  |  |
| A <sub>0</sub> -A <sub>7</sub> | A-to-B Data Inputs or                   |  |  |  |  |  |  |
|                                | B-to-A TRI-STATE® Outputs               |  |  |  |  |  |  |
| B <sub>0</sub> -B <sub>7</sub> | B-to-A Data Inputs or                   |  |  |  |  |  |  |
|                                | A-to-B TRI-STATE Outputs                |  |  |  |  |  |  |



TL/F/10667-4

7

### **Functional Description**

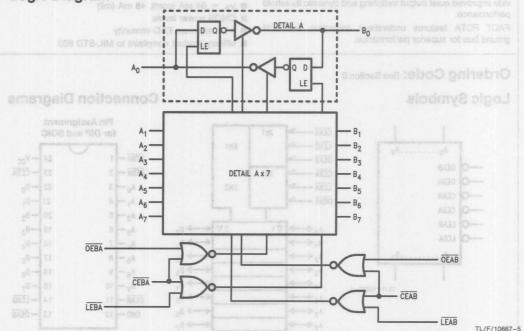
The FCT543A contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{\text{CEAB}}$ ) input must be LOW in order to enter data from A<sub>0</sub>-A<sub>7</sub> or take data from B<sub>0</sub>-B<sub>7</sub>, as indicated in the Data I/O Control Table. With  $\overline{\text{CEAB}}$  LOW, a LOW signal on the A-to-B Latch Enable ( $\overline{\text{LEAB}}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{\text{LEAB}}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{\text{CEAB}}$  and  $\overline{\text{OEAB}}$  both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$  and  $\overline{\text{OEBA}}$  inputs,

### Data I/O Control Table

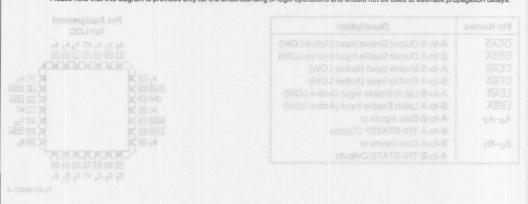
|      | Input |      | Latch Status | Output Buffers |  |  |
|------|-------|------|--------------|----------------|--|--|
| CEAB | LEAB  | OEAB | Laton Status | Output Duners  |  |  |
| Н    | X     | X    | Latched      | High Z         |  |  |
| X    | Н     | X    | Latched      | losoft.        |  |  |
| L    | L     | X    | Transparent  | HOVO C         |  |  |
| X    | X     | Н    | _            | High Z         |  |  |
| L    | X     | regi | rginose@ (   | Driving        |  |  |

- H = HIGH Voltage Level
- L = LOW Voltage Level | 0 eponds yrenogmel to 1 sorfols
- X = Immaterial
  - A-to-B data flow shown; B-to-A flow control
  - is the same, except using CEBA, LEB and OEBA

### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Terminal Voltage with Respect to GN     | D (V <sub>TERM</sub> ) |
|---|------------------------|
| 54FCTA                                  | -0.5V to $+7.0V$       |
| 74FCTA                                  | -0.5V to $+7.0V$       |
| Temperature under Bias (TBIAS)          |                        |
| 74FCTA (8 eight) VA 8 =                 | -55°C to +125°C        |
| 54FCTA                                  | -65°C to +135°C        |
| Storage Temperature (T <sub>STG</sub> ) |                        |
|   | -55°C to +125°C        |
| 54FCTA                                  | -65°C to +150°C        |
| Power Dissipation (P <sub>T</sub> )     | 0.544                  |
| DC Output Current (IOUT)                | 120 mA                 |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

### Absolute Maximum Ratings (Note 1) Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> )<br>54FCTA | 4.5V to 5.5V                    |
|---|---------------------------------|
| 74FCTA                                      | 4.75V to 5.25V                  |
| Input Voltage                               | 0V to V <sub>CC</sub>           |
| Output Voltage                              | OV to V <sub>CC</sub>           |
| Operating Tomporature (T.)                  | −55°C to +125°C<br>0°C to +70°C |
| Junction Temperature (T <sub>J</sub> )      |                                 |
| CDIP  | 175°C                           |
| PDIP  | 140°C                           |
|   |                                 |

### **DC Characteristics for 'FCTA Family Device**

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$  to  $+125^{\circ}C$ ,  $V_{CC} = V_{CC} = 0.2V$ 

| Symbol          | Parameter                              | 54F                           | CTA/74F                       | CTA                 | Units        | Conditions   |   |  |
|-----------------|--|-------------------------------|-------------------------------|---------------------|--------------|--|---|--|
| Symbol          | raidiffeter                            | Min                           | Тур                           | Max                 | Office       |  | onations  |  |
| VIH             | Minimum High Level Input Voltage       | 2.0                           |                               | 70                  | ST V 0       | 2  |   |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage        | CEAS S                        |                               | 0.8                 | ٧            |  |   |  |
| HI<br>4.8 = p   | Input Current<br>(Except I/O Pins)     |                               |                               | 5.0<br>5.0          | μΑ           | V <sub>CC</sub> = Max  | $V_I = V_{CC}$ $V_I = 2.7V \text{ (Note 2)}$  |  |
| IIL - N         | Input Low Current<br>(Except I/O Pins) | Eght Bi                       |                               | -5.0<br>-5.0        | μΑ           | V <sub>CC</sub> = Max  | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$   |  |
| l <sub>IH</sub> | Input High Currents<br>(I/O Pins)      | AU at 60                      | emit evio ta t                | 15<br>15            | μΑ           | V <sub>CC</sub> = Max  | $V_I = V_{CC}$ $V_I = 2.7V$   |  |
| IIL             | Input Low Currents<br>(I/O Pins)       |                               | anolinions.                   | -15<br>-15          | μА           | V <sub>CC</sub> = Max  | $V_{l} = 0.5V$  |  |
| V <sub>IK</sub> | Clamp Diode Voltage                    | Liotest                       | -0.7                          | -1.2                | V            | $V_{CC} = Min; I_N = -1$                                     | 8 mA  |  |
| los             | Short Circuit Current                  | -60                           | -120                          |                     | mA           | V <sub>CC</sub> = Max (Note 1);                              | V <sub>O</sub> = GND  |  |
|                 | Minimum High Level                     | 2.8                           | 3.0                           |                     | (VA.E        | $V_{CC} = 3V; V_{IN} = 0.2$                                  | V or $V_{HC}$ ; $I_{OH} = -32 \mu\text{A}$  |  |
| V <sub>OH</sub> | Output Voltage                         | V <sub>HC</sub><br>2.4<br>2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                     | V            | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$          | $I_{OH} = -300 \mu A$<br>$I_{OH} = -12 \text{ mA (Mil)}$<br>$I_{OH} = -15 \text{ mA (Com)}$ |  |
|                 | Maximum Low Level                      |                               | GND                           | 0.2                 | Register Dai | $V_{CC} = 3V; V_{IN} = 0.2$                                  | V or $V_{HC}$ ; $I_{OL} = 300 \mu A$  |  |
| V <sub>OL</sub> | Output Voltage                         |                               | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55 | V            | $V_{CC} = Min$ $V_{IN} = V_{IL} \text{ or } V_{IL}$          | $I_{OL} = 300 \mu A$<br>$I_{OL} = 48 \text{ mA (Mil)}$<br>$I_{OL} = 64 \text{ mA (Com)}$    |  |
| loc             | Maximum Quiescent<br>Supply Current    |                               | 0.001                         | 1.5                 | mA           | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2$ $f_I = 0$ | v   |  |

| Symbol   | Parameter   | 54F0                       | 17.0        | Jnits        |  | Conditions   |                                |  |  |
|--|---|----------------------------|-------------|--------------|--|--|--------------------------------|--|--|
| 201 01 41  |   | Min                        | Тур         | Max          | V0.7-  | or Va.o  |                                |  | ZAFCTA                                 |
| ΔI <sub>CC</sub>   | Quiescent Supply Current;<br>TTL Inputs HIGH  | Tempera                    | 0.5         | 0.2          | orași  | mA .   | _                              | Max<br>3.4V (Note 3)   | raperature<br>74FCTA -                 |
| TAVE<br>O'AVE  | Dynamic Power<br>Supply Current (Note 4)  |                            | 0.25        | 0.55         | mA   | A/MHz  | CEAB One In                    | Max Outputs Open  ROEAB = GND  VCC  out Toggling  uty Cycle  | $V_{IN} \ge V_{H}$ $V_{IN} \le 0.2$    |
| lc   | Total Power<br>Supply Current (Note 6)  |                            | 1.5         | 4.0          | egernal<br>eruskibr<br>enokito<br>elos bi i<br>selelah | o doktw bno<br>nap grifen n<br>doeds spoot<br>fised med<br>neding va | 50% D<br>CEAB                  | s Open<br>10 MHz<br>uty Cycle<br>& ŌEAB = GND  | $V_{IN} \ge V_{H}$ $V_{IN} \le 0.2$    |
|  | nditions shown as Max, use $eq:max_max_max_max_max_max_max_max_max_max_$  | or test or                 |             | 6.0          | dini<br>dan bi<br>vo.a                                 | ns freidr  | One Bit<br>at f <sub>I</sub> = | EAB = 10 MHz<br>Toggling   | $V_{IN} = 3.4$ $V_{IN} = GN$           |
|  |   |                            |             | U X          |  | mA   | (Note 5                        |  | lodm                                   |
|  |   |                            | 3.0         | 16.5         |  |  | Outputs<br>t <sub>CP</sub> =   | The state of the s | $V_{IN} \ge V_{H}$<br>$V_{IN} \le 0.2$ |
|  |   |                            |             |              | 30   |  |                                | ROEAB = GND  | dat .                                  |
| lote 2)  |   | oc = Ma                    |             | 21.75        | 98<br>98   |  | $f_{CP} = \bar{I}$             | EAB = 10 MHz   | V <sub>IN</sub> = 3.4                  |
| (S etal  |   | oc = Me                    |             |              | 8-   |  | at f <sub>I</sub> =            | its Toggling<br>5 MHz<br>uty Cycle   | V <sub>IN</sub> = GN                   |
|  | imum test duration not to exceed one  | second, not                | more than o | one output   | shorted  | at one tim   | е.                             | O Pins)  | vit i                                  |
| Note 3: Per  | parameter guaranteed but not tested.<br>TTL driven input (V <sub>IN</sub> = 3.4V); all other<br>parameter is not directly testable, but |                            | D A         | al Power S   | Supply o   | alculations.   |                                |  |  |
|  | es for these conditions are examples  | of the I <sub>CC</sub> fo  | rmula. Thes | e limits are | guaran   | nteed but no   | ot tested.                     |  |  |
|  | QUIESCENT + INPUTS + IDYNAMIC ICC + ΔICC DHNT + ICCD (fcp/2 +   | fi Ni)                     |             |              |  |  |                                |  |  |
|  | = Quiescent Current   |                            |             |              |  |  |                                |  |  |
|  | = Power Supply Current for a TTL H  | igh Input (VII             | N = 3.4V    |              |  |  |                                |  |  |
| DH -   | <ul> <li>Duty Cycle for TTL Inputs High</li> <li>Number of Inputs at DH</li> </ul>  |                            |             |              |  |  |                                |  |  |
|  | Transpor or impate at DH  | ut Transition              | Pair (HLH   | or LHL)      |  |  |                                |  |  |
| N <sub>T</sub>   | = Dynamic Current Caused by an Inc  |                            | and and     |              | 0  |  |                                |  |  |
| (IM) N <sub>T</sub> =                                    | <ul> <li>Dynamic Current Caused by an Inp</li> <li>Clock Frequency for Register Device</li> </ul>                                       |                            | Non-Registe | J. DOVIOUS   |  |  |                                |  |  |
| N <sub>T</sub> = ICCD f <sub>CP</sub> = f <sub>I</sub> = | <ul> <li>Clock Frequency for Register Device<br/>Input Frequency</li> </ul>   |                            | Non-Registe |              |  |  |                                |  |  |
| $N_T = I_{CCD}$ $f_{CP} = f_1 = N_1 = I_{CD}$            | Clock Frequency for Register Device<br>Input Frequency     Number of Inputs at f <sub>I</sub>   | es (Zero for               | V           |              |  |  |                                |  |  |
| $N_T = I_{CCD}$ $f_{CP} = f_1 = N_1 = AII c$             | <ul> <li>Clock Frequency for Register Device<br/>Input Frequency</li> </ul>   | es (Zero for               | V           |              |  |  |                                |  |  |
| $N_T = I_{CCD}$ $f_{CP} = f_1 = N_1 = AII c$             | Clock Frequency for Register Device Input Frequency     Number of Inputs at f <sub>1</sub> urrents are in millamps and all frequents.   | es (Zero for cies are in m | negahertz.  |              |  |  |                                |  |  |

| <b>AC Electrical Chara</b> | acteristics: See Section 2 | for Waveforms | lenoit | olAl | P.W. |
|----------------------------|----------------------------|---------------|--------|------|------|
|                            | 54FCTA/74FCTA              | 74FCTA        | 54FCTA |      | 1987 |

|                                      |   | 54FCTA/74FCTA   | 74FCTA   | 54FCTA  |          |      |
|--------------------------------------|---|---|--|---|----------|------|
| Symbol                               | Parameter   | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$                                      | $T_A$ , $V_{CC} = Com$ $R_L = 500\Omega$ $C_L = 50 pF$ | $T_A$ , $V_{CC}=Mil$ $R_L=500\Omega$ $C_L=50pF$                                       | Units    | Fig. |
|                                      |   | Тур   | Min<br>(Note)  | Min Max   | A la     | Oct  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>Transparent Mode<br>A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub> | NATURES<br>HSC 54FCT/74FCT54<br>ant to IDT 54FCT/74I                      | 1.5 6.5  | escription :tal transceiver contains to   | ns<br>ns | 2-8  |
| t <sub>PLH</sub>                     | Propagation Delay  LEAB to An,  LEAB to Bn  | lack to back registers<br>lata flow in each direc<br>nout clamp diodes to |  | acti Enable and Curput I<br>n register to permit indep<br>putling in either direction |          | 2-8  |
| t <sub>PZH</sub>                     | Output Enable Time OEBA or OEAB to An or Bn CEBA or CEAB to An or Bn  | DL = .64 mA (Com), 4<br>MOS power levels<br>AV minkeum ESD in             |  | tilizes NSC quiet series to<br>ist output switching and d                             |          | 2-11 |
| t <sub>PHZ</sub>                     | Output Disable Time OEBA or OEAB to An or Bn CEBA or CEAB to An or Bn   | Ailitery Product compl  | 2 7.5  | stures undershoot com<br>uperior performance.   | ns       | 2-11 |
| tsu                                  | Set Up Time<br>High or Low<br>An or Bn to LEBA or LEAB  | 00  | 2  | Code: See Section 8   | ns       | 2-10 |
| tH                                   | Hold Time   |   | 23   |   | ns       | 2-10 |

Note: Minimum propagation delays are guaranteed but not listed.

### Capacitance TA = +25°C, f = 1.0 MHz

| 7      |                    |     | The second secon |         | 100                   |
|--------|--------------------|-----|--|---------|-----------------------|
| Symbol | Parameter (Note)   | Тур | Max  | Units   | Conditions            |
| CIN    | Input Capacitance  | 6   | 10   | pF 7830 | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12   | pF      | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.



### 54FCT/74FCT544A **Octal Registered Transceiver**

### **General Description**

The 'FCT544A octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The 'FCT544A inverts data in both directions.

FACTTM FCTA utilizes NSC quiet series technology to provide improved guiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

### **Features**

■ NSC 54FCT/74FCT544A is pin and functionally equivalent to IDT 54FCT/74FCT544A

AC Electrical Characteristics: see Section 2 for Waveforms

- Back to back registers for storage separate controls for data flow in each direction
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

Ordering Code: See Section 8

### **Logic Symbols**

### **Connection Diagrams**

-V<sub>CC</sub>

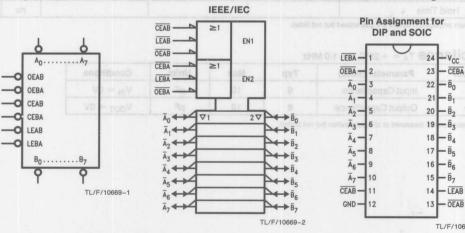
- B<sub>5</sub>

- B<sub>6</sub>

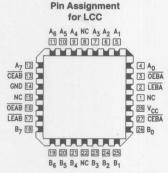
- OEAB

TL/F/10669-3

Symbol



| Pin Names                         | Description                             |  |  |
|-----------------------------------|---|--|--|
| OEAB                              | A-to-B Output Enable Input (Active LOW) |  |  |
| OEBA                              | B-to-A Output Enable Input (Active LOW) |  |  |
| CEAB                              | A-to-B Enable Input (Active LOW)        |  |  |
| CEBA                              | B-to-A Enable Input (Active LOW)        |  |  |
| LEAB                              | A-to-B Latch Enable Input (Active LOW)  |  |  |
| LEBA                              | B-to-A Latch Enable Input (Active LOW)  |  |  |
| $\overline{A}_0 - \overline{A}_7$ | A-to-B Data Inputs or B-to-A            |  |  |
|                                   | TRI-STATE® Outputs                      |  |  |
| $\overline{B}_0 - \overline{B}_7$ | B-to-A Data Inputs or A-to-B            |  |  |
|                                   | TRI-STATE Outputs                       |  |  |



### Functional Description

The 'FCT544A contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable  $(\overline{CEAB})$  input must be LOW in order to enter data from  $\overline{A}_0-\overline{A}_7$  or take data from  $\overline{B}_0-\overline{B}_7$ , as indicated in the Data I/O Control Table. With  $\overline{CEAB}$  LOW, a LOW signal on the A-to-B Latch Enable ( $\overline{LEAB}$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $\overline{LEAB}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}$  and  $\overline{OEAB}$  both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$  outputs.

Data I/O Control Table

| Input |      |      | Latch       | Output            |
|-------|------|------|-------------|-------------------|
| CEAB  | LEAB | OEAB | Status      | Buffers           |
| H     | X    | X    | Latched     | High-Z            |
| X     | Н    | X    | Latched     | ALOTAL            |
| L     | L    | X    | Transparent | mperature         |
| X     | X    | Н    |             | High-Z            |
| L     | X    | L    | 77          | High-Z<br>Driving |

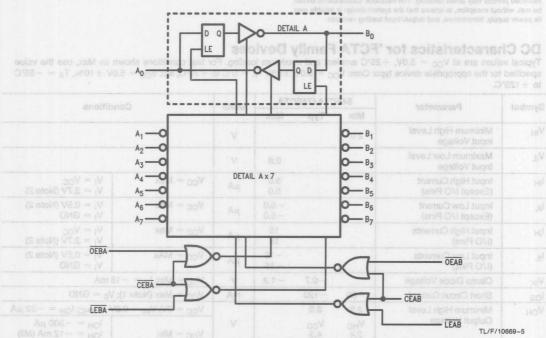
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using CEBA, LEBA and OEBA.

### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

7

#### **Absolute Maximum Ratings (Note)**

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Terminal Voltage with Respect to G      | IND (V <sub>TERM</sub> ) |
|---|--------------------------|
| 54FCTA                                  | -0.5V to $+7.0V$         |
| 74FCTA                                  | -0.5V to $+7.0V$         |
| Temperature under Bias (TBIAS)          |                          |
| 54FCTA                                  | -65°C to +135°C          |
| 74FCTA                                  | -55°C to +125°C          |
| Storage Temperature (T <sub>STG</sub> ) |                          |
| 54FCTA                                  | -65°C to +150°C          |
| 74FCTA                                  | -55°C to +125°C          |
| Power Dissipation (P <sub>T</sub> )     | A-01-S (1990) 0.5W       |
| DC Output Current (I <sub>OUT</sub> )   | 120 mA                   |

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

### Recommended Operating

| Supply Voltage (V <sub>CC</sub> )        |                       |
|--|-----------------------|
| 54FCTA                                   | 4.5V to 5.5V          |
| 74FCTA                                   | 4.75V to 5.25V        |
| Input Voltage                            | 0V to V <sub>CC</sub> |
| Output Voltage                           | 0V to V <sub>CC</sub> |
| Operating Temperature (T <sub>A</sub> )  |                       |
| -154FCTA ne spom sperote art ni serio    |                       |
| 74FCTA                                   |                       |
| Junction Temperature (T <sub>J</sub> )   |                       |
| CUID AND THE PROPERTY OF THE COLD PARTY. | 175°C                 |
| PDIP of ted assimilar, but a mort wol    |                       |
|  |                       |

**DC Characteristics for 'FCTA Family Devices** 

Typical values are at V<sub>CC</sub> = 5.0V,  $+25^{\circ}$ C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V<sub>CC</sub> = 5.0V  $\pm 5\%$ , T<sub>A</sub> = 0°C to  $+70^{\circ}$ C; Mil: V<sub>CC</sub> = 5.0V  $\pm 10\%$ , T<sub>A</sub> =  $-55^{\circ}$ C to  $+125^{\circ}$ C.

| Symbol           | Parameter                                    | 54F                     | CTA/74F                       | CTA                 | Units  | Conditions   |   |
|------------------|--|-------------------------|-------------------------------|---------------------|--|--|---|
| Symbol           | raidilletei                                  | Min                     | Тур                           | Max                 | Ollits   | and the same of th | iditions  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                     | Musik                         |                     | ٧  | 0-14   |   |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           | O                       |                               | 0.8                 | ٧  | 0-ja   |   |
| liн              | Input High Current<br>(Except I/O Pins)      | 10-14<br>20-15          |                               | 5.0<br>5.0          | μΑ   | V <sub>CC</sub> = Max  | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| IIL              | Input Low Current<br>(Except I/O Pins)       | 8C                      |                               | -5.0<br>-5.0        | μΑ   | V <sub>CC</sub> = Max  | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND                                      |
| liн              | Input High Currents<br>(I/O Pins)            |                         |                               | 15<br>15            | μΑ   | V <sub>CC</sub> = Max  | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| l <sub>IL</sub>  | Input Low Currents<br>(I/O Pins)             | 170                     |                               | -15<br>-15          | μА   | $V_{CC} = MAx$   | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND                                      |
| V <sub>IK</sub>  | Clamp Diode Voltage                          | Section 1               | -0.7                          | -1.2                | V  | $V_{CC} = Min; I_N = -1$   | 8 mA  |
| los              | Short Circuit Current                        | -60                     | -120                          | and the second      | mA   | V <sub>CC</sub> = Max (Note 1);  | $V_0 = GND$   |
| VoH              | Minimum High Level                           | 2.8                     | 3.0                           |                     | CONCESSOR OF THE PERSON OF THE | $V_{CC} = 3V; V_{IN} = 0.2$  | $2V \text{ or } V_{HC}; I_{OH} = -32 \mu$   |
| 8-9890           | Output Voltage                               | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                     | V  | V <sub>CC</sub> = Min<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  | $I_{OH} = -300 \mu A$<br>$I_{OH} = -12 \text{ mA (Mil)}$<br>$I_{OH} = -15 \text{ mA (Cor)}$ |
| VOL              | Maximum Low Level                            |                         | GND                           | 0.2                 |  | $V_{CC} = 3V; V_{IN} = 0.2$  | $2V \text{ or } V_{HC}; I_{OL} = 300 \mu A$   |
|                  | Output Voltage                               |                         | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55 | V  | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | I <sub>OL</sub> = 300 μA<br>I <sub>L</sub> = 48 mA (Mil)<br>I <sub>OL</sub> = 64 mA (Com)   |
| lcc              | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                 | mA   | $ \begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2 \\ &f_I = 0 \end{aligned} $  | 2V  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                 | mA   | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   |   |

#### DC Characteristics for 'FCTA Family Devices (Continued) 181081840 [80110013 OA

Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_{A} = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_{A} = -55^{\circ}C$ 

| Symbol | Parameter                                | 54F    | CTA/7  | 4FC  | TA    | Units        | Conditions  |
|--------|--|--------|--------|------|-------|--------------|---|
| Symbol | raidilletei                              | Min    | Тур    | 0    | Max   |              | Conditions  |
| ICCD   | Dynamic Power<br>Supply Current (Note 4) | natA ( | r otoM | rill | 1     | Typ          | V <sub>CC</sub> = Max<br>Outputs Open   |
| 2-6    | in .                                     | 7.0    | 0.25   | 1.6  | 0.3   | mA/MHz       |   |
| Ics    | Total Power Supply<br>Current (Note 6)   | 0,8    | 1.5    | 1.5  | 4.0   |              | $V_{CC} = Max$ Outputs Open $f_{CP} = 10 \text{ MHz}$ $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2$  |
|        | en                                       | 8      |        |      |       |              | CEAB + OEAB = GND CEBA = VCC.   |
|        | in .                                     | 7.5    | 1.8    |      | 6.0   | mA           | $\begin{array}{l} \text{f}_{\text{CP}} = \overline{\text{LEAB}} = 10 \text{ MHz} \\ \text{One Bit Toggling} \\ \text{at f}_1 = 5 \text{ MHz} \\ \text{50\% Duty Cycle} \\ \end{array} \qquad \begin{array}{l} \text{V}_{\text{IN}} = 3.4 \\ \text{V}_{\text{IN}} = \text{GN} \end{array}$ |
|        | en                                       |        | 3.0    |      | 16.5  |              | $\begin{array}{l} \text{(Note 5)} \\ \text{V}_{CC} = \text{Max} \\ \text{Outputs Open} \\ \text{f}_{CP} = 10 \text{ MHz} \\ \end{array}  \begin{array}{l} \text{V}_{IN} \geq \text{V}_{HC} \\ \text{V}_{IN} \leq 0.2 \text{V} \\ \text{Open} \end{array}$                                 |
| 2-10   | en                                       |        |        |      |       |              | 50% Duty Cycle CEAB + OEAB = GND CEBA = V <sub>CC</sub> . f <sub>CP</sub> = LEAB = 10 MHz   |
|        |  |        | 5.0    |      | 21.75 | balant fon h | Eight Bits Toggling at $f_1 = 5$ MHz $V_{IN} = 3.4$ $V_{IN} = GN$   |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (VIN = 3.4); all other inputs at VCC or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6:  $|_{C} = |_{QUIESCENT} + |_{INPUTS} + |_{DYNAMIC}$   $|_{C} = |_{CC} + \Delta|_{CC} D_{H}N_{T} + |_{CCD} (f_{CP}/2 + f_{I}N_{I})$   $|_{CC} = |_{Quiescent} Current$ 

 $\Delta I_{CC} =$  Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL Inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

| Symbol Parameter                     |   | $T_{A} = +25^{\circ}C$ $V_{CC} = 5.0V$ | $R_L = 500\Omega$<br>$C_L = 50 pF$ | R <sub>L</sub> = 500Ω<br>C <sub>L</sub> = 50 pF | Units | Fig. |
|--------------------------------------|---|--|------------------------------------|---|-------|------|
|                                      | Voc = Max   | Тур                                    | Min (Note 1) Max                   | Min Max   | Dyr   | cco  |
| tрцц ∨ ≤ ;;<br>tрнс 0 ≥ ;;           | Propagation Delay<br>Transparent Mode<br>A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub> | sHM\Am                                 | 1.5 35.0 7.0                       | (Note 4)  | ns    | 2-8  |
| tplH<br>tpHL<br>OMV ≤ ¥              | Propagation Delay  LEAB to An,  LEAB to Bn  |  | 1.5 8.0                            | al Power Supply<br>rent (Note 6)                | oT ns | 2-8  |
| <sup>t</sup> PZH<br><sup>t</sup> PZL | Output Enable Time OEBA or OEAB to An or Bn CEBA or CEAB to An or Bn  |  | 1.5 9                              |   | ns    | 2-11 |
| t <sub>PHZ</sub>                     | Output Disable Time  CEBA or OEAB to An or Bn  CEBA or OEAB to An or Bn                                       | Am                                     | 1.5 7.5                            |   | ns    | 2-11 |
| tsu<br>0HV ≤ 1/<br>VS.0 ≥ 1/         | Setup Time<br>High or Low<br>A <sub>n</sub> or B <sub>n</sub> to LEBA or LEAB                                 |  | 2 0.8                              |   | ns    | 2-10 |
| t <sub>H</sub>                       | Hold Time<br>High or Low<br>A <sub>n</sub> or B <sub>n</sub> to LEBA or LEAB                                  |  | 2                                  |   | ns    | 2-10 |

Note 1: Minimum propagation delays are guaranteed but not tested.

#### Capacitance T<sub>A</sub> = +25°C, f = 1.0 MHz

| Symbol           | Parameter (Note)   | Тур | Max | Units | Conditions            | ate 2: This perameter gueranteed but not vested.<br>ate 3: Per TTL driven Ingut (V <sub>IX</sub> = 3.4); ell atner Ingur |
|------------------|--------------------|-----|-----|-------|-----------------------|--|
| CIN              | Input Capacitance  | 6   | 10  | pF    | V <sub>IN</sub> = 0V  | ota 4: This parentator is not discotly testable, but in de-  |
| C <sub>OUT</sub> | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V | ose 5: Values for these conditions are examples of the ose 6: or louisscent + laurums + forexamic                        |

### 54FCT/74FCT563A Octal Latch with TRI-STATE® Outputs

#### **General Description**

The 'FCT563A is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable  $(\overline{OE})$  inputs.

The 'FCT563A device is functionally identical to the 'FCT573A, but with inverted outputs.

FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

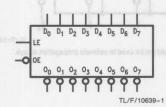
#### **Features**

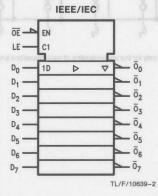
- Inputs and outputs on opposite side of package allow easy interface with microprocessors
- Useful as input or output port for microprocessors
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD-883
- Inherently radiation tolerant

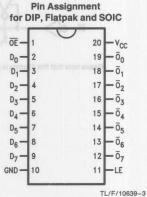
Ordering Code: See Section 8

**Logic Symbols** 

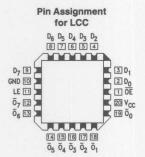
#### **Connection Diagrams**







| Pin Names                         | Description                   |  |  |  |
|-----------------------------------|-------------------------------|--|--|--|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                   |  |  |  |
| LE                                | Latch Enable Input            |  |  |  |
| ŌĒ                                | TRI-STATE Output Enable Input |  |  |  |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Latch Outputs       |  |  |  |



TL/F/10639-4

#### **Functional Description**

The 'FCT563A contains eight D-type latches with TRI-STATE complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D<sub>n</sub> inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable (OE) input. When OE is LOW, the buffers are in the TRI-STATE mode. When  $\overline{\text{OE}}$  is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

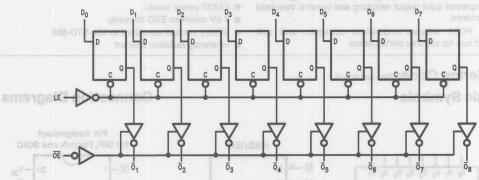
#### Function Table

|      |       | Inputs Outputs |     | Function    |             |
|------|-------|----------------|-----|-------------|-------------|
|      | OE LE |                | D   | 0           | a diletion  |
|      | Н     | X              | X   | Z           | High-Z      |
|      | L     | H              | OC! | H           | Transparent |
| 9 8  | L'S   | S &H TO        | H   | a wholesa ! | Transparent |
| 1000 | L     | TATE A         | X   | NC          | Latched     |

- H = HIGH Voltage Level
- L = LOW Voltage Level
- X = Immaterial
- X = High Impedance

### Logic Diagram Judho bes Jugal 20MOVETT IS

RECEN



TL/F/10639-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

#### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (VTFRM) 54FCTA -0.5V to +7.0V74FCTA -0.5V to +7.0VTemperature under Bias (TBIAS) -55°C to +125°C -65°C to +135°C 54FCTA Storage Temperature (TSTG) -55°C to +125°C 74FCTA 54FCTA 6 etc/ Va 8-65°C to +150°C Power Dissipation (PT) DC Output Current (IOUT) 120 mA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

### Recommended Operating Conditions

Supply Voltage (VCC) 4.5V to 5.5V 54FCTA 74FCTA 4.75V to 5.25V OV to VCC Input Voltage Output Voltage OV to Vcc Operating Temperature (TA) 54FCTA -55°C to +125°C 0°C to +70°C 74FCTA Junction Temperature (TJ) 175°C PDIP 140°C

#### **DC Characteristics for 'FCTA Family Devices**

Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$   $T_A=-55$ °C to +125°C,  $V_{HC}=V_{CC}-0.2V$ 

| Symbol          | Parameter                           | 54FCTA/74F                           | CTA                            | Units          | Co  | onditions  |
|-----------------|-------------------------------------|--------------------------------------|--------------------------------|----------------|---|--|
| Symbol          | Parameter gall                      | Min Typ                              | Max                            | Office         |   | manions  |
| V <sub>IH</sub> | Minimum High Level<br>Input Voltage | 2.0                                  | Am                             | ٧              |   |  |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     | Outputs Ope                          | 0.8                            | V 0,8          |   |  |
| I <sub>IH</sub> | Input High Current                  | LE = V <sub>GG</sub><br>ft = 2.5 MHz | 5.0<br>5.0                     | µА од          | V <sub>CC</sub> = Max   | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$        |
| I <sub>IL</sub> | Input Low Current                   | Elght Bits To<br>50% Duty Cy         | -5.0<br>-5.0                   | μА             | V <sub>CC</sub> = Max   | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND |
| loz             | Maximum TRI-STATE<br>Current        | verni eno re b                       | 10.0<br>10.0<br>-10.0<br>-10.0 | Au<br>Or GND.  | V <sub>CC</sub> = Max O #3000 m<br>m for fundaes for find the fu | $V_0 = 0.5V \text{ (Note 2)}$                          |
| VIK             | Clamp Diode Voltage                 | Betref for 1-0.7                     | -1.2                           | V              | $V_{CC} = Min; I_N = -18$   | 3 mA no asset to soule V st elok                       |
| los             | Short Circuit Current               | -60 -120                             |                                | mA             | V <sub>CC</sub> = Max (Note 1);   | Vo = GND   |
| VoH             | Minimum High Level                  | 2.8 3.0                              |                                |                | $V_{CC} = 3V; V_{IN} = 0.2V$  | $V$ or $V_{HC}$ ; $I_{OH} = -32 \mu\text{A}$           |
|                 | Output Voltage                      | V <sub>HC</sub> V <sub>CC</sub>      |                                |                |   | $I_{OH} = -300 \mu\text{A}$                            |
|                 |                                     | 2.4 4.3                              | UR                             | to HVI) the    | $V_{IN} = V_{IH} \text{ or } V_{IL}$  |  |
|                 |                                     | 2.4 4.3                              | taesiver                       | k ridalge/k-ni | Register Devices (Zero for Ni   | $I_{OH} = -15 \text{ mA (Com)}$                        |
| V <sub>OL</sub> | Maximum Low Level                   | GND                                  | 0.2                            | schering       | $V_{CC} = 3V; V_{IN} = 0.2V$  | $V$ or $V_{HC}$ ; $I_{OL} = 300 \mu A$                 |
|                 | Output Voltage                      | GND                                  | 0.2                            | V              | V <sub>CC</sub> = Min   | $I_{OL} = 300 \mu\text{A}$                             |
|                 |                                     | 0.3                                  | 0.50                           |                | $V_{IN} = V_{IH} \text{ or } V_{IL}$  | I <sub>OL</sub> = 32 mA (Mil)                          |
|                 |                                     | 0.3                                  | 0.50                           |                |   | I <sub>OL</sub> = 48 mA (Com)                          |

DC Characteristics for FCTA Family Devices (Continued) Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0 \text{V} \pm 5\%$ ,  $T_{A} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ; Mil:  $V_{CC} = 5.0 \text{V} \pm 10\%$   $T_{A} = -55^{\circ}\text{C}$ to +125°C,  $V_{HC} = V_{CC} - 0.2V$ 

| Symbol                  | Parameter                                 | 54FCTA/74FCTA | Units       | Cond   |  |
|-------------------------|---|---------------|-------------|--|--|
| ooV of V                | Parameter                                 | Min Typ Max   | V0.7 + of   | V8.0-  | 74FCTA   |
| O 125 C                 | Maximum Quiescent<br>Supply Current       | 0.001 1.5     | mA          | $V_{CC} = Max$ (AART) 8 $V_{IN} \ge V_{HC} \le 0.2V$ $f_I = 0$   | Temperature under Bia<br>74FCTA<br>64FCTA                                |
| ΔI <sub>CC</sub>        | Quiescent Supply Current;                 | 0.5 2.0       | mA          | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   | 74FCTA<br>54FCTA   |
| ICCD                    | Dynamic Power<br>Supply Current (Note 4)  | 0.25 0.45     | mA/MHz      | V <sub>CC</sub> = Max Outputs Open $\overline{OE}$ = GND LE = V <sub>CC</sub> One Input Toggling 50% Duty Cycle  | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$                                 |
| lc<br>eulev er<br>0°88- | Total Power<br>Supply Current (Note 6)    | 1.5 4.5       | beam bee to | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND  | $\begin{aligned} V_{IN} &\geq V_{HC} \\ V_{IN} &\leq 0.2V \end{aligned}$ |
|                         | Conditions                                | 1.8 5.0       | ATDYMY      | LE = V <sub>CC</sub> f <sub>I</sub> = 10 MHz One Bit Toggling 50% Duty Cycle   | $V_{IN} = 3.4V$ $V_{IN} = GND$   |
|                         |   | 3.0 8.0       | 10          | The second secon | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$                                    |
| te 2)                   |   | 5.0 Au 14.5   | 1.8<br>.8   | f <sub>I</sub> = 2.5 MHz   | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND                          |
| (S ef                   | $V_i = 0.5V$ (No Vi = 0.5V (No Vi = 0.5V) | S pA Voc =    | 8-<br>8-    | Eight Bits Toggling<br>50% Duty Cycle  | It Input Low C   |
| VH                      | Input Hysteresis on Clock Only            | 200           | mV          | STATELO  |  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6:  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$ 

I<sub>CC</sub> = Quiescent Current

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

DH = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

Logic Symbols

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                      |  | 54FCTA/74FCTA                                     |     | 74FCTA   | 54FCTA   | olma2    |             |
|--------------------------------------|--|---|-----|--|--|----------|-------------|
| Symbol Parameter                     | Parameter  | T <sub>A</sub> = 25°C<br>V <sub>CC</sub> = 5.0V   | R   | V <sub>CC</sub> = Com<br><sub>L</sub> = 500Ω<br><sub>L</sub> = 50 pF | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$           | Units    | Fig.<br>No. |
|                                      |  | Тур 💮 🗇   | Min | Max  | Min Max  | 7 O h    | eto O       |
| t <sub>PLH</sub>                     | Propagation Delay D <sub>n</sub> to O <sub>n</sub> | 4.0   | 1.5 | 5.2  | nolloisa   | ns       | 2-8         |
| t <sub>PLH</sub>                     | Propagation Delay LE to On                         | 7.0 TATE  | 2.0 | 10 8.5 late  | igh-speed, low power at<br>Clack (CP) and a bu                   | ns       | 2-8         |
| t <sub>PZL</sub><br>t <sub>PZH</sub> | Output Enable Time                                 | 5.5   | 1.5 | G edit of betre  | <ol> <li>The information presse flip flops on the LOW</li> </ol> | ns ns    | 2-11        |
| t <sub>PHZ</sub>                     | Output Disable Time                                | 4.0   | 1.5 | edi o 5.5 mo   | vice is functionally id  | b ns351  | 2-11        |
| ts                                   | Set Up Tme<br>High or Low<br>D <sub>n</sub> to LE  | f ineliquos subora yu<br>inerelo) notelber yitner | 2.0 |  | es NSC quiet series ted<br>output switching and dy               |          | 2-10        |
| t <sub>H</sub>                       | Hold Time<br>High or Low<br>D <sub>n</sub> to LE   | 1.0   | 1.5 | Rige bas noits   | res undernincot corre-<br>rior performance:                      | deat ATO | 2-10        |
| t <sub>W</sub>                       | LE Pulse Width<br>High or Low                      | 4.0   | 5.0 |  | do: See Section 8  | ns       | 2-9         |

Minimum limits are guaranteed but not tested on propagation delays.

#### Capacitance TA = +25°C, f = 1.0 MHz

| Symbol | Parameter          | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.

00[3]



## 54FCT/74FCT564A Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'FCT564A is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable (OE). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'FCT564A device is functionally identical to the 'FCT574A, but with inverted outputs.

FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

#### **Features**

- TRI-STATE outputs for bus-oriented applications
- Useful as input or output port for microprocessors
- Input clamp diodes to limit bus reflections

Electrical Citaracteristics: See Section 2 for Wayelorms

- TTL/CMOS input and output level compatible
- I<sub>OI</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD-883
- Inherently radiation tolerant

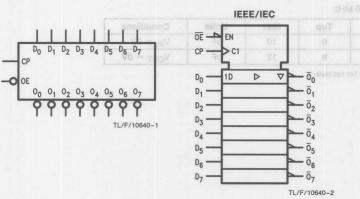
Ordering Code: See Section 8

**Logic Symbols** 

#### **Connection Diagrams**

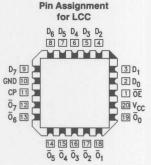
Pin Assignment

Symbol



| 2 million          |                     |
|--------------------|---------------------|
| OE 1               | 20 -V <sub>CC</sub> |
| D <sub>0</sub> - 2 | 19 - 00             |
| D <sub>1</sub> -3  | 18 — Ō <sub>1</sub> |
| D <sub>2</sub> - 4 | 17 — Ō <sub>2</sub> |
| D <sub>3</sub> — 5 | 16 — Ō <sub>3</sub> |
| D <sub>4</sub> — 6 | 15 — Ō <sub>4</sub> |
| D <sub>5</sub> — 7 | 14 — Ō <sub>5</sub> |
| D <sub>6</sub> — 8 | 13 — Ō <sub>6</sub> |
| D <sub>7</sub> 9   | 12 - 07             |
| ND - 10            | 11 — CP             |

| Pin Names                         | Description                   |
|-----------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs                   |
| CP                                | Clock Pulse Input             |
| ŌĒ                                | TRI-STATE Output Enable Input |
| $\overline{O}_0 - \overline{O}_7$ | TRI-STATE Outputs             |



TL/F/10640-4

#### Absolute Maximum Rating (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Terminal Voltage with respect to GND (<br>54FCTA<br>74FCTA      | (V <sub>TERM</sub> )<br>-0.5V to 7.0V<br>-0.5 to 7.0V |
|---|---|
| Temperature Under Bias (T <sub>BIAS</sub> )<br>74FCTA<br>54FCTA | -55°C to +125°C<br>-65°C to +135°C                    |
| Storage Temperature (T <sub>STG</sub> )<br>74FCTA<br>54FCTA     | -55°C to +125°C<br>-65°C to +150°C                    |
| Power Dissipation (P <sub>T</sub> )                             | 0.5w  |
| DC Output Current (I <sub>OUT</sub> )                           | 120 mA  |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACTTM FCT circuits outside databook specifications.

### Recommended Operating Conditions

| Supply Voltage (V <sub>CC</sub> )           | VSC - 0.2V  | , |
|---|---|---|
| 54FCTA<br>74FCTA                            | 4.5V to 5.5V<br>4.75V to 5.25V                      |   |
| Input Voltage                               | 0V to V <sub>CC</sub>                               |   |
| Output Voltage                              | OV to V <sub>CC</sub>                               | 5 |
| Operating Temperature (<br>54FCTA<br>74FCTA | T <sub>A</sub> )<br>-55°C to +125°C<br>0°C to +70°C |   |
| Junction Temperature (T, CDIP               | MOH atugal JTT 175°C                                |   |
| PDIP  | 140°C   | 3 |
|   |   |   |

#### **DC Characteristics for 'FCTA Family Devices**

Typical values are at V<sub>CC</sub> 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com: V<sub>CC</sub> 5.0V +5%,  $T_A = 0$ °C to +70°; Mil: V<sub>CC</sub> = 5.0V  $\pm 10$ %  $T_A = 55$ °C +125°C V<sub>HC</sub> = V<sub>CC</sub> -0.2V

| Symbol          | Parameter                           | 54                      | FCTA/74F                      | CTA                            | Units        | C   | onditions   |
|-----------------|-------------------------------------|-------------------------|-------------------------------|--------------------------------|--------------|---|---|
| Cymbol          | raiameter                           | Min                     | Тур                           | Max                            | Omics        |   | onditions .   |
| VIH             | Minimum High Level<br>Input Voltage | 2.0                     |                               | 7.8                            | o.V          |   |   |
| V <sub>IL</sub> | Maximum Low Level Input Voltage     | 30<br>40 <sup>†</sup>   |                               | 0.8                            | ٧            |   |   |
| IHAD = N        | Input High Current                  | = 11<br>= 11            |                               | 5.0<br>5.0                     | μА           | V <sub>CC</sub> = Max                               | $V_I = V_{CC}$<br>$V_I = 2.7V \text{ (Note 2)}$   |
| I <sub>IL</sub> | Input Low Current                   | 500                     |                               | -5.0<br>-5.0                   | μА           | V <sub>CC</sub> = Max                               | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND  |
| loz             | Maximum TRI-STATE<br>Current        |                         | VRN<br>emit sno ta b          | 10.0<br>10.0<br>-10.0<br>-10.0 | μ <b>A</b>   | V <sub>CC</sub> = Max                               | $V_{O} = V_{CC}$ $V_{O} = 2.7V \text{ (Note 2)}$ $V_{O} = 0.5V \text{ (Note 2)}$ $V_{O} = \text{GND}$         |
| VIK             | Clamp Diode Voltage                 | bufasti                 | -0.7                          | -1.2                           | V            | $V_{CC} = Min; I_N = -1$                            | 8 mA  |
| los             | Short Circuit Current               | -60                     | -120                          |                                | mA           | V <sub>CC</sub> = Max (Note 1);                     | V <sub>O</sub> = GND  |
| V <sub>OH</sub> | Minimum High Level                  | 2.8                     | 3.0                           |                                |              | $V_{CC} = 3V; V_{IN} = 0.2$                         | V or $V_{HC}$ ; $I_{OH} = -32 \mu A$  |
|                 | Output Voltage                      | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                | ٧            |   | $I_{OH} = -300 \mu\text{A}$<br>$I_{OH} = -12 \text{mA} (\text{Mil})$<br>$I_{OH} = -15 \text{mA} (\text{Com})$ |
| V <sub>OL</sub> | Maximum Low Level                   |                         | GND                           | 0.2                            | to MUH) tist | $V_{CC} = 3V; V_{IN} = 0.2$                         | V or $V_{HC}$ ; $I_{OL} = 300 \mu A$  |
|                 | Output Voltage                      |                         | GND<br>0.3<br>0.3             | 0.2<br>0.50<br>0.50            | ٧            | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = 300 \mu\text{A}$ $I_{OL} = 32 \text{mA} (\text{Mil})$ $I_{OL} = 48 \text{mA} (\text{Com})$          |

| Symbol    | Paramet  | er                              | 54                   | FCTA/74                                   | FCTA                                    | Units   | Conditions  | Terminal Volta  |
|-----------|--|---------------------------------|----------------------|---|---|---|---|---|
| ooV of VI |  |                                 | Min                  | Тур                                       | Max                                     | -0.510  |   | TAFOTA  |
| lcc       | Maximum Quiesce<br>Supply Current  | nt<br>(AT) enutsied             | ollage<br>g Tem<br>A | 0.001                                     | 1.5                                     | 1 + cmA 22 -                                    | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.2V$ $f_I = 0$   |   |
| Δlcc      | Quiescent Supply<br>TTL Inputs HIGH  | Current;                        | eqmeT                | 0.5                                       | 2.0                                     | r + cmA   | V <sub>CC</sub> = Max V <sub>IN</sub> = 3.4V (Note 3)   | Storage Temp<br>74FCTA<br>848CTA  |
| ICCD      | Dynamic Power<br>Supply Current (No  | ote 4)                          |                      | 0.25                                      | 0.40                                    | mA/MHz  | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND<br>One Input Toggling<br>50% Duty Cycle   | V <sub>IN</sub> ≥ V <sub>HC</sub><br>V <sub>IN</sub> ≤ 0.2V   |
| lc        | Total Power  |                                 |                      | 4.5                                       | 4.0                                     | sons dees not a<br>sbook specification          | V <sub>CC</sub> = Max   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$  |
|           | Supply Current (No   | ote 6)                          |                      | 1.5                                       | 4.0                                     | DTA Fau   | Outputs Open  OE = GND  | VIN 2 0.2V  |
|           | Supply Current (No<br>eulay ent seu ,xelf a<br>r3st + 0*35 = AT &  | is nworfe anoil                 |                      |   |   | CTA Fan<br>ient and mee<br>; 5.0V + 5%,         | $\overline{OE} = GND$<br>$f_{CP} = 10 \text{ MHZ}$<br>$f_{I} = 5 \text{ MHz}$<br>50% Duty Cycle   | V <sub>IN</sub> = 3.4\  |
|           | a Max, use the value   | se nworte ancil<br>eor ± vo.a = |                      |   | e O ylia<br>bed mun<br>6.0              | CTA Fair ient and mexi s.OV + 5.% EMPCTA/745 Am | $\overline{OE} = GND$<br>$f_{CP} = 10 \text{ MHZ}$<br>$f_{I} = 5 \text{ MHz}$   | V <sub>IN</sub> = 3.4\<br>V <sub>IN</sub> = GNI   |
|           | Mex, use the value & TABP  | se nworte ancil<br>eor ± vo.a = |                      | ng Fortes<br>to +70°; to<br>8.1           | ed ylin<br>ibed mun<br>1000 = A1<br>6.0 |   | OE = GND<br>f <sub>CP</sub> = 10 MHZ<br>f <sub>I</sub> = 5 MHz<br>50% Duty Cycle<br>One Bit Toggling  | $V_{IN} = 3.4$<br>$V_{IN} = GNI$<br>$V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2$   |
|           | Mex, use the value & TABP  | se nworte ancil<br>eor ± vo.a = |                      | ryices<br>ng Fortes<br>to +70°; to<br>1.8 | 6.0                                     |   | OE = GND<br>f <sub>CP</sub> = 10 MHZ<br>f <sub>I</sub> = 5 MHz<br>50% Duty Cycle<br>One Bit Toggling<br>50% Duty Cycle<br>(Note 5)<br>V <sub>CC</sub> = Max   | $\begin{aligned} & V_{IN} = 3.44 \\ & V_{IN} = GNI \\ \end{aligned}$ $\begin{aligned} & V_{IN} \geq V_{HC} \\ & V_{IN} \leq 0.2V \end{aligned}$   |
| = DHV O   | Mex, use the value & TABP  | as nworte anoil<br>ear ± vo.8 = |                      | 1.8                                       | 6.0                                     |   | OE = GND  f <sub>CP</sub> = 10 MHZ f <sub>I</sub> = 5 MHz 50% Duty Cycle One Bit Toggling 50% Duty Cycle  (Note 5) V <sub>CC</sub> = Max Outputs Open OE = GND f <sub>CP</sub> = 10 MHz 50% Duty Cycle f <sub>I</sub> = 2.5 MHz | $V_{IN} = 3.4V$ $V_{IN} = GNI$ $V_{IN} \ge V_{HC}$  |
| C VHC =   | Max, use the value of the value of the transfer of the transfe | as nworte anoil<br>ear ± vo.8 = | lii: Voc             | 3.0                                       | 6.0                                     |   | OE = GND  f <sub>CP</sub> = 10 MHZ  f <sub>I</sub> = 5 MHz  50% Duty Cycle  One Bit Toggling  50% Duty Cycle  (Note 5)  V <sub>CC</sub> = Max  Outputs Open  OE = GND  f <sub>CP</sub> = 10 MHz  50% Duty Cycle                 | $\begin{aligned} &V_{IN} = 3.4 V \\ &V_{IN} = GNI \\ &V_{IN} \geq V_{HC} \\ &V_{IN} \leq 0.2 V \\ &V_{IN} = 3.4 V \\ &V_{IN} = GNI \end{aligned}$ |

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>

 $I_{C} = I_{CC} + \Delta I_{CC} D_{H} N_{T} + I_{CCD} (f_{CP}/2 + f_{J} N_{J})$ 

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

| Symbol                                    | Parameter                                | V <sub>CC</sub> = 5.0V  | and the same | L = 500Ω<br>L = 50 pF | R <sub>L</sub> = C <sub>L</sub> = | 500Ω<br>50 pF                  | Units | No.   |
|---|--|---|--------------|-----------------------|-----------------------------------|--------------------------------|-------|-------|
|   |  | Тур   | Min          | (Note) Max            | Min                               | Max                            | s.lle | JoC ! |
| t <sub>PLH</sub><br>t <sub>PHL</sub>      | Propagation Delay CP to $\overline{O}_n$ | 4.5   | 2.0          | 6.5                   |                                   | oltohoa                        | ns    | 2-8   |
| t <sub>PZH</sub> meta<br>t <sub>PZL</sub> | Output Enable Date Time                  | SA/7AFCTS73A is pin   | 1.5          | 6.5                   | t octal latch i<br>i bultered con | a high-speed<br>nable (LE) and | ns    | 2-11  |
| t <sub>PHZ</sub>                          | Output Disable<br>Timed                  | oxiqo no siudico una<br>oxim div 4.0 chem ya                            | 1.5          | and A(5.5)            | entroal to the                    | g<br>functionally ide          | a ns  | 2-11  |
| ts  | High or Low                              | 48 mA (Com), 32 mA<br>TATE out,0.1s for bus i<br>y product compliant to | 2.0          |                       |                                   |                                | ns    | 2-10  |
| tн  | HOLD Time                                | igus and output level o<br>ipus acc 0.1 CMOS lev                        | 1.5          |                       |                                   |                                | ns    | 2-10  |
| t <sub>W</sub>                            | CP Pulse Width<br>High or Low            | 4.0   | 5.0          |                       | lection 8                         | oes tebul                      | ns    | 2-9   |

#### Capacitance ( $T_A = +25^{\circ}C$ , f = 1.0 MHz)

| Symbol | Parameter          | Тур | Max | Units | Conditions            |
|--------|--------------------|-----|-----|-------|-----------------------|
| CIN    | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| Cout   | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Note: This parameter is measured at characterization but not tested.



# 54FCT/74FCT573A Octal Latch with TRI-STATE® Outputs

#### **General Description**

The 'FCT573A is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs.

The 'FCT573A is functionally identical to the 'FCT373A but has inputs and outputs on opposite sides.

#### **Features**

- NSC 54/74FCT573A is pin and functionally equivalent to IDT 54/74FCT573A
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors

AC Electrical Characteristics: See Section 2 for Waveforms

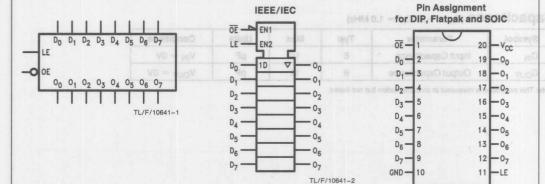
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- TRI-STATE outputs for bus interfacing
- Military product compliant to MIL-STD-883
- TTL input and output level compatible
- TTL inputs accept CMOS levels

Ordering Code: See Section 8

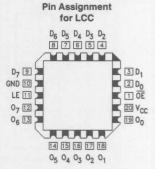
#### **Logic Symbols**

#### **Connection Diagrams**

Symbol



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| LE                             | Latch Enable Input            |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Latch Outputs       |



TL/F/10641-4

TL/F/10641-3

#### Functional Description

The FCT573A contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the  $D_{\rm n}$  inputs enters the latches. In this condition the latches are transparent, and the latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ( $\overline{\rm OE}$ ) input. When  $\overline{\rm OE}$  is LOW, the latch contents are presented inverted at the outputs  $\overline{\rm O}_7-\overline{\rm O}_0$ . When  $\overline{\rm OE}$  is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

#### Truth Table Ital mumixsM etuloadA

|              | Outputs         |               |                  |
|--------------|-----------------|---------------|------------------|
| OE           | loege ILE: yill | telfaup sot a | rotudir On \e    |
| L            | GNH (VTERM      | th Repeat to  | w ngstle H lank  |
| VO.Y - OF VA | Н               | L             | L <sub>TOS</sub> |
| L            | L               | X             | 00               |
| Н            | X               | X             | Z Z              |

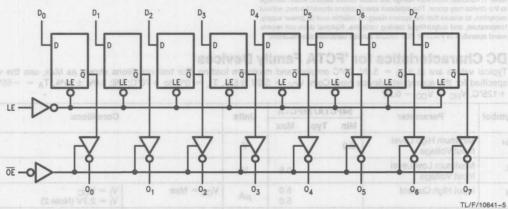
H = HIGH Voltage

L = LOW Voltage Z = High Impedance

X = Immaterial

O<sub>0</sub> = Previous O<sub>0</sub> before HIGH-to-LOW transition of Latch Enable

#### **Logic Diagram**



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| Terminal Voltage with Respect to Gi<br>54FCTA<br>74FCTA<br>Temperature under Bias (T <sub>BIAS</sub> )<br>54FCTA<br>74FCTA<br>Storage Temperature (T <sub>STG</sub> ) | -0.5V to +7.0V<br>-0.5V to +7.0V<br>-65°C to +135°C<br>-55°C to +125°C | 74FCTA 4.75V to 5.25V Input Voltage 0V to V <sub>CC</sub> Output Voltage 0V to V <sub>CC</sub> Operating Temperature (T <sub>A</sub> ) 54FCTA -55°C to +125°C 74FCTA 0°C to +70°C |
|---|--|---|
| 54FCTA  | -65°C to +150°C<br>-55°C to +125°C                                     | Junction Temperature (T <sub>J</sub> ) CDIP 175°C   |
| Power Dissipation (P <sub>T</sub> )   | 0.5W   | PDIP 140°C  |
| DC Ouput Current (IOUT)   | 120 mA   |   |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ FCT circuits outside databook specifications.

DC Characteristics for 'FCTA Family Devices Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to  $\pm70$ °C; Mil:  $5.0V\pm10\%$ ,  $T_A=-55$ °C to  $\pm125$ °C,  $V_{HC}=V_{CC}-0.2V$ 

| Symbol           | Parameter                                    | 54F             | CTA/74            | FCTA                           | Units  |  | Conditions   |  |
|------------------|--|-----------------|-------------------|--------------------------------|--------|--|--|--|
| Oymbor           | ranameter                                    | Min             | Тур               | Max                            | Ointo  | - Constitution   |  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0             | V                 |                                | V      | V V V  |  |  |
| V <sub>IL</sub>  | Maximum Low Level Input Voltage              |                 |                   | 0.8                            | V      | 71-71  | Jo- 50   |  |
| IH<br>&=rsaoi    | Input High Current                           | 0               | 10                | 5.0<br>5.0                     | μΑ     | V <sub>CC</sub> = Max  | $V_I = V_{CC}$<br>$V_I = 2.7V$ (Note 2)  |  |
| I <sub>IL</sub>  | Input Low Current                            | nau ed to       | in bluoria i      | -5.0<br>-5.0                   | μА     | V <sub>CC</sub> = Max  | V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND   |  |
| loz              | Maximum TRI-STATE<br>Current                 |                 |                   | 10.0<br>10.0<br>-10.0<br>-10.0 | μΑ     | V <sub>CC</sub> = Max  | V <sub>O</sub> = V <sub>CC</sub><br>V <sub>O</sub> = 2.7V (Note 2)<br>V <sub>O</sub> = 0.5V (Note 2)<br>V <sub>O</sub> = GND |  |
| VIK              | Clamp Doide Voltage                          |                 | -0.7              | -1.2                           | V      | $V_{CC} = Min; I_N = -18 \text{ mA}$   |  |  |
| los              | Short Circuit Current                        | -60             | -120              |                                | mA     | V <sub>CC</sub> = Max (Note 1); V <sub>O</sub> = GND   |  |  |
| V <sub>OH</sub>  | Minimum High Level                           | 2.8             | 3.0               |                                |        | $V_{CC} = 3V$ ; $V_{IN} = 0.2V$ or $V_{HC}$ ; $I_{OH} = -32 \mu A$                                   |  |  |
|                  | Output Voltage                               | V <sub>HC</sub> | Vcc               | Total !                        | V      | V <sub>CC</sub> = Min  | $I_{OH} = -300 \mu\text{A}$  |  |
|                  |  | 2.4             | 4.3               |                                |        | $V_{IN} = V_{IH} \text{ or } V_{IL}$   | $I_{OH} = -12 \text{ mA (Mil)}$  |  |
|                  |  | 2.4             | 4.3               |                                |        |  | $I_{OH} = -15 \text{ mA (Com)}$  |  |
| VOL              | Maximum Low Level                            |                 | GND               | 0.2                            |        | $V_{CC} = 3V; V_{IN} = 0.2$  | V or $V_{HC}$ ; $I_{OL} = 300 \mu A$   |  |
|                  | Output Voltage                               |                 | GND<br>0.3<br>0.3 | 0.2<br>0.50<br>0.50            | V      | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OL} = 300 \mu A$<br>$I_{OL} = 32 \text{ mA (Mil)}$<br>$I_{OL} = 48 \text{ mA (Com)}$                                     |  |
| Icc              | Maximum Quiescent<br>Supply Current          |                 | 0.001             | 1.5                            | mA     | $\begin{array}{l} V_{CC} = \text{Max} \\ V_{IN} \geq V_{HC}, V_{IN} \leq 0.2 \\ f_I = 0 \end{array}$ | V  |  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                 | 0.5               | 2.0                            | mA     | $V_{CC} = Max$<br>$V_{IN} = 3.4V \text{ (Note 3)}$   |  |  |
| ICCD             | Dynamic Power<br>Supply Current (Note 4)     |                 | 0.25              | 0.45                           | mA/MHz | $V_{CC} = Max$ Outputs Open One Input Toggling 50% Duty Cycle $\overline{OE} = GND$ $LE = V_{CC}$    | $\begin{array}{c} V_{IN} \geq V_{HC} \\ V_{IN} \leq 0.2V \end{array}$  |  |

| Symbol                                | Parameter                              | 54FCTA/74FCTA |     | Units | Conditions |  |   |  |
|---------------------------------------|--|---------------|-----|-------|------------|--|---|--|
| Symbol                                | rarameter                              | Min           | Тур | Max   | Omio       | based for Jud nollemabases   | to homeson at submission and totals                                   |  |
| Total Power<br>Supply Current (Note 6 | Total Power<br>Supply Current (Note 6) |               | 1.5 | 4.5   | mA.        | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND, LE = V <sub>CC</sub>      | $\begin{array}{c} V_{IN} \geq V_{HC} \\ V_{IN} \leq 0.2V \end{array}$ |  |
|                                       |  |               | 1.8 | 5.0   |            | f <sub>CP</sub> = 10 MHz<br>One Bit Toggling<br>50% Duty Cycle               | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND                       |  |
|                                       |  |               | 3.0 | 8.0   | mA         | (Note 5)  V <sub>CC</sub> = Max Outputs Open  OE = GND, LE = V <sub>CC</sub> | $\begin{array}{c} V_{IN} \geq V_{HC} \\ V_{IN} \leq 0.2V \end{array}$ |  |
|                                       |  |               | 5.0 | 14.5  |            | f <sub>CP</sub> = 2.5 MHz<br>Eight Bits Toggling<br>50% Duty Cycle           | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GND                       |  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

 $\begin{aligned} \textbf{Note 6: } & \textbf{I}_{\text{C}} = \textbf{I}_{\text{QUIESCENT}} + \textbf{I}_{\text{INPUTS}} + \textbf{I}_{\text{DYNAMIC}} \\ & \textbf{I}_{\text{C}} = \textbf{I}_{\text{CC}} + \Delta \textbf{I}_{\text{CC}} \, \textbf{D}_{\text{HNT}} + \textbf{I}_{\text{CCD}} \, (\textbf{f}_{\text{CP}}/2 \, + \, \textbf{f}_{\text{I}} \textbf{N}_{\text{I}}) \\ & \textbf{I}_{\text{CC}} = \text{Quiescent Current} \end{aligned}$ 

 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

#### AC Electrical Characteristics: See Section 2 for Waveforms

|                                      |   | 54/74FCTA                            | 74F              | CTA                    | 54F  | CTA |       |             |
|--------------------------------------|---|--------------------------------------|------------------|------------------------|--|-----|-------|-------------|
| Symbol                               | Parameter   | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$ | R <sub>L</sub> = | = Com<br>500Ω<br>50 pF | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$ |     | Units | Fig.<br>No. |
|                                      |   | Тур                                  | Min              | Max                    | Min  | Max |       |             |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay<br>D <sub>n</sub> to O <sub>n</sub> | 4.0                                  | 1.5              | 5.2                    |  |     | ns    | 2-8         |
| t <sub>PLH</sub>                     | Propagation Delay<br>LE to O <sub>n</sub>             | 7.0                                  | 2.0              | 8.5                    |  |     | ns    | 2-8         |
| t <sub>PZH</sub>                     | Output Enable Time                                    | 5.5                                  | 1.5              | 6.5                    |  |     | ns    | 2-11        |
| t <sub>PHZ</sub>                     | Output Disable Time                                   | 4.0                                  | 1.5              | 5.5                    |  |     | ns    | 2-11        |
| ts                                   | Setup Time High or<br>Low, D <sub>n</sub> to LE       | 1.0                                  | 2.0              |                        |  |     | ns    | 2-10        |
| t <sub>H</sub>                       | Hold Time High or<br>Low, D <sub>n</sub> to LE        | 1.0                                  | 1.5              |                        |  |     | ns    | 2-10        |
| t <sub>W</sub>                       | LE Pulse Width<br>High or Low                         | 4.0                                  | 5.0              |                        |  |     | ns    | 2-9         |

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

#### Capacitance (T<sub>A</sub> = +25°C, f = 1.0 MHz) 2001/VIII ATOF TO BOTTON BOTTON DO

| Symbol          | Parameter          | Тур | Max | Units | Conditions            |
|-----------------|--------------------|-----|-----|-------|-----------------------|
| C <sub>IN</sub> | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| COUT            | Output Capacitance | 8   | 10  | pF    | V <sub>OUT</sub> = 0V |

| COUT             | Output G             | apacitance          | 8             | 10 | pi  | 2.3.384 | VOUT | L = OA |  |
|------------------|----------------------|---------------------|---------------|----|-----|---------|------|--------|--|
| Note: This param | neter is measured at | characterization bu | t not tested. |    | Mak | dist    | DIM  |        |  |
|                  |                      |                     |               |    |     |         |      |        |  |
|                  |                      |                     |               |    |     |         |      |        |  |
|                  |                      |                     |               |    |     |         |      |        |  |
|                  |                      |                     |               |    |     |         |      |        |  |

AC Flectrical Characteristics: see section 2 for Waveforms



## 54FCT/74FCT574A Octal D Flip-Flop with TRI-STATE® Outputs

#### **General Description**

The 'FCT574A is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable  $(\overline{\text{OE}})$ . The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'FCT574A is functionally identical to the 'FCT374A except for the pinouts.

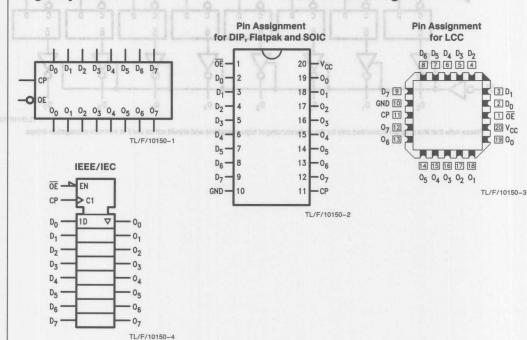
#### **Features**

- NSC 54/74FCT574A is pin and functionally equivalent to IDT54/74FCT574A
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'FCT374A
- TRI-STATE outputs for bus-oriented applications
- 'FCT574A has TTL-compatible inputs
- I<sub>OL</sub> = 48 mA (Comm) and 32 mA (Mil)
- TTL inputs accept CMOS levels

Ordering Code: See Section 8

**Logic Symbols** 

#### **Connection Diagrams**



| Pin Names                      | Description                   |
|--------------------------------|-------------------------------|
| D <sub>0</sub> -D <sub>7</sub> | Data Inputs                   |
| CP                             | Clock Pulse Input             |
| ŌĒ                             | TRI-STATE Output Enable Input |
| 00-07                          | TRI-STATE Outputs             |

M

requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable (OE) LOW, the contents of the eight flip-flops are available at the outputs. When OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

| H | H | .L     | NC         | Z         | Hold              |
|---|---|--------|------------|-----------|-------------------|
| H | Н | Н      | NC         | Z         | Hold              |
| Н | 5 | L      | L          | Z         | Load              |
| Н | _ | Н      | Н          | Z         | Load              |
| L | 1 | 36Fade | sed, jow p | a high-sp | Data Available    |
| L | 5 | H      | H          | Н         | Data Available    |
| L | Н | L      | NC         | NC        | No Change in Data |
| L | Н | Н      | NC         | NC        | No Change in Data |

H = HIGH Voltage Level

L = LOW Voltage Level

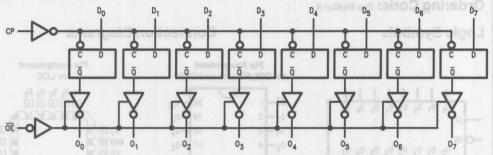
X = Immaterial

Z = High Impedance

= LOW-to-HIGH Transition

NC = No Change

#### **Logic Diagram**



TL/F/10150-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

 Pin Names
 Description

 Do-Dy
 Date inputs

 CP
 Clock Puts Input

 OE
 TRI-STATE Output Enable input

 Ob-Oy
 TRI-STATE Outputs

| Cilico, Diolinatoro for availability a  | ila apecilicationa.   | 54FCTA                     | 4             | .5V to 5.5V           |
|---|---|----------------------------|---------------|-----------------------|
| Terminal Voltage with Respect to GNI  | 54FCTA  -0.5V to +7.0V -0.5V to +7.0V -0.5V to +7.0V -0.5V to +7.0V -0.5C to +125°C -65°C to +125°C -65°C to +125°C -65°C to +125°C -65°C to +150°C -65°C to +125°C |                            |               |                       |
| 54FCTA<br>74FCTA  |   | Input Voltage              | 1949191871874 | OV to V <sub>CC</sub> |
| Temperature under Bias (T <sub>BIAS</sub> ) 74FCTA 54FCTA   | -55°C to +125°C   | Operating Temper<br>54FCTA | _55°C         | to +125°C             |
| Storage Temperature (T <sub>STG</sub> ) 74FCTA 54FCTA   |   | 2.0                        |               |                       |
| Power Dissipation (P <sub>T</sub> ) DC Output Current (I <sub>OUT</sub> ) Note 1: Absolute maximum ratings are those val to the device may occur. The databook specificat exception, to ensure that the system design is rel temperature, and output/input loading variables. | 120 mA<br>ues beyond which damage<br>ions should be met, without<br>lable over its power supply,<br>National does not recom-  | PDIP                       |               |                       |
| mend operation of FACT FCT circuits outside da  | tabook specifications.  |                            |               |                       |

**DC Characteristics for 'FCTA Family Devices** Typical values are at  $V_{CC}=5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0$ °C to +70°C; Mil:  $V_{CC}=5.0V\pm10\%$ ,  $T_A=-55$ °C to +125°C,  $V_{HC}=V_{CC}-0.2V$ 

| Symbol                      | Parameter A grade                    | 54       | FCTA/74F                     | CTA                            | Units                        | Co  | onditions   |
|-----------------------------|--------------------------------------|----------|------------------------------|--------------------------------|------------------------------|---|---|
| OHV ≤                       | cc = Max V <sub>I</sub>              | Min      | Тур                          | Max                            | 0.0                          |   | on a second   |
| V <sub>IH</sub> 2           | Minimum High Level<br>Input Voltage  | 2.0      |                              |                                | V                            |   |   |
| V <sub>IL</sub><br>VA.S = 1 | Maximum Low Level Input Voltage      | Ž<br>Ž   |                              | 0.8                            | V<br>5.0                     |   |   |
| I <sub>IH</sub>             | Input High Current                   |          | wit orn is h                 | 5.0<br>5.0                     | μΑ                           | V <sub>CC</sub> = Max                               | $V_I = V_{CC}$ $V_I = 2.7V \text{ (Note 2)}$  |
| I <sub>IL</sub>             | Input Low Current                    |          |                              | -5.0<br>-5.0                   | μΑ                           | V <sub>CC</sub> = Max                               | $V_I = 0.5V \text{ (Note 2)}$<br>$V_I = \text{GND}$   |
| loz                         | Maximum TRI-STATE<br>Current         | beisel h | anoits/uplac<br>on aud besin | 10.0<br>10.0<br>-10.0<br>-10.0 | μA                           | V <sub>CC</sub> = Max Mayor Cool                    | $V_0 = 2.7V \text{ (Note 2)}$   |
| V <sub>IK</sub>             | Clamp Diode Voltage                  |          | -0.7                         | -1.2                           | V8 =                         | $V_{CC} = Min; I_N = -18$                           | B mA and temps = colA   |
| los                         | Short Circuit Current                | -60      | -120                         |                                | mA                           | V <sub>CC</sub> = Max (Note 1);                     | $V_O = GND$   |
| V <sub>OH</sub>             | Minimum High Level<br>Output Voltage |          | 2.8<br>V <sub>HC</sub>       | 3.0<br>V <sub>CC</sub>         | air (HLH) de<br>n-Register D | Hagean Devides (Yako 10) Mil                        | V or V <sub>HC</sub> ; $I_{OH} = -32 \mu A$ $I_{OH} = -300 \mu A$   |
|                             |                                      |          | 2.4                          | 4.3<br>4.3                     | V                            | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -300 \mu\text{A}$<br>$I_{OH} = -12 \text{mA} \text{(Mil)}$<br>$I_{OH} = -15 \text{mA} \text{(Com)}$ |
| V <sub>OL</sub>             | Maximum Low Level                    |          | GND                          | 0.2                            |                              | $V_{CC} = 3V; V_{IN} = 0.2$                         | V or $V_{HC}$ ; $I_{OL} = 300 \mu A$  |
|                             | Output Voltage                       |          | GND<br>0.3<br>0.3            | 0.2<br>0.5<br>0.5              | V                            | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 300 \mu A$ $I_{OL} = 32 \text{ mA (Mil)}$ $I_{OL} = 48 \text{ mA (Com)}$                            |

DC Characteristics for 'FCTA Family Devices Typical values are at  $V_{CC} = 5.0V$ , 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC} = 5.0V \pm 10\%$ ,  $T_A = -55^{\circ}C$ to  $+125^{\circ}$ C,  $V_{HC} = V_{CC} - 0.2V$  (Continued)

| Symbol                  | Parameter  | 54FCTA/7                            | 4FCTA               | Units                          | Condition   | Terminal Volta<br>SAFOTA 81                     |
|-------------------------|--|-------------------------------------|---------------------|--------------------------------|---|---|
| OV to Voc               | T didiliotoi   | Min Typ                             | Max                 | - 01 Vã.0                      | Containo  | 74FCTA  |
| 0 + 128°C<br>10 + 128°C | Maximum Quiescent<br>Supply Current                        | 00.0 sing Tempe<br>54FCTA<br>74FCTA | 1 1.5 <sub>03</sub> | + of <b>mA</b> d — + of O'68 — | $V_{CC} = Max$ $V_{IN} \ge V_{HC}, V_{IN} \le 0.20$ $f_I = 0$                             | ATOHAG  |
| 20I∆                    | Quiescent Supply Current; TTL Inputs HIGH                  | negrasT ncit 0.5                    | 2.0                 | mA                             | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)                                  |   |
| ICCD                    | Dynamic Power<br>Supply Current (Note 4)                   | 0.15                                | 0.25                | mA/MHz                         | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND<br>One Input Toggling<br>50% Duty Cycle | $V_{IN} \ge V_{HC}$ $V_{IN} \le 0.2V$           |
| lc                      | Total Power<br>Supply Current (Note 6)                     | 1.5<br>890                          |                     | FCTA Fai                       | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        |
|                         | conditions shown as Max, use PC; Milit Voc = 5.0V ±10%, TA |                                     |                     | c Som: Voc =                   | f <sub>I</sub> = 5.0 MHz One Bit Toggling 50% Duty Cycle                                  | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GNE |
|                         | Conditions   | Units                               |                     | AT\AMA                         | (Note 5)  | lodniy  |
|                         |  | 3.0<br>V                            | 7.8                 | qyT ni                         | V <sub>CC</sub> = Max<br>Outputs Open<br>OE = GND   | $V_{IN} \ge V_{HC}$<br>$V_{IN} \le 0.2V$        |
|                         |  | 5.0                                 | 16.8                |                                | f <sub>CD</sub> = 10 MHz<br>f <sub>I</sub> = 2.5 MHz<br>Eight Bits Toggling               | V <sub>IN</sub> = 3.4V<br>V <sub>IN</sub> = GNI |
|                         | anV = IV   |                                     |                     |                                | 50% Duty Cycle  | 1114  |

Note 1: Maximum test duration not to exceed one second, not more than one output shorted at one time.

Note 2: This parameter guaranteed but not tested.

Note 3: Per TTL driven input (V<sub>IN</sub> = 3.4V); all other inputs at V<sub>CC</sub> or GND.

Note 4: This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

Note 5: Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC

IC = ICC + AICC DHNT + ICCD (fcp/2 + fl Ni)

I<sub>CC</sub> = Quiescent Current

ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)

D<sub>H</sub> = Duty Cycle for TTL inputs High

N<sub>T</sub> = Number of Inputs at D<sub>H</sub>

I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f<sub>I</sub> = Input Frequency

N<sub>I</sub> = Number of Inputs at f<sub>I</sub>

All currents are in milliamps and all frequencies are in megahertz.

2-10

2-9

ns

|                  |   | 54FCTA/74FCTA  | 74FCTA  | 1          | 54FCTA  | Units  | Fig.<br>No. |
|------------------|---|--|---|------------|---|--|-------------|
| Symbol           | Parameter                                 | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$   | T <sub>A</sub> , V <sub>CC</sub> = 0<br>R <sub>L</sub> = 500<br>C <sub>L</sub> = 50 p | Ω          | $T_A$ , $V_{CC} = Mil$ $R_L = 500\Omega$ $C_L = 50 pF$                              |  |             |
|                  |   | Тур  | Min   | Max        | Min Max   |  |             |
| t <sub>PLH</sub> | Propagation Delay<br>CP to O <sub>n</sub> | 4.5  | 2.0   | 6.5        | orintion  | ns   | 2-8         |
| t <sub>PZH</sub> | Output Enable Time                        | S 64FOTY AFOT846A  | 1967  |            | st of registered bus trans<br>flip-flops and control or                             | Control of the Contro |             |
| t <sub>PHZ</sub> | Output Disable Time                       | bns emit4.0n bexelqu   | uM 1.5 8 to A   | 5.5        | ision of data cirectly from<br>storage registers. Data<br>to the respective registe | ns   | 2-11        |
| tsu              |   | /GMOS input and output and output and company as magnificant, as more levels | 2.0   |            | of the appropriate clock<br>as NSC quiot series tect                                | ns   | 2-10        |
| tн               | Hold Time                                 |  |   | enti Qinno | culput switching and dyr  | delup bevo   | iqmi eb     |

1.5

5.0

tilga bas notbered toorlarebau as

0.5

4.0

Note 1: Minimum limits are guaranteed but not tested on propagation delays.

#### Capacitance (T<sub>A</sub> = +25°C, f = 1.0 MHz)

High or Low

D<sub>n</sub> to CP CP Pulse Width

High or Low

tw

| Symbol           | Parameter (Note 1) | Тур | Max | Units | Conditions            |
|------------------|--------------------|-----|-----|-------|-----------------------|
| CIN              | Input Capacitance  | 6   | 10  | pF    | $V_{IN} = 0V$         |
| C <sub>OUT</sub> | Output Capacitance | 8   | 12  | pF    | V <sub>OUT</sub> = 0V |

Pin Names Description
Ag-Ar Oata Register A Inputs
Bg-Br Data Register A Outputs
Data Register B Inputs
Data Register B Inputs
CPAB, Clock Pulse Inputs
CPBA
Transmit/Receive Inputs
SAB, SBA
Transmit/Receive Inputs
Output Enable Input
Output Control Input

# 54FCT/74FCT646A Octal Transceiver/Register with TRI-STATE® Outputs

#### **General Description**

The FCT646A consist of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CPAB or CPBA).

FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

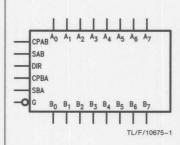
#### **Features**

- NSC 54FCT/74FCT646A is pin and functionally equivalent to IDT 54FCT/74FCT646A
- Independent registers for A and B buses
- Multiplexed real-time and stored data transfers
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 64 mA (Com), 48 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

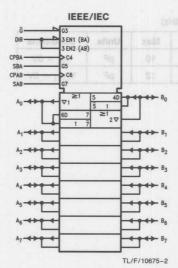
#### **Logic Symbols**

#### **Connection Diagrams**

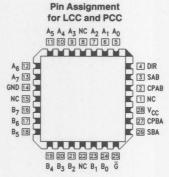
Symbol



| Pin Names                      | Description                                    |
|--------------------------------|--|
| A <sub>0</sub> -A <sub>7</sub> | Data Register A Inputs Data Register A Outputs |
| B <sub>0</sub> -B <sub>7</sub> | Data Register B Inputs Data Register B Outputs |
| CPAB,<br>CPBA                  | Clock Pulse Inputs                             |
| SAB, SBA<br>G                  | Transmit/Receive Inputs Output Enable Input    |
| DIR                            | Direction Control Input                        |







TL/F/10675-4

# 54FCT/74FCT821A • 54FCT/74FCT821B • 54FCT/74FCT82B • 54FCT/7

#### **General Description**

The 'FCT821A/B is a 10-bit D flip-flop with TRI-STATE oututs arranged in a broadside pinout.

FACTTM FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

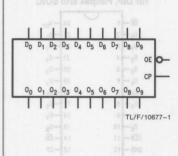
FACT FCTA features GTOTM output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

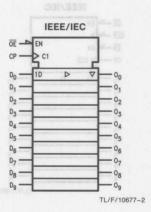
#### **Features**

- NSC 54FCT/74FCT821A/B is pin and functionally equivalent to IDT 54FCT/74FCT821A/B
- High-speed parallel registers with positive edge-triggered D-type flip-flops for ringing suppression
- Buffered common clock enable (EN) and asynchronous clear input (CLR)
- Input clamp diodes for ringing suppression
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (COM), 32 mA (MIL)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883
- TRI-STATE outputs for bus interfacing
- Noninverting outputs

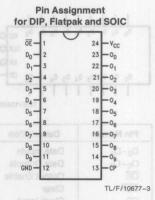
#### **Logic Symbols**

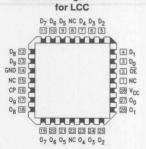


| Pin Names                      | Description         |  |  |
|--------------------------------|---------------------|--|--|
| D <sub>0</sub> -D <sub>9</sub> | Data Inputs         |  |  |
| 00-09                          | Data Outputs        |  |  |
| ŌĒ                             | Output Enable Input |  |  |
| CP 400                         | Clock Input         |  |  |



#### **Connection Diagrams**





**Pin Assignment** 

TL/F/10677-4



#### ADVANCE INFORMATION

# 54FCT/74FCT823A • 54FCT/74FCT823B S TOTAL TOTAL 9-Bit D Flip-Flop (1988) TOTAL

#### **General Description**

The 'FCT823A/B is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems.

FACTTM FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

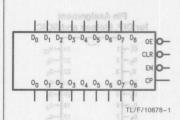
FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

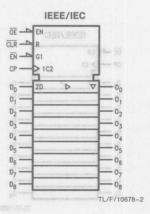
- NSC 54FCT/74FCT823A/B is pin and functionally equivalent to IDT 54FCT/74ACT823A/B
- High speed parallel registers with positive edge-triggered D-type flip-flop
- Buffered common clock enable (EN) and asynchronous clear input (CLR)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- IOI = 48 mA (Com), 32 mA (Mil)
- CMOS power levels of an advance not and anuono stigs a
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD 883

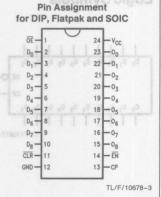
#### **Logic Symbols**

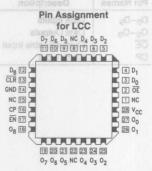
#### **Connection Diagrams**



| Pin Names                      | Description   |
|--------------------------------|---------------|
| D <sub>0</sub> -D <sub>8</sub> | Data Inputs   |
| 00-08                          | Data Outputs  |
| ŌĒ                             | Output Enable |
| - CLR                          | Clear         |
| CP                             | Clock Input   |
| EN insmr                       | Clock Enable  |







TL/F/10678-4





## 54FCT/74FCT825A • 54FCT/74FCT825B

#### **General Description**

The 'FCT825A/B is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multiuse control of the interface.

FACTTM FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- NSC 54FCT/74FCT825A/B is pin and functionally equivalent to IDT 54FCT/74FCT825A/B
- High-speed parallel registers with positive edge-triggered D-type flip flops
- Buffered common clock enable (EN) and asynchronous Clear input (CLR)
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

#### **Logic Symbols**

Pin Nam

D0-D7

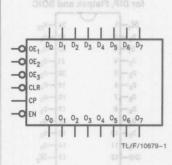
00-07

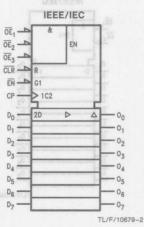
EN

CLR

CP

OE1, OE2,

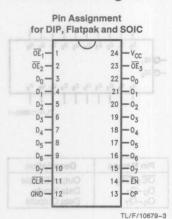


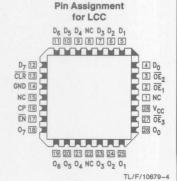


|                 |  | D <sub>i</sub> |
|-----------------|--|----------------|
| es              | Description  | 7              |
| ŌĒ <sub>3</sub> | Data Inputs Data Outputs Output Enables Clock Enable Clear |                |

Clock Input

#### **Connection Diagrams**





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# 54FCT/74FCT827A • 54FCT/74FCT827B 10-Bit Buffer/Line Driver with TRI-STATE® Outputs

#### **General Description**

The 'FCT827A/B 10-bit bus buffer provides high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

FACTTM FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

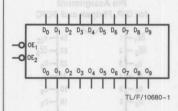
#### **Features**

- NSC 54FCT/74FCT827A/B is pin and functionally equivalent to IDT 54FCT/74FCT827A/B
- High Speed parallel registers with positive edge-triggered D-type flip-flops
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels

TI /F/10680-2

- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

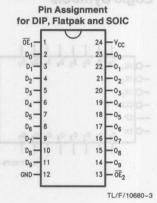
#### **Logic Symbols**



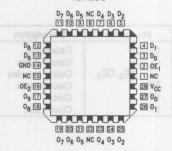
| Pin Names                         | Description Output Enable |  |  |
|-----------------------------------|---------------------------|--|--|
| OE <sub>1</sub> , OE <sub>2</sub> |                           |  |  |
| D <sub>0</sub> -D <sub>7</sub>    | Data Inputs Data Outputs  |  |  |

#### IEEE/IEC FN1 D<sub>1</sub> D<sub>2</sub> 03 D<sub>4</sub> 04 D<sub>5</sub> 05 D<sub>6</sub> 06 D<sub>7</sub> 07 D<sub>8</sub> D<sub>9</sub> 09

#### **Connection Diagrams**



### Pin Assignment for LCC



TL/F/10680-4

### 10-Bit Transparent Latch with TRI-STATE® Outputs

#### **General Description**

The bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT841A/B is a 10-bit transparent latch, a 10-bit version of the FCT373A.

FACTTM FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

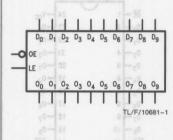
FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

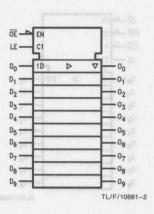
FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

- NSC 54FCT/74FCT841A/B is pin and functionally equivalent to IDT 54FCT/74FCT841A/B
- High Speed parallel latches
- Buffered common latch enable, clear and preset input
- Input clamp diodes to limit bus reflections
- TIL/CMOS input and output level compatible
- IOI = 48 mA (com), 32 mA (mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military Product compliant to MIL-STD 883

#### **Logic Symbols**





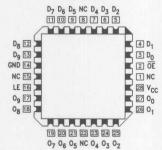
| Pin Names   | Description       |  |  |
|---|-------------------|--|--|
| D <sub>0</sub> -D <sub>9</sub>                                | Data Inputs       |  |  |
| D <sub>0</sub> -D <sub>9</sub> O <sub>0</sub> -O <sub>9</sub> | TRI-STATE Outputs |  |  |
| OE  | Output Enable     |  |  |
| LE  | Latch Enable      |  |  |

#### **Connection Diagrams**

Pin Assignment for DIP, Flatpak and SOIC



### Pin Assignment for LCC



TL/F/10681-4



#### ADVANCE INFORMATION

# 54FCT/74FCT843A • 54FCT/74FCT843B 9-Bit Transparent Latch

#### **General Description**

The 'FCT843A/B bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths.

FACTTM FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

#### **Features**

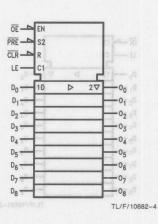
- NSC 54FCT/74FCT843A/B is pin and functionally equivalent to IDT 54FCT/74FCT843A/B
- High Speed parallel latches
- Buffered common latch enable, clear and preset inputs
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- I<sub>OL</sub> = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity TOTAL ASSISTED ATOP TOAR
- Military Product compliant to MIL-STD 883

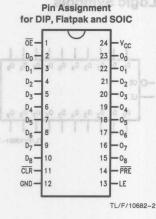
#### **Logic Symbols**

#### **Connection Diagrams**

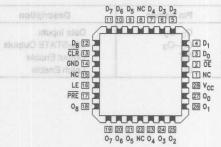


| A  |                               |  |  |
|--|-------------------------------|--|--|
| Pin Names  | Description                   |  |  |
| D <sub>0</sub> -D <sub>7</sub><br>O <sub>0</sub> -O <sub>7</sub> | Data Inputs<br>Data Outputs   |  |  |
| OE LE  | Output Enable<br>Latch Enable |  |  |
| PRE Inom   | Clear<br>Preset               |  |  |









TL/F/10682-3



### 54FCT/74FCT845A • 54FCT/74FCT845B 8-Bit Transparent Latch with TRI-STATE® Outputs

#### **General Description**

The 'FCT845A/B bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple OE controls.

FACTTM FCTA/B utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features GTO™ output control and undershoot corrector in addition to a split ground bus for superior per-

FACT FCTB features an undershoot corrector in addition to a split ground bus for superior performance.

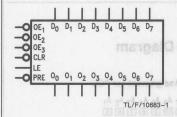
#### **Features**

- NSC 54FCT/74FCT845A/B is pin and functionally equivalent to IDT 54FCT/74FCT845A/B
- High speed parallel latches
- Buffered common latch enable, clear and preset input
- Input clamp diodes to limit bus reflections
- TTL/CMOS input and output level compatible
- IOI = 48 mA (Com), 32 mA (Mil)
- CMOS power levels
- 4 kV minimum ESD immunity
- Military product compliant to MIL-STD 883

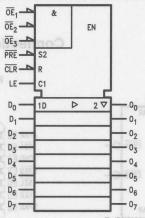
#### **Logic Symbols**

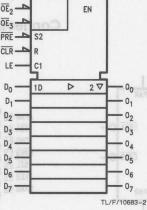
#### **Connection Diagrams**

Pin Assignment for DIP, Flatpak and SOIC

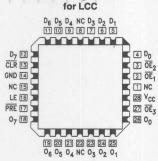


| Pin Names                        | Description    |
|----------------------------------|----------------|
| D <sub>0</sub> -D <sub>7</sub>   | Data Inputs    |
| 00-07                            | Data Outputs   |
| OE <sub>1</sub> -OE <sub>3</sub> | Output Enables |
| LE .88                           | Latch Enable   |
| CLR                              | Clear          |
| PRE                              | Preset         |









**Pin Assignment** 

TL/F/10683-4

#### 54FC1//4FC1899A

#### 54FCT/74FCT845A · 54FCT/74F 9-Bit Latchable Transceiver with Parity Generator/Checker

#### **General Description**

The 'FCT899A is a 9-bit to 9-bit parity transceiver with transparent latches. The device can operate as a feed-through transceiver or it can generate/check parity from the 8-bit data busses in either direction. It has a guaranteed current sinking capability of 24 mA at the A-bus and 64 mA at the

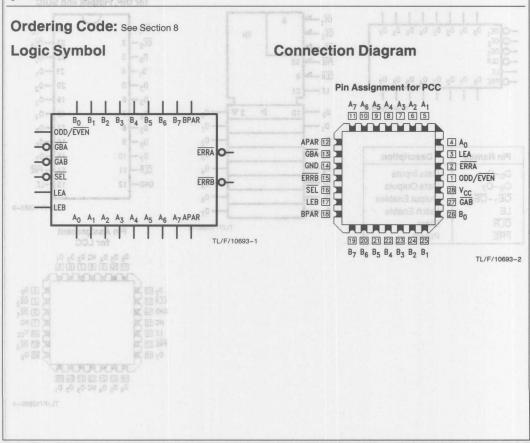
The 'FCT899A features independent latch enables for the A-to-B direction and the B-to-A direction, a select pin for ODD/EVEN parity, and separate error signal output pins for

FACTTM FCTA utilizes NSC quiet series technology to provide improved quiet output switching and dynamic threshold performance.

FACT FCTA features undershoot correction and split ground bus for superior performance.

#### **Features**

- Latchable transceiver with output sink of 24 mA at the A-bus and 64 mA at the B-bus
- Option to select generate parity and check or "feedthrough" data/parity in directions A-to-B or B-to-A
- Independent latch enables for A-to-B and B-to-A direc-
- Select pin for ODD/EVEN parity
- ERRA and ERRB output pins for parity checking
- Ability to simultaneously generate and check parity
- CMOS power levels what to be and and beautiful as
- Guaranteed 4000V min ESD protection



| ODD/EVEN   | ODD/EVEN Parity Select, Active LOW for EVEN Parity                                    |
|------------|---|
| GBA, GAB   | Output Enables for A or B Bus,<br>Active LOW  |
| SEL        | Select Pin for Feed-Through or<br>Generate Mode, LOW for Generate<br>Mode             |
| LEA, LEB   | Latch Enables for A and B Latches,<br>HIGH for Transparent Mode                       |
| ERRA, ERRB | Error Signals for Checking<br>Generated Parity with Parity In,<br>LOW if Error Occurs |

- Bus A (B) communicates to Bus B (A), parity is generated and passed on to the B (A) Bus as BPAR (APAR). If LEB (LEA) is HIGH and the Mode Select (SEL) is LOW, the parity generated from B[0:7] (A[0:7]) can be checked and monitored by ERRB (ERRA).
- Bus A (B) communicates to Bus B (A) in a feed-through mode if SEL is HIGH. Parity is still generated and checked as ERRA and ERRB in the feed-through mode (can be used as an interrupt to signal a data/parity bit error to the CPU).
- Independent Latch Enables (LEA and LEB) allow other permutations of generating/checking (see Function Table below).

|     | Function Table function |     |     |           |  |  |
|-----|-------------------------|-----|-----|-----------|--|--|
|     | Inputs                  |     |     | Operation |  |  |
| GAB | GBA                     | SEL | LEA | LEB       |  |  |
| Н   | Н                       | X   | X   | X         | Busses A and B are TRI-STATE®.   |  |
| Н   | L                       | L   | L   | Н         | Generates parity from B[0:7] based on O/Ē (Note 1). Generated parity → APAR. Generated parity checked against BPAR and output as ĒRRĒ.   |  |
| Н   | L                       | L   | Н   | Н         | Generates parity from B[0:7] based on O/Ē. Generated parity → APAR. Generated parity checked against BPAR and output as ERRB Generated parity also fed back through the A latch for generate/chec as ERRA.   |  |
| Н   | L                       | L   | X   | -         | Generates parity from B latch data based on O/Ē. Generated parity  → APAR. Generated parity checked against latched BPAR and output as ERRB.   |  |
| Н   | L                       | Н   | X   | Н         | BPAR/B[0:7] → APAR/A0:7] Feed-through mode. Generated parity checked against BPAR and output as ERRB.  |  |
| H   | L                       | Н   | Н   | Н         | BPAR/B[0:7] → APAR/A[0:7] Feed-through mode. Generated parity checked against BPAR and output as ERRB. Generated parity also fed back through the A latch for generate/check as ERRA.                        |  |
| L   | Н                       | L   | Н   | L         | Generates parity for A[0:7] based on O/Ē. Generated parity → BPAR. Generated parity checked against APAR and output as ERRĀ.   |  |
| L   | Н                       | L   | Н   | Н         | Generates parity from A[0:7] based on O/Ē. Generated parity → BPAR. Generated parity checked against APAR and output as ĒRRĀ. Generated parity also fed back through the B latch for generate/check as ĒRRĒ. |  |
| L   | Н                       | L   | L   | X         | Generates parity from A latch data based on O/Ē. Generated parity  → BPAR. Generated parity checked against latched APAR and output as ERRA.   |  |
| L   | Н                       | Н   | Н   | L         | APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as ERRA.   |  |
| L   | Н                       | Н   | Н   | Н         | APAR/A[0:7] → BPAR/B[0:7] Feed-through mode. Generated parity checked against APAR and output as ERRA. Generated parity also fed back through the B latch for generate/check as ERRB.                        |  |

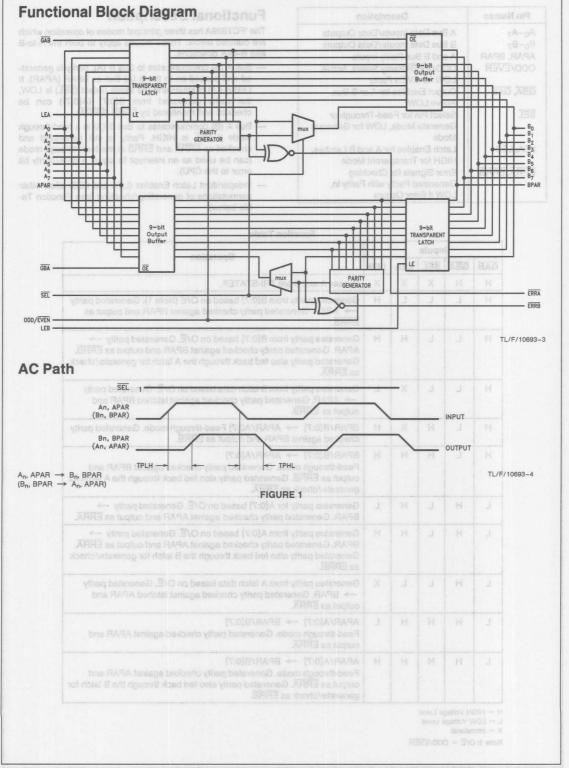
H = HIGH Voltage Level

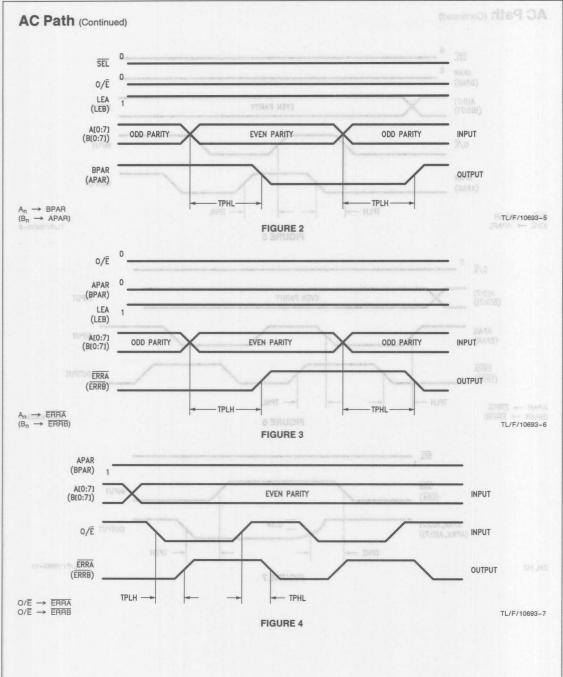
Note 1: O/E = ODD/EVEN

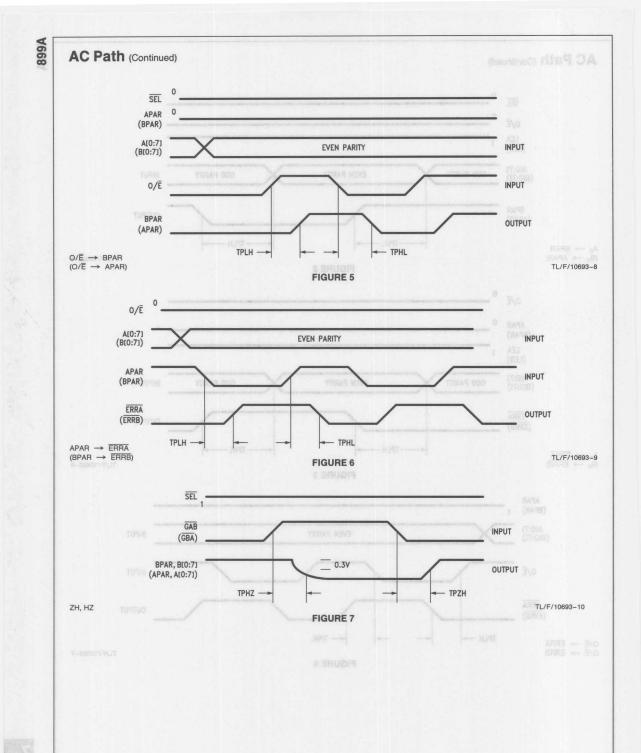
L = LOW Voltage Level

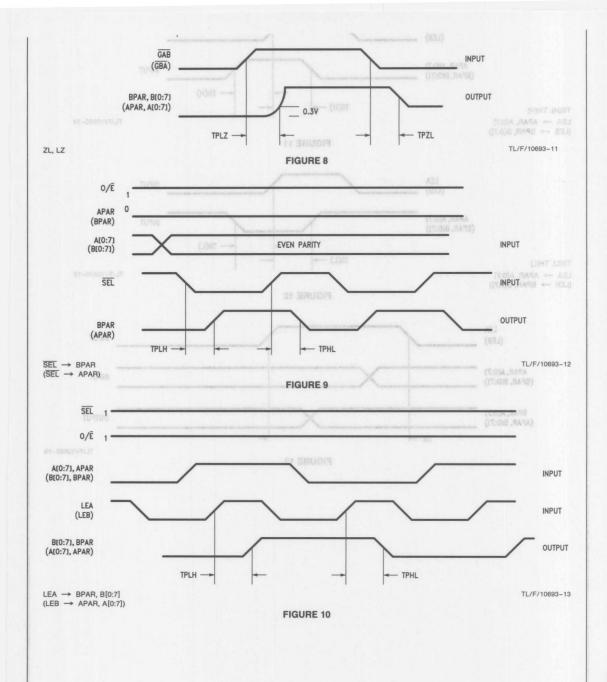
X = Immaterial

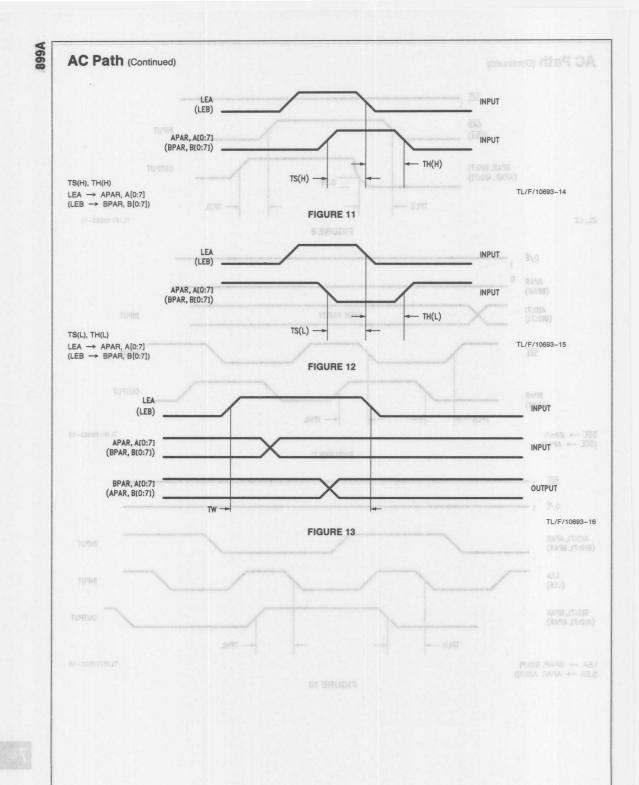












#### Absolute Maximum Ratings (Note 1) Recommended Operating

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Terminal Voltage with Respect to GND (V<sub>TERM</sub>) -0.5V to +7.0V 54FCTA 74FCTA -0.5V to +7.0V Temperature under Bias (TBIAS) -55°C to +125°C 74FCTA 54FCTA -65°C to +135°C Storage Temperature (T<sub>STG</sub>)

54FCTA -65°C to +150°C Power Dissipation (P<sub>T</sub>) 0.5W DC Output Current (I<sub>OUT</sub>) 120 mA

74FCTA

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. Exposure to absolute maximum rating conditions for extended periods may affect reliability. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

### Conditions No.2 = DOV to etc. equiev lookyT

Supply Voltage (Vcc) 4.5V to 5.5V 54FCTA 74FCTA 4.75V to 5.25V Input Voltage OV to Vcc OV to VCC Output Voltage Operating Temperature (TA) -55°C to +125°C 54FCTA 74FCTA -0°C to +70°C Junction Temperature (T<sub>J</sub>) CDIP 175°C PDIP 140°C

#### DC Characteristics for 'FCTA Family Devices

-55°C to +125°C

Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading. For test conditions shown as Max, use the value specified for the appropriate device type: Com:  $V_{CC}=5.0V\pm5\%$ ,  $T_A=0^{\circ}C$  to  $+70^{\circ}C$ ; Mil:  $V_{CC}5.0V\pm10\%$   $T_A=-55^{\circ}C$  to  $+125^{\circ}$ C,  $V_{HC} = V_{CC} - 0.2V$ 

| Symbol           | Parameter                                    | 54                      | FCTA/74F                      | CTA                               | Units      | h, brodes and besides of for reciprob last mumbers of along  |  |  |
|------------------|--|-------------------------|-------------------------------|-----------------------------------|------------|--|--|--|
|                  | rarameter                                    | Min                     | Тур                           | Max                               | MO so solv | betsel for the Conditions of the start of th |  |  |
| V <sub>IH</sub>  | Minimum High Level<br>Input Voltage          | 2.0                     | pply calculat<br>parameted b  | ntal Polser Su<br>se limita ara p | Trained to | e Tria parameter la not directly testable, but la derivad<br>E: Values for these conditions are examples of the Igo  |  |  |
| V <sub>IL</sub>  | Maximum Low Level<br>Input Voltage           |                         |                               | 0.8                               | V          | + 1ecp (1cp/2 + 1; Ni)   |  |  |
| IIH              | Input High Current                           |                         |                               | 5.0<br>5.0                        | μΑ         | V <sub>CC</sub> = Max  | T.   (14010 L)   |  |
| IIL              | Input Low Current                            |                         |                               | -5.0<br>-5.0                      | μΑ         | V <sub>CC</sub> = Max  | $V_l = 0.5V \text{ (Note 2)}$<br>$V_l = \text{GND}$  |  |
| loz              | Maximum TRI-STATE<br>Current                 |                         |                               | 10.0<br>10.0<br>-10.0<br>-10.0    | μΑ         | V <sub>CC</sub> = Max  | V <sub>I</sub> = V <sub>CC</sub><br>V <sub>I</sub> = 2.7V (Note 2)<br>V <sub>I</sub> = 0.5V (Note 2)<br>V <sub>I</sub> = GND |  |
| V <sub>IK</sub>  | Clamp Diode Voltage                          |                         | -0.7                          | -1.2                              | V          | $V_{CC} = Min; I_N = -1$   | 8 mA   |  |
| los              | Short Circuit Current                        | -60                     | -120                          |                                   | mA         | V <sub>CC</sub> = Max (Note 1);  | $V_O = GND$  |  |
|                  |  | 2.8                     | 3.0                           |                                   |            | $V_{CC} = 3V; V_{IN} = 0.2$  | $PV \text{ or } V_{HC}; I_{OH} = -32 \mu r$  |  |
| V <sub>OH</sub>  | Minimum High Level<br>Output Voltage         | V <sub>HC</sub> 2.4 2.4 | V <sub>CC</sub><br>4.3<br>4.3 |                                   | ٧          | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OH} = -300 \mu\text{A}$<br>$I_{OH} = -12 \text{mA} (\text{Mil})$<br>$I_{OH} = -15 \text{mA} (\text{Com})$                |  |
|                  |  |                         | GND                           | 0.2                               |            | $V_{CC} = 3V; V_{IN} = 0.2V \text{ or } V_{HC}; I_{OL} = 300$  |  |  |
| V <sub>OL</sub>  | Maximum Low Level<br>Output Voltage          |                         | GND<br>0.3<br>0.3             | 0.2<br>0.55<br>0.55               | V          | $V_{CC} = Min$ $V_{IN} = V_{IH} \text{ or } V_{IL}$  | $I_{OL} = 300 \mu A$<br>$I_{OL} = 48 \text{ mA (Mil)}$<br>$I_{OL} = 64 \text{ mA (Com)}$                                     |  |
| Icc              | Maximum Quiescent<br>Supply Current          |                         | 0.001                         | 1.5                               | mA         | $\begin{aligned} &V_{CC} = Max \\ &V_{IN} \geq V_{HC}, V_{IN} \leq 0.2 \\ &f_I = 0 \end{aligned}$  | ev   |  |
| ΔI <sub>CC</sub> | Quiescent Supply Current;<br>TTL Inputs HIGH |                         | 0.5                           | 2.0                               | mA         | V <sub>CC</sub> = Max<br>V <sub>IN</sub> = 3.4V (Note 3)   |  |  |

| Symbol  | Parameter                              |   | 5                  | 54FCTA/74FCTA           |                     |  | nits                          | Terminal Voltage with Respect to GND  Conditions ATCAS   |   |   |  |
|---|--|---|--------------------|-------------------------|---------------------|--|-------------------------------|--|---|---|--|
| 20 v 01 v0  |  | Min   | Тур                | Max                     |                     | -0.5\  |                               |  | ZAFCT   |   |  |
| Dynamic Power Supply Current (Note  |  | 12, 17, 27123   | emperative rations | 0.25 0.40               |                     |  | /MHz                          | V <sub>CC</sub> = Max<br>Outputs Open<br>One Input Toggling<br>50% Duty Cycle  | $\begin{aligned} & V_{\text{IN}} \geq V_{\text{HC}} \\ & V_{\text{IN}} \leq 0.2V \end{aligned}$ $\begin{aligned} & V_{\text{IN}} \leq V_{\text{HC}} \\ & V_{\text{IN}} \leq 0.2V \end{aligned}$ |   |  |
| 175°C   |  |   | 1.5                |                         | 4.0                 | 0 + 150°C<br>0 SW<br>120 mA  | - 65°C 1                      | V <sub>CC</sub> = Max<br>Outputs Open<br>f <sub>I</sub> = 10 MHz   |   |   |  |
|   | Total Power                            | er  |                    | 1.8                     | 5.0                 | hich damag<br>ng oceal tion  | w bnoyed a                    | One Bit Toggling<br>50% Duty Cycle   | 47 103337120  | $\begin{aligned} &V_{IN} = 3.4V \\ &V_{IN} = GND \end{aligned}$ $\begin{aligned} &V_{IN} \geq V_{HC} \\ &V_{IN} \leq 0.2V \end{aligned}$ $\begin{aligned} &V_{IN} = 3.4V \end{aligned}$ |  |
| etilev offi   | Supply Cui                             | rrent (Note 6)  |                    |                         | 6.5                 | and in regions and interest and | ATO- neidma C                 | (Note 5)  V <sub>CC</sub> = Max  Outputs Open  f <sub>I</sub> = 2.5 MHz  Eight Bits Toggling   | VIN   |   |  |
|   |  |   |                    | 0.0                     | 14.0                |  |                               | 50% Duty Cycle   | VIN   | = GND   |  |
| Note 2: This p  | parameter guaran                       | not to exceed one steed but not tested.                       |                    |                         |                     | shorted at or  | ne time.                      | Parameter  |   | lodmy   |  |
| Note 4: This p  | parameter is not ones for these condi- | lirectly testable, but i                                      | is derived         | for use in To           | otal Power S        |  |                               | ed. Level Level to the level to |   |   |  |
| Note 6: IC = IQUIESCENT + INPUTS + IDYNAMIC  IC = ICC + AICC DHNT + ICCD (fcp/2 + f)  ICC = Quiescent Current |  | N <sub>I</sub> )  | ¥                  |                         |                     |  | ximum Low Level<br>ut Voltage |  |   |   |  |
| D <sub>H</sub> =  | Duty Cycle for T                       |   | gh Input (         | V <sub>IN</sub> = 3.4V) |                     |  |                               |  |   |   |  |
| ICCD :  |  | s at D <sub>H</sub> nt Caused by an Inper for Register Device |                    |                         |                     |  |                               | t Low Current  |   |   |  |
| (S. N <sub>L</sub> =  |  | at f <sub>l</sub><br>imps and all frequen                     | icles are in       | n megahertz.            |                     |  |                               | TAVE TALESTATE   |   |   |  |
|   | CIVID = IV                             |   |                    |                         | -10.0               |  |                               |  |   |   |  |
|   |  |   |                    |                         | -1.2                |  |                               |  |   |   |  |
|   |  |   |                    |                         |                     |  |                               | rt Circuit Current   |   |   |  |
|   |  |   |                    |                         |                     | 3.0<br>Voc<br>4.3  | 2.8<br>VHC<br>2.4<br>2.4      | Minimum High Level<br>Output Vollage   |   |   |  |
|   |  |   |                    |                         |                     |  |                               |  |   |   |  |
|   |  |   |                    |                         | 0.2<br>0.55<br>0.55 |  |                               | Maximum Low Level<br>Output Voltage  |   |   |  |
|   |  |   |                    |                         |                     |  |                               |  |   |   |  |
|   |  |   |                    |                         |                     | 100.0  |                               |  |   |   |  |

#### **AC Electrical Characteristics**

| Symbol                               |  | 54FCTA/74FCTA                        |      | FCTA                         | 541  | CTA | Units | Fig.  |
|--------------------------------------|--|--------------------------------------|------|------------------------------|--|-----|-------|-------|
|                                      | Parameter  | $T_A = +25^{\circ}C$ $V_{CC} = 5.0V$ | RL = | C = Com<br>= 500Ω<br>= 50 pF | $\begin{aligned} \mathbf{T_A}, \mathbf{V_{CC}} &= \mathbf{Mil} \\ \mathbf{R_L} &= 500\Omega \\ \mathbf{C_L} &= 50 \ \mathbf{pF} \end{aligned}$ |     |       |       |
|                                      |  | Тур                                  | Min  | Max                          | Min  | Max |       |       |
| t <sub>PHL</sub>                     | Propagation Delay A <sub>n</sub> to B <sub>n</sub> or B <sub>n</sub> to A <sub>n</sub> | 10.0                                 | 2.5  | 11.0                         |  |     | ns    | 1     |
| t <sub>PLH</sub>                     | Propagation Delay<br>APAR to BPAR or<br>BPAR to APAR                                   | 11.0                                 | 1.5  | 8.0                          |  |     | ns    | 1     |
| t <sub>PHL</sub>                     | Propagation Delay A to BPAR or B to APAR SEL = 0                                       | 13.0                                 | 2.5  | 11.5                         |  |     | ns    | 2     |
| t <sub>PHL</sub>                     | Propagation Delay A to ERRA or B to ERRB   | 13.0                                 | 2.0  | 11.0                         |  |     | ns    | 3     |
| t <sub>PHL</sub>                     | Propagation Delay ODD/EVEN to ERRA, ERRB or APAR, BPAR                                 | 13.0                                 | 2.0  | 11.0                         |  |     | ns    | 4, 5  |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay<br>SEL to APAR or BPAR   | 10.5                                 | 1.5  | 8.5                          |  |     | ns    | 9     |
| t <sub>PHL</sub>                     | Propagation Delay<br>LEA/LEB to B/A<br>or BPAR/APAR                                    | 11.0                                 | 2.0  | 11.0                         |  |     | ns    | 10, 1 |
| t <sub>PZL</sub><br>t <sub>PZH</sub> | Output Enable Delay  | 9.5                                  | 1.5  | 10.0                         |  |     | ns    | 7, 8  |
| t <sub>PHZ</sub>                     | Output Disable Enable  | 11.0                                 | 1.5  | 8.5                          |  |     | ns    | 7, 8  |
| tset                                 | Setup Time<br>A to LEA or B to LEB   | 3.0                                  | 3.0  |                              |  |     | ns    | 11, 1 |
| <sup>t</sup> HOLD                    | Hold Time<br>A to LEA, B to LEB  | 1.5                                  | 1.5  |                              |  |     | ns    | 11, 1 |
| t <sub>W</sub>                       | Pulse Width<br>LEA or LEB  | 5.0                                  | 4.0  |                              |  |     | ns    | 13    |

#### AC Electrical Characteristics

|  |  |      |     | 74FCTA 54FC            |   |    |        |
|--|--|------|-----|------------------------|---|----|--------|
|  |  |      |     | = Com<br>600Ω<br>80 pF | $T_{A}$ $V_{CC} = MH$ $H_L = 500\Omega$ $C_L = 80 pF$ |    |        |
|  |  |      |     | XEM                    | Min Max   |    |        |
|  | Propagation Delay An to Bn or Sn to An           |      |     |                        |   |    |        |
|  | Propagation Delay APAR to BPAR or BPAR to APAR   | 0.11 |     |                        |   | an | r      |
|  | Propagation Delay A to BPAR or 8 to APAR SEL = 0 |      |     | 11.5                   |   |    |        |
|  | Propagation Dalay A to ERRA or B to ERRE         |      |     |                        |   | an |        |
|  |  |      |     |                        |   |    | 4,5    |
|  | Propagation Delay<br>SEI to APAR or SPAR         |      |     |                        |   |    |        |
|  |  |      |     | 0.11                   |   |    |        |
|  |  |      |     |                        |   |    |        |
|  |  |      |     |                        |   |    |        |
|  |  |      |     |                        |   |    | 11, 12 |
|  |  | a.r  | 1.5 |                        |   | en |        |
|  |  |      | 4.0 |                        |   |    |        |



| Contents | Section 8    |
|----------|--------------|
|          | Ordering Inl |
|          |              |

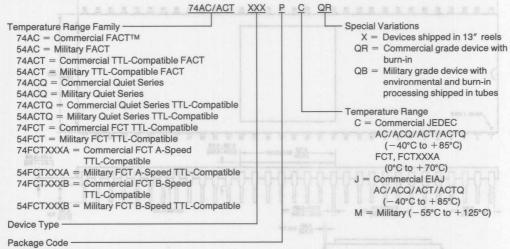
Section 8
Ordering Information and
Physical Dimensions

# **Section 8 Contents** Ordering Information and Physical Dimensions ..... 8-3 Bookshelf Distributors



#### Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



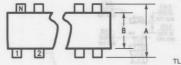
- P = Plastic DIP
- SP = Slim Plastic DIP
- D = Ceramic DIP
- SD = Slim Ceramic DIP
- F = Flatpak
- L = Leadless Ceramic Chip Carrier (LCC)
- Q = Plastic Leaded Chip Carrier (PCC)
- S = Small Outline (SOIC)

For most current packaging information, contact Product Marketing.

#### JEDEC-EIAJ Small Outline Package Comparison

|        | Dim | 14 Pin          |                 | 16 Pin          |                  | 20 Pin          |                 | 24 Pin          |                 |
|--------|-----|-----------------|-----------------|-----------------|------------------|-----------------|-----------------|-----------------|-----------------|
|        |     | Min             | Max             | Min             | Max              | Min             | Max             | Min             | Max             |
| JEDEC  | А   | 0.228 (5.80)    | 0.245 (6.20)    |                 | 0.420<br>(10.65) |                 |                 |                 |                 |
| ULDLO  | В   | 0.149 (3.80)    | 0.158 (4.00)    |                 |                  |                 |                 | 100             | 0.300<br>(7.60) |
| EIAJ   | А   | 0.300 (7.62)    | 0.350<br>(8.89) | 0.300<br>(7.62) | 0.350<br>(8.89)  | 0.300<br>(7.62) | 0.350<br>(8.89) | 0.300<br>(7.62) | 0.350<br>(8.89) |
| 217.10 | В   | 0.198<br>(5.02) | 0.245 (6.22)    | 0.198<br>(5.02) | 0.245<br>(6.22)  | 0.198<br>(5.02) | 0.245<br>(6.22) | 0.198<br>(5.02) | 0.245<br>(6.22) |

Units: Inch (mm)

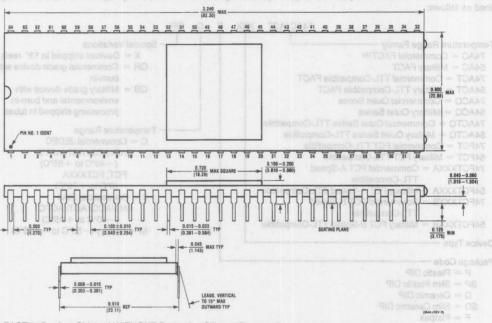


TL/F/10162-2



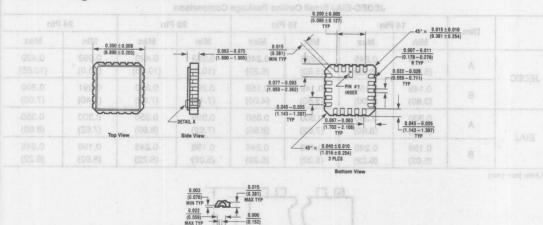
All dimensions are in inches (millimeters)

#### 64 Lead Side Brazed Ceramic Dual-In-Line Package (D) **NS Package Number D64A**

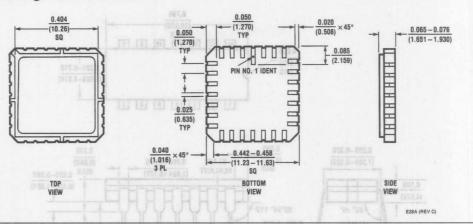


Note: FACTTM Product Shipped WITHOUT Protective Silicon "Bumpers".

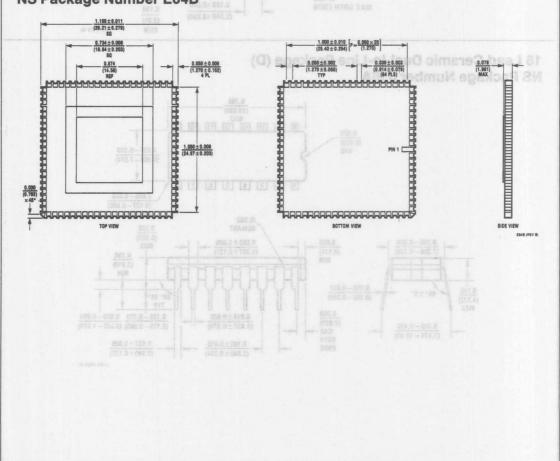
#### 20 Terminal Ceramic Leadless Chip Carrier (L) **NS Package Number E20A**



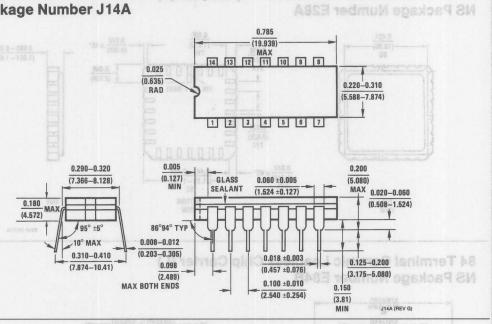
## 28 Terminal Ceramic Leadless Chip Carrier (L) Manual Simon Section 18 NS Package Number E28A



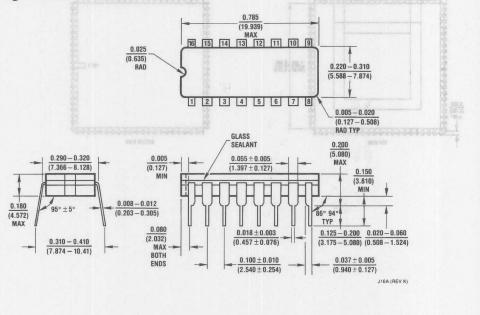
## 84 Terminal Ceramic Leadless Chip Carrier (L) NS Package Number E84B



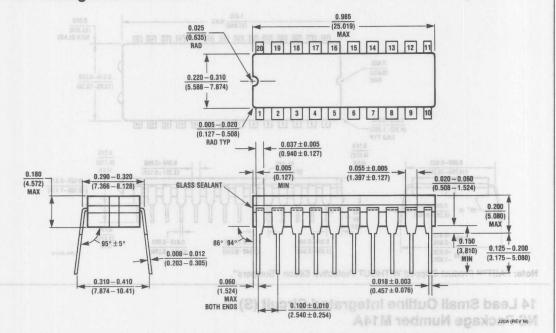
## 14 Lead Ceramic Dual-In-Line Package (D) 13 sasibas 1 simas 3 lanimis T 83 NS Package Number J14A A833 redmuM spackage 3M



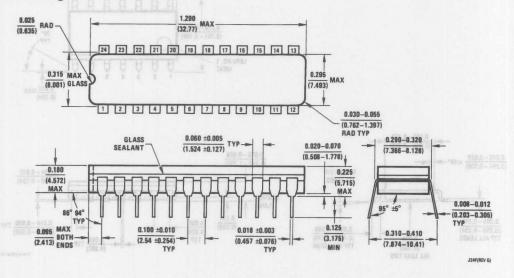
## 16 Lead Ceramic Dual-In-Line Package (D) NS Package Number J16A



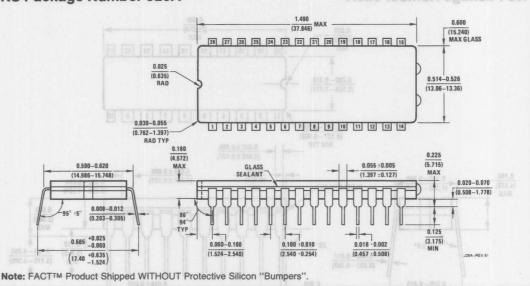




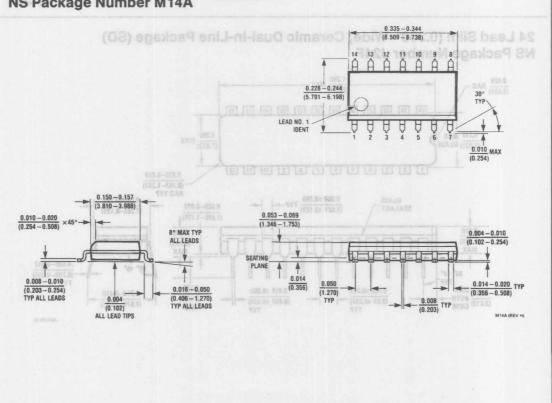
## 24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line Package (SD) NS Package Number J24F



## 28 Lead Ceramic Dual-In-Line Package (D) 89 ent.1-n1-lsuQ otmareO bee.1 02 NS Package Number J28A

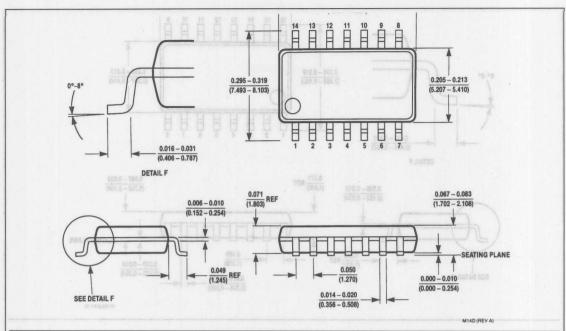


## 14 Lead Small Outline Integrated Circuit (S) NS Package Number M14A

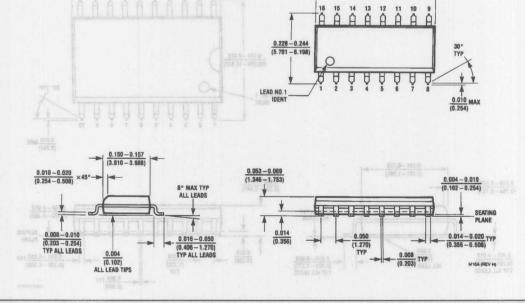


NS Package Number M208

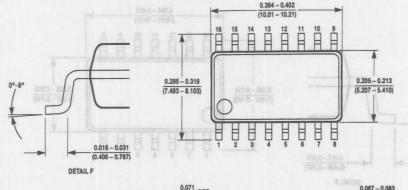
0.386 - 0.394 (9.804 - 10.00)

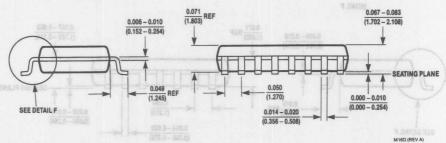


#### 20 Lead Small Outline Integrated C 16 Lead Small Outline Integrated Circuit (S) **NS Package Number M16A**

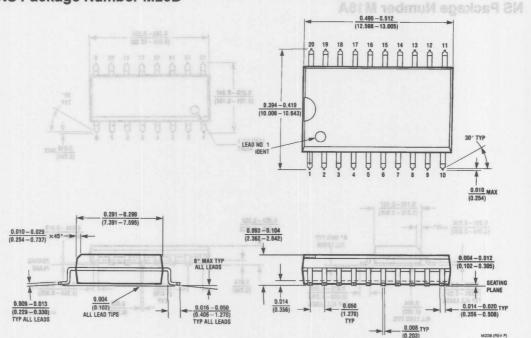


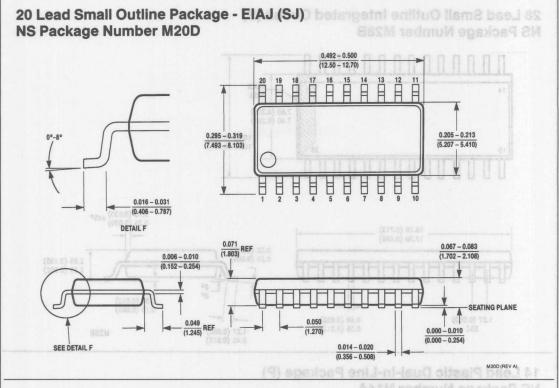
#### 

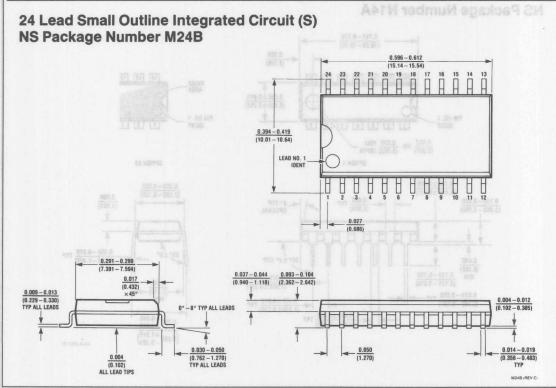




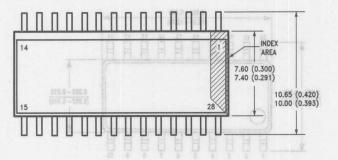
## 20 Lead Small Outline Integrated Circuit (S) NS Package Number M20B

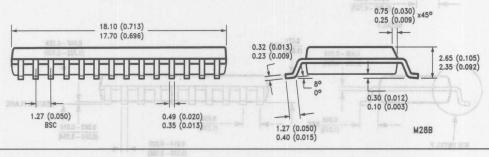






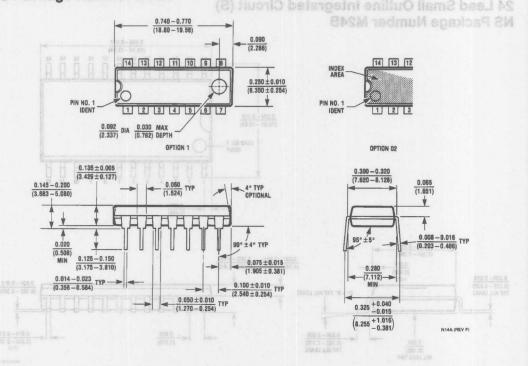
#### 28 Lead Small Outline Integrated Circuit (S) - species 9 shifts 0 lism2 bas\_1 0\$ **NS Package Number M28B**





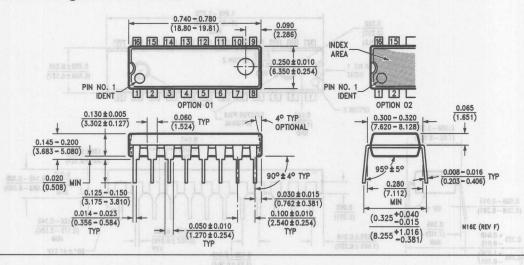
MS Package Number M20D

#### 14 Lead Plastic Dual-In-Line Package (P) **NS Package Number N14A**

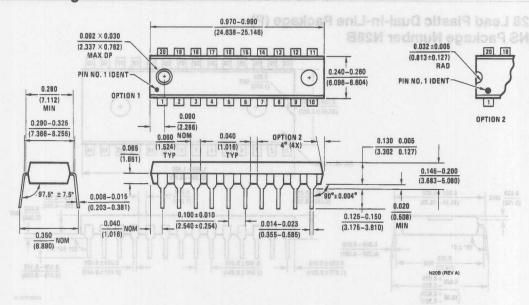


24 Lead Plastic Slim (0.300"

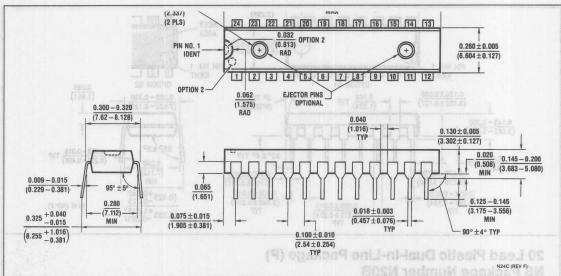
## 16 Lead Plastic Dual-In-Line Package (P) NS Package Number N16E



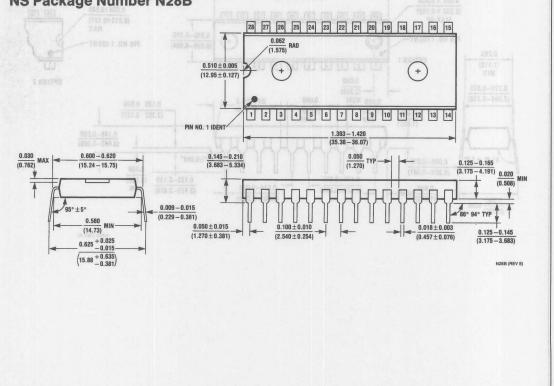
## 20 Lead Plastic Dual-In-Line Package (P) NS Package Number N20B





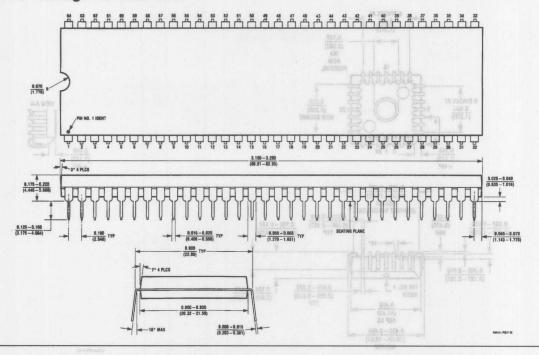


#### 28 Lead Plastic Dual-In-Line Package (P) NS Package Number N28B

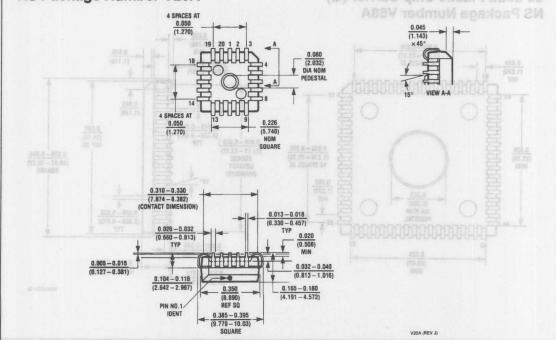


28 Lead Plastic Chip Carrier (Q)

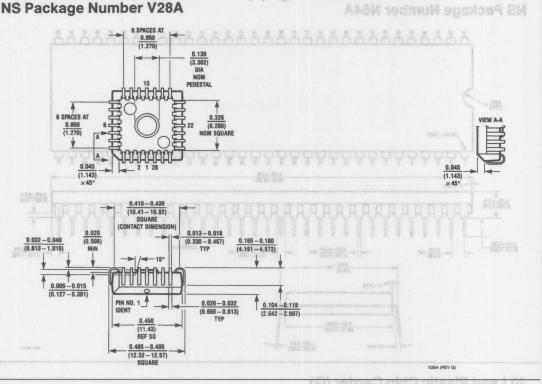
#### 64 Lead Plastic Dual-In-Line Package (P) NS Package Number N64A



## 20 Lead Plastic Chip Carrier (Q) NS Package Number V20A

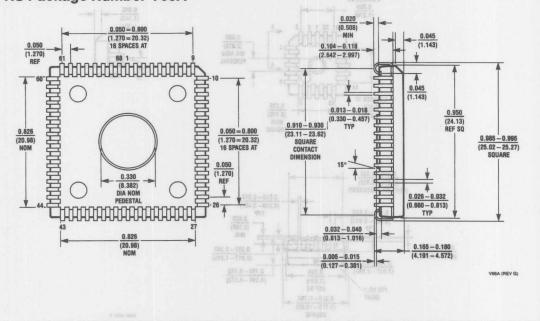


#### 28 Lead Plastic Chip Carrier (Q) NS Package Number V28A



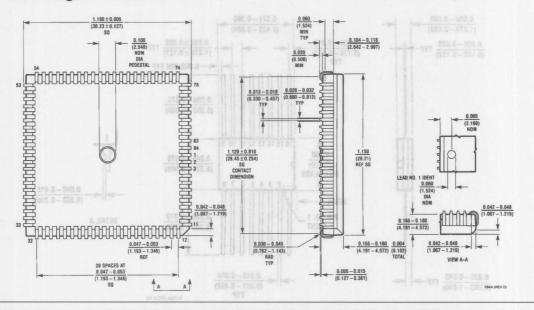
64 Lead Plastic Dual-In-Line Package (P)

#### 68 Lead Plastic Chip Carrier (Q) NS Package Number V68A

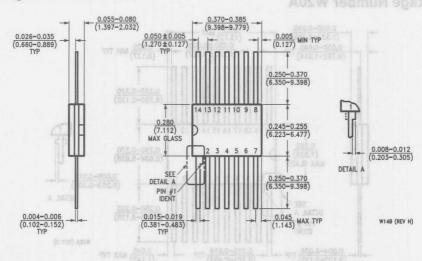


NS Package Number W16A

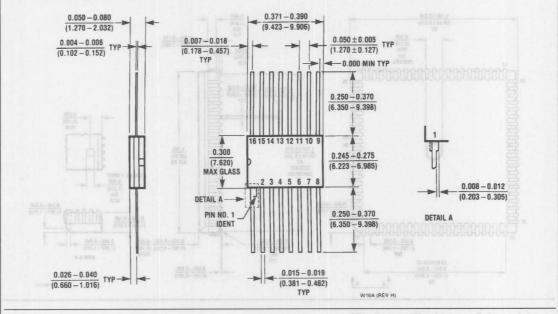
#### 84 Lead Plastic Chip Carrier (Q) NS Package Number V84A



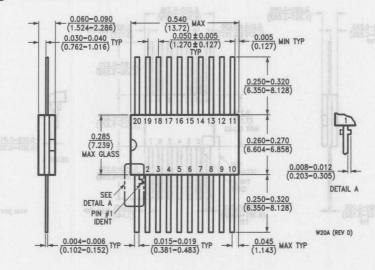
#### 14 Lead Ceramic Flatpak (F) NS Package Number W14B



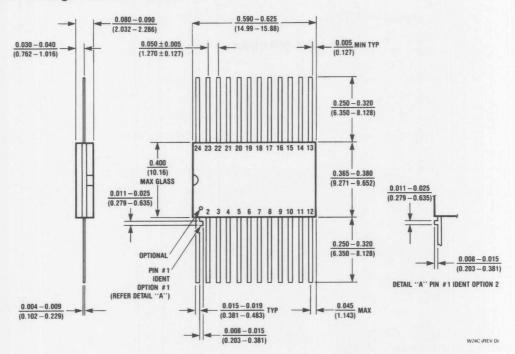
#### 16 Lead Ceramic Flatpak (F) NS Package Number W16A



#### 20 Lead Ceramic Flatpak (F) NS Package Number W20A

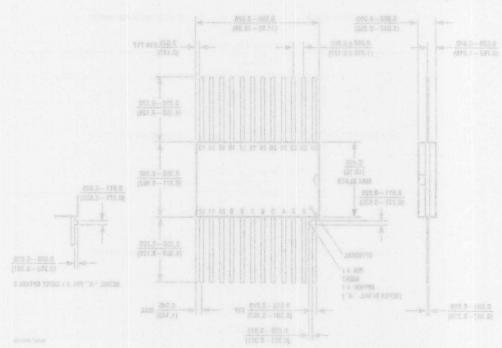


#### 24 Lead Ceramic Flatpak (F) NS Package Number W24C



#### 24 Lead Ceramic Flatpak (F) NS Package Number W24C







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• MM54HC/MM74HCT 

MM54HCT/MM74HCT 

• CDAXXX 

• MM54CXXX/MM74CXXX 

• Surface Mount

#### DATA ACQUISITION LINEAR DEVICES-1989

Active Filters \* Analog Switches/Multiplaxers \* Analog to Digital Converters \* Digital to-Analog Conveners

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#### DISCRETE SEMICONDUCTOR PRODUCTS DATABOOK -- 1989

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Oynamic Memory Control © Error Detection and Correction • Microprocessor Applications for the DP8408A/08A/17/18/18/28/29 • Microprocessor Applications for the DP8420A/21A/22A Microprocessor Applications for the NS32CG821

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Description and Family Characteristics • Ratings, Specifications and Waveforms
Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX • Quiet Series: 54ACQ/74ACQXXX
Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA

#### FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—1990

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#### FAST® APPLICATIONS HANDBOOK—1990

Reprint of 1987 Fairchild FAST Applications Handbook

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FAST Characteristics and Testing • Packaging Characteristics

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The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

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Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program
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Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

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Audio Circuits • Radio Circuits • Video Circuits • Motion Control Circuits • Special Function Circuits • Tons softeness of Tead Surface Mount

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DOAL MANAGERII BUBINABA IARA MADIALI

prications using com monoritric and tryone circuits from reacosal semiconoucios. dividual application notes are nomally written to explain the operation and use of one particular device or to detail various ethods of ecocomplishing a given function. The organization of this handbook takes advantage of this innate coherence by seging each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

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